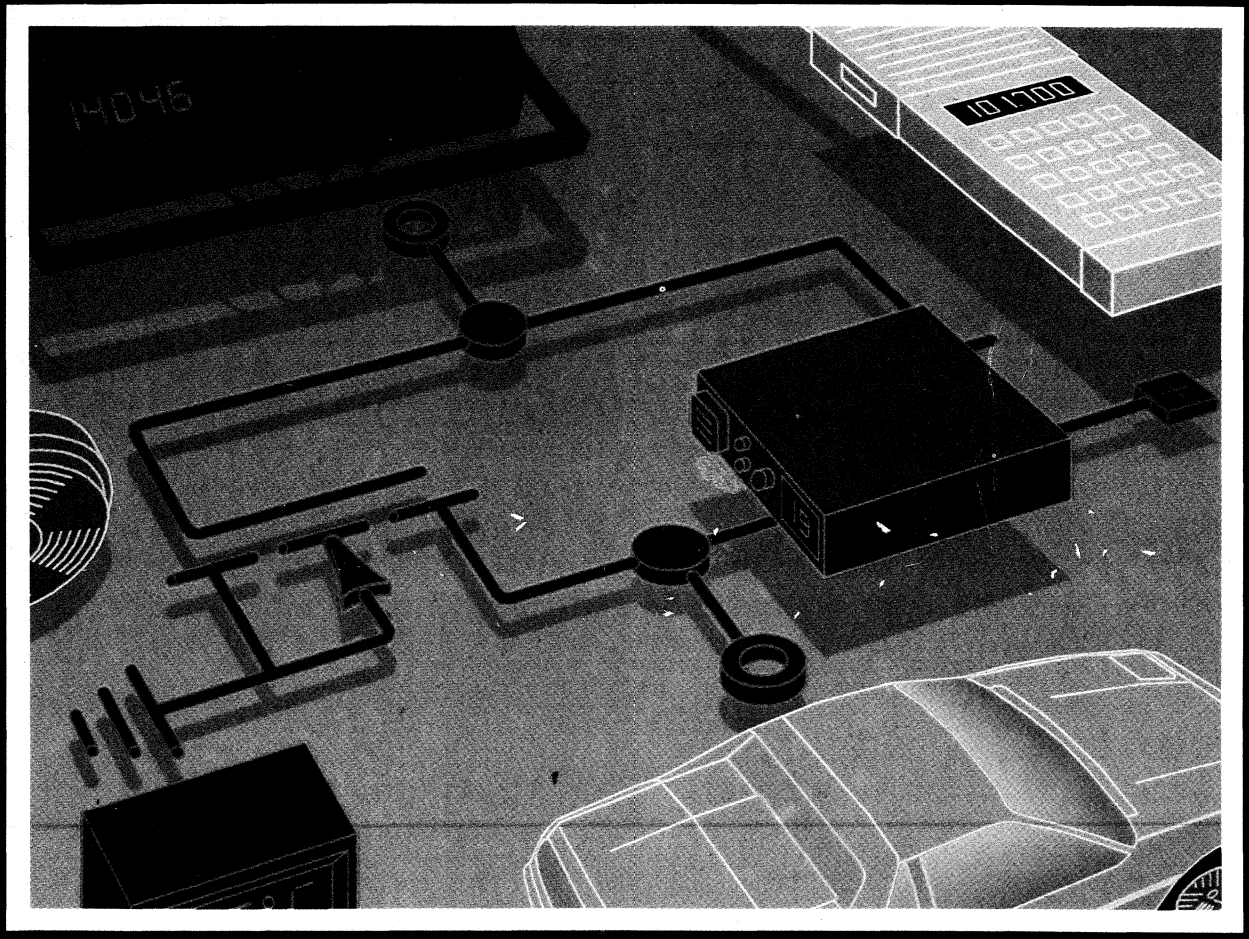
DL130
REV 1

MOTOROLA



CMOS APPLICATION-SPECIFIC STANDARD ICs

(Formerly CMOS/NMOS Special Functions)

Handling and Design Guidelines

ADCs/DACs

Decoders/Display Drivers

Operational Amplifiers/Comparators

PLL Frequency Synthesizers

Remote Control Functions

Smoke Detectors

Miscellaneous Functions

Reliability

Applications Information 1

Package Dimensions 1

Handling and Design Guidelines

ADCs/DACs

Decoders/Display Drivers

Operational Amplifiers/Comparators

PLL Frequency Synthesizers

Remote Control Functions

Smoke Detectors

Miscellaneous Functions

Reliability

Applications Information

Package Dimensions

MOTOROLA

CMOS APPLICATION-SPECIFIC STANDARD DIGITAL-ANALOG INTEGRATED CIRCUITS

(Formerly CMOS/NMOS Special Functions)

Prepared by
Technical Information Center

This book presents technical data for CMOS application-specific standard digital-analog integrated circuits. Complete specifications are provided in the form of data sheets. In addition, a function selector guide may be found at the beginning of each chapter. Handling precautions and applications chapters have been included to familiarize the user with these circuits.

For marketing and application information contact your local Motorola Semiconductor sales office or:

Motorola Inc.
P.O. Box 6000
Austin, TX 78762

Attn: MOS Digital-Analog IC Marketing
Mail Stop: F-8

DL130/D

Printed in U.S.A.

DATA CLASSIFICATION

Product Preview

This heading on a data sheet indicates that the device is in the formative stages or in design (under development) at the time of printing of this data book. Please check with Motorola for current status. The disclaimer at the bottom of the first page reads: "This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice."

Advance Information

This heading on a data sheet indicates that the device is in sampling, preproduction, or first production stages at the time of printing of this data book. Please check with Motorola for updated information. The disclaimer at the bottom of the first page reads: "This document contains information on a new product. Specifications and information herein are subject to change without notice."

Fully Released

A fully released data sheet contains neither a classification heading nor a disclaimer at the bottom of the first page. This document contains information on a product in full production. Guaranteed limits will not be changed without written notice to your local Motorola Semiconductor Sales Office.

CONTENTS

		Page
Alphanumeric Index		ix
Chapter 1 Handling and Design Guidelines		
Handling and Design Guidelines		1-3
CMOS Latch Up		1-5
Chapter 2 ADCs/DACs		
Selector Guide for ADCs/DACs		2-2
MC14433	3 1/2 Digit A/D Converter	2-3
MC14442	8-Bit A/D Converter with Parallel Interface	2-15
MC14443	6-Channel A/D Converter Subsystem	2-24
MC14444	8- Bit A/D Converter	Note 1
MC14447	6-Channel A/D Converter Subsystem	2-24
MC144110	6-Bit D/A Converter with Serial Interface	2-29
MC144111	6-Bit D/A Converter with Serial Interface	2-29
MC145040	8-Bit A/D Converter with Serial Interface	2-35
MC145041	8-Bit A/D Converter with Serial Interface	2-35
MC145050	10- Bit A/D Converter with Serial Interface	2-44
MC145051	10-Bit A/D Converter with Serial Interface	2-44
MC145053	10-Bit A/D Converter with Serial Interface	2-57
Chapter 3 Decoders/Display Drivers		
Selector Guide for Decoders/Display Drivers		3-2
MC14489	Multi-Character LED Display/Lamp Driver	3-3
MC14495-1	Hex-to-7 Segment Latch/Decoder/LED Driver	3-20
MC14499	7-Segment LED Display Decoder/Driver	3-25
MC145000	Serial Input Multiplexed LCD Driver (Master)	3-31
MC145001	Serial Input Multiplexed LCD Driver (Slave)	3-31
MC145453	LCD Driver with Serial Interface	3-42
Chapter 4 Operational Amplifiers/Comparators		
Selector Guide for Operational Amplifiers Comparators		4-2
MC14471	Low-Power Comparators plus Alarm Driver Circuitry	4-3
MC14573	Quad Programmable Operational Amplifier	4-8
MC14574	Quad Programmable Comparator	4-8
MC14575	Programmable Dual Operational Amplifier/Dual Comparator	4-8
MC14576A	Dual Video Amplifier	4-17
MC14577A	Dual Video Amplifier	4-17
MC14578	Micro-Power Comparator plus Voltage Follower	4-23
Chapter 5 PLL Frequency Synthesizers (PLL FS)		
Selector Guide for PLL FS		5-2
MC145106	PLL FS (Single Modulus)	5-3
MC145145-2	4-Bit Data Bus Input PLL FS (Single-Modulus)	5-10
MC145146-2	4-Bit Data Bus Input PLL FS (Dual-Modulus)	5-22
MC145149	Dual PLL FS (Dual-Modulus)	5-34
MC145151-2	Parallel Input PLL FS (Single-Modulus)	5-45
MC145152-2	Parallel Input PLL FS (Dual-Modulus)	5-45
MC145155-2	Serial Input PLL FS (Single-Modulus)	5-45
MC145156-2	Serial Input PLL FS (Dual-Modulus)	5-45
MC145157-2	Serial Input PLL FS (Single-Modulus)	5-45
MC145158-2	Serial Input PLL FS (Dual-Modulus)	5-45

ALPHANUMERIC INDEX

Device Number	Function	Page Number
MC68HC68T1	Real Time Clock plus RAM with Serial Interface	8-3
MC14433	3 1/2 Digit A/D Converter	2-3
MC14442	8-Bit A/D Converter with Parallel Interface	2-15
MC14443	6-Channel A/D Converter Subsystem	2-24
MC14444	8 Bit A/D Converter	Note 1
MC14447	6-Channel A/D Converter Subsystem	2-24
MC14457	Remote Control Transmitter	Note 1
MC14458	Remote Control Receiver	Note 1
MC14460	Automotive Speed Control Processor	Note 1
MC14466	Ionization Smoke Detector (Battery)	Note 1
MC14467-1	Ionization Smoke Detector (Battery)	7-3
MC14468	Ionization Smoke Detector with I/O (Battery)	7-8
MC14469	Addressable Asynchronous Receiver/Transmitter	6-3
MC14470	Ionization Smoke Detector with I/O (Line)	7-13
MC14471	Low-Power Comparators plus Alarm Driver Circuitry	4-3
MC14489	Multi-Character LED Display/Lamp Driver	3-3
MC14495-1	Hex-to-7 Segment Latch/Decoder/LED Driver	3-20
MC14497	PCM Remote Control Transmitter	6-11
MC14499	7-Segment LED Display Decoder/Driver	3-25
MC14573	Quad Programmable Op Amp	4-8
MC14574	Quad Programmable Comparator	4-8
MC14575	Programmable Dual Op Amp/Dual Comparator	4-8
MC14576A	Dual Video Amplifier	4-17
MC14577A	Dual Video Amplifier	4-17
MC14578	Micro-Power Comparator plus Voltage Follower (Line)	7-18, 4–23
MC141620	Enhanced Comb Filter	8-25
MC144110	6-Bit D/A Converter with Serial Interface	2-29
MC144111	6-Bit D/A Converter with Serial Interface	2-29
MC145000	Serial Input Multiplexed LCD Driver (Master)	3-31
MC145001	Serial Input Multiplexed LCD Driver (Slave)	3-31
MC145010	Photoelectric Smoke Detector with I/O (Battery)	7-21
MC145011	Photoelectric Smoke Detector with I/O (Line)	7-31
MC145026	Remote Control Encoder	6-17
MC145027	Remote Control Decoder	6-17
MC145028	Remote Control Decoder	6-17
MC145029	Remote Control Decoder	Note 1
MC145030	Remote Control Encoder/Decoder	6-35
MC145031	Remote Control Encoder	6-43
MC145032	Remote Control Decoder	6-43
MC145033	Remote Control Encoder/Decoder	6-43
MC145034	Remote Control Encoder	6-43
MC145035	Remote Control Decoder	6-43
MC145040	8-Bit A/D Converter with Serial Interface	2-35
MC145041	8-Bit A/D Converter with Serial Interface	2-35
MC145050	10-Bit A/D Converter with Serial Interface	2-44
MC145051	10-Bit A/D Converter with Serial Interface	2-44
MC145053	10-Bit A/D Converter with Serial Interface	2-57
MC145106	PLL FS (Single-Modulus)	5-3

Handling and Design Guidelines

HANDLING PRECAUTIONS

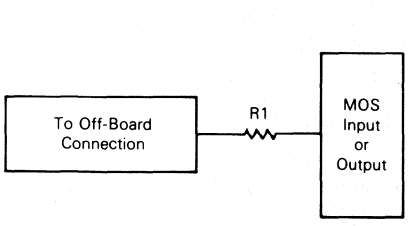
All MOS devices have an insulated gate that is subject to voltage breakdown. The high-impedance gates on the devices are protected by on-chip networks. However, these on-chip networks do not make the IC immune to electrostatic damage (ESD). Laboratory tests show that devices may fail after one very-high voltage discharge. They may also fail due to the cumulative effect of several discharges of lower potential.

Static-damaged devices behave in various ways, depending on the severity of the damage. The most severely damaged are the easiest to detect because the input or output has been completely destroyed and is either shorted to V_{DD}, shorted to V_{SS}, or open-circuited. The effect is that the device is no longer functional. Less severe cases are more difficult to detect because they appear as intermittent failures or degraded performance. Another effect of static damage is, often, increased leakage currents.

CMOS and NMOS devices are not immune to large static voltage discharges that can be generated while handling. For example, static voltages generated by a person walking across a waxed floor have been measured in the 4-15 kV range (depending on humidity, surface conditions, etc.). Therefore, the following precautions should be observed.

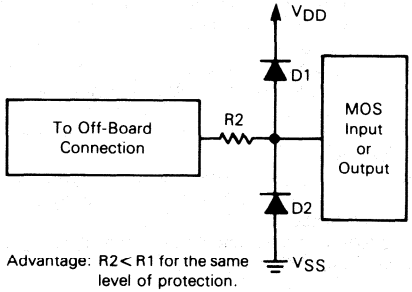
1. Do not exceed the Maximum Ratings specified by the data sheet.
2. All unused device inputs should be connected to V_{DD} or V_{SS}.
3. All low-impedance equipment (pulse generators, etc.) should be connected to CMOS or NMOS inputs only after the device is powered up. Similarly, this type of equipment should be disconnected before power is turned off.
4. A circuit board containing CMOS or NMOS devices is merely an extension of the device and the same handling precautions apply. Contacting edge connectors wired directly to devices can cause damage. Plastic wrapping should be avoided. When external connections to a PC board address pins of CMOS or NMOS integrated circuits, a resistor should be used in series with the inputs or outputs. The limiting factor for the series resistor is the added delay caused by the time constant formed by the series resistor and input capacitance. This resistor will help limit accidental damage if the PC board is removed and brought into contact with static generating materials. For convenience, equations for added propagation delay and rise time effects due to series resistance size are given in Figure 1.

FIGURE 1 — NETWORKS FOR MINIMIZING ESD AND REDUCING CMOS LATCH UP SUSCEPTIBILITY



Advantage: Requires minimal board area

Disadvantage: R1 > R2 for the same level of protection, therefore rise and fall times, propagation delays, and output drives are severely affected.



Advantage: R2 < R1 for the same level of protection. Impact on ac and dc characteristics is minimized.

Disadvantage: More board area, higher initial cost

Note: These networks are useful for protecting the following:
A. digital inputs and outputs
B. analog inputs and outputs
C. 3-state outputs
D. bidirectional (I/O) ports

EQUATION 1 — PROPAGATION DELAY vs. SERIES RESISTANCE

$$R \approx \frac{t}{C \cdot k}$$

where:
R = the maximum allowable series resistance in ohms
t = the maximum tolerable propagation delay in seconds
C = the board capacitance plus the driven device's input capacitance in farads
k = 0.33 for devices with TTL input levels (switch point ≈ 1.3 V)
k = 0.7 for devices with CMOS input levels (switch point ≈ 50% V_{DD})

EQUATION 2 — RISE TIME vs. SERIES RESISTANCE

$$R \approx \frac{t}{C \cdot k}$$

where:
R = the maximum allowable series resistance in ohms
t = the maximum rise time per data sheet in seconds
C = the board capacitance plus the driven device's input capacitance in farads
k = 0.7 for devices with TTL input levels (switch point ≈ 1.3 V)
k = 2.3 for devices with CMOS input levels (switch point ≈ 50% V_{DD})

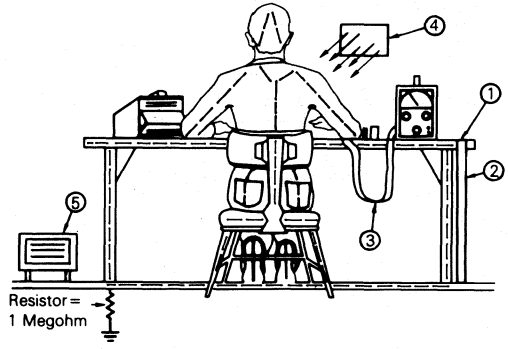
5. All CMOS or NMOS devices should be stored or transported in materials that are antistatic. Devices must not be inserted into conventional plastic "snow", styrofoam or plastic trays, but should be left in their original container until ready for use.
6. All CMOS or NMOS devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices, since a worker can be statically charged with respect to the bench surface. Wrist straps in contact with skin are strongly recommended. See Figure 2.
7. Nylon or other static generating materials should not come in contact with CMOS or NMOS circuits.
8. If automatic handling is being used, high levels of static electricity may be generated by the movement of devices, belts, or boards. Reduce static build-up by using ionized air blowers or room humidifiers. All parts of machines which come into contact with the top, bottom, and sides of IC packages must be grounded metal or other conductive material.
9. Cold chambers using CO_2 for cooling should be equipped with baffles, and devices must be contained on or in conductive material.
10. When lead-straightening or hand-soldering is necessary, provide ground straps for the apparatus used and be sure that soldering ties are grounded.
11. The following steps should be observed during wave solder operations.
    a. The solder pot and conductive conveyor system of the wave soldering machine must be grounded to an earth ground.
    b. The loading and unloading work benches should have conductive tops which are grounded to an earth ground.
    c. Operators must comply with precautions previously explained.
    d. Completed assemblies should be placed in antistatic containers prior to being moved to subsequent stations.
12. The following steps should be observed during board cleaning operation.
    a. Vapor degreasers and baskets must be grounded to an earth ground. Operators must likewise be grounded.
    b. Brush or spray cleaning should not be used.
    c. Assemblies should be placed into the vapor degreaser immediately upon removal from the antistatic container.
    d. Cleaned assemblies should be placed in antistatic containers immediately after removal from the cleaning basket.
    e. High velocity air movement or application of solvents and coatings should be employed only when module circuits are grounded and a static eliminator is directed at the module.
13. The use of static detection meters for line surveillance is highly recommended.
14. Equipment specifications should alert users to the presence of CMOS or NMOS devices and require familiarization with this specification prior to performing any kind of maintenance or replacement of devices or modules.
15. Do not insert or remove CMOS or NMOS devices from test sockets with power applied. Check all power supplies to be used for testing devices to be certain there are no voltage transients present.
16. Double check test equipment setup for proper polarity of voltage before conducting parametric or functional testing.

RECOMMENDED FOR READING

"Total Control of the Static in Your Business"

Available by writing to:
3M Company
Static Controls Systems
Building A145-3N-01
P.O. Box 2963
Austin, Texas 78769-2963
Or by Calling:
1-800-328-1368

FIGURE 2 — TYPICAL MANUFACTURING WORK STATION



NOTES: 1. 1/16 inch conductive sheet stock covering bench top work area.
2. Ground strap.
3. Wrist strap in contact with skin.
4. Static neutralizer. (Ionized air blower directed at work.) Primarily for use in areas where direct grounding is impractical.
5. Room humidifier. Primarily for use in areas where the relative humidity is less than 45%. Caution: building heating and cooling systems usually dry the air causing the relative humidity inside of buildings to be less than outside humidity.

CMOS LATCH UP

Latch up will not be a problem for most designs, but the designer should be aware of it, what causes it, and how to prevent it.

Figure 3 shows the layout of a typical CMOS inverter and Figure 4 shows the parasitic bipolar devices that are formed. The circuit formed by the parasitic transistors and resistors is the basic configuration of a silicon controlled rectifier, or SCR. In the latch-up condition, transistors Q1 and Q2 are turned on, each providing the base current necessary for the other to remain in saturation, thereby latching the devices on. Unlike a conventional SCR, where the device is turned on by applying a voltage to the base of the NPN transistor, the parasitic SCR is turned on by applying a voltage to the emitter of either transistor. The two emitters that trigger the SCR are the same point, the CMOS output. Therefore, to latch up the CMOS device, the output voltage must be greater than V_{DD} + 0.5 Vdc or less than − 0.5 Vdc and have sufficient current to trigger the SCR. The latch-up mechanism is similar for the inputs.

Once a CMOS device is latched up, if the supply current is not limited, the device will be destroyed. Ways to prevent such occurrences are listed below.

1. Insure that inputs and outputs are limited to the maximum rated values given in the data sheet.
2. If voltage transients of sufficient energy to latch up the device are expected on the outputs, external protection diodes can be used to clamp the voltage. Another method of protection is to use a series resistor to limit the expected worst case current to the Maximum Ratings values. See Figure 1.
3. If voltage transients are expected on the inputs, protection diodes may be used to clamp the voltage or a series resistor may be used to limit the current to a level less than the maximum rating given in the data sheet. See Figure 1.
4. Sequence power supplies so that the inputs or outputs of CMOS devices are not powered up first (e.g., recessed edge connectors may be used in plug-in board applications and/or series resistors).
5. Power supply lines should be free of excessive noise. Care in board layout and filtering should be used.
6. Limit the available power supply current to the devices that are subject to latch-up conditions. This can be accomplished with the power supply filtering network or with a current-limiting regulator.

FIGURE 3 — CMOS WAFER CROSS SECTION

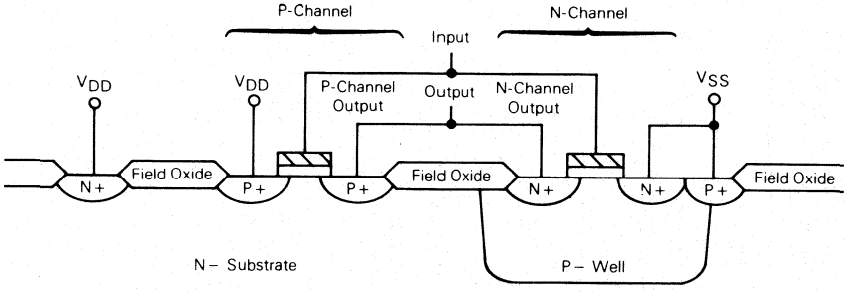
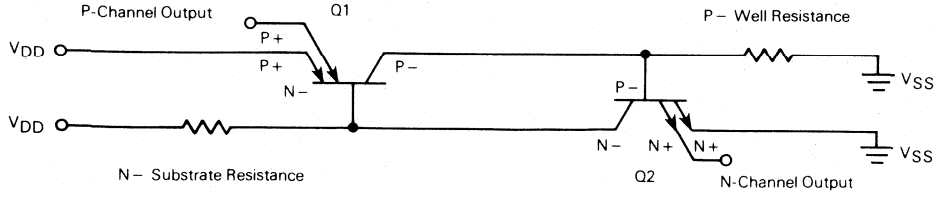


FIGURE 4 — LATCH UP CIRCUIT SCHEMATIC



ADCs/DACs

ADCs/DACs

		Page No.
MC14433	3 1/2 Digit A/D Converter	2-3
MC14442	8-Bit A/D Converter with Parallel Interface	2-15
MC14443	6-Channel A/D Converter Subsystem	2-24
MC14447	6-Channel A/D Converter Subsystem	2-24
MC144110	6-Bit D/A Converter with Serial Interface	2-29
MC144111	6-Bit D/A Converter with Serial Interface	2-29
MC145040	8-Bit A/D Converter with Serial Interface	2-35
MC145041	8-Bit A/D Converter with Serial Interface	2-35
MC145050	10-Bit A/D Converter with Serial Interface	2-44
MC145051	10-Bit A/D Converter with Serial Interface	2-44
MC145053	10-Bit A/D Converter with Serial Interface	2-57

SELECTOR GUIDE

Function	I/O Format	Resolution	Number of Analog Channels	On-Chip Oscillator	Other Features	Device Number
ADC	Serial	8 Bits	11	—	Successive Approximation	**MC145040**
		10 Bits	11			**MC145050**
		8 Bits	11	√	Successive Approximation	**MC145041**
		10 Bits	11			**MC145051**
		10 Bits	5			**MC145053**
	Parallel	3 1/2 Digit BCD	1	√	Dual Slope	**MC14433**
		8 Bits	11	—	Successive Approximation	**MC14442**
ADC Linear Subsystem	Parallel	8 to 10 Bits	6	—	Single Slope w/ Auto Zeroing	**MC14443**
		8 to 10 Bits	6	—	Single Slope w/ Auto Zeroing	**MC14447**
DAC	Serial	6 Bits	6	—	Emitter-Follower Outputs	**MC144110**
		6 Bits	4	—	Emitter-Follower Outputs	**MC144111**

MC14433

3½ DIGIT A/D CONVERTER

The MC14433 is a high-performance, low-power, 3½ digit A/D converter combining both linear CMOS and digital CMOS circuits on a single monolithic IC. The MC14433 is designed to minimize use of external components. With two external resistors and two external capacitors, the system forms a dual-slope A/D converter with automatic zero correction and automatic polarity.

The MC14433 is ratiometric and may be used over a full-scale range of 1.999 volts or 199.9 millivolts. Systems using the MC14433 may operate over a wide range of power supply voltages for ease of use with batteries, or with standard 5 volt supplies. The output drive conforms with standard B-Series CMOS specifications and can drive a low-power Schottky TTL load.

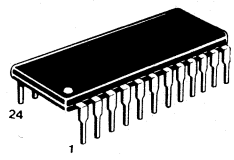
The high-impedance MOS inputs allow applications in current and resistance meters as well as voltmeters. In addition to DVM/DPM applications, the MC14433 finds use in digital thermometers, digital scales, remote A/D, A/D control systems, and in MPU systems.

- Accuracy: ±0.05% of Reading ±1 Count
- Two Voltage Ranges: 1.999 V and 199.9 mV
- Up to 25 Conversions per Second
- Z_{in} > 1000 M ohm
- Auto-Polarity and Auto-Zero
- Single Positive Voltage Reference
- Standard B-Series CMOS Outputs — Drives One Low Power Schottky Load
- Uses On-Chip System Clock, or External Clock
- Wide Supply Range: e.g., ±4.5 V to ±8.0 V
- Overrange and Underrange Signals Available
- Operates in Auto Ranging Circuits
- Operates with LED and LCD displays
- Low External Component Count
- Chip Complexity: 1326 FETs

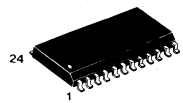
CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

3½ DIGIT A/D CONVERTER



P SUFFIX
PLASTIC DIP
CASE 709

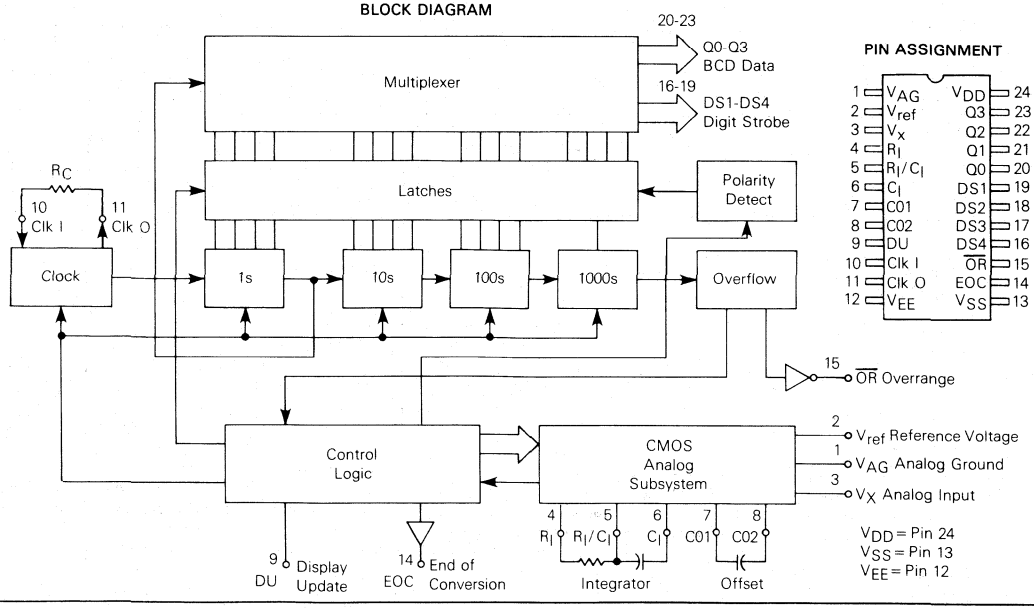


DW SUFFIX
SOG
CASE 751E

ORDERING INFORMATION

MC14433P	Plastic DIP
MC14433DW	SOG Package

BLOCK DIAGRAM



PIN ASSIGNMENT

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD} to V_{EE}	−0.5 to +18	V
Voltage, any pin, referenced to V_{EE}	V	−0.5 to V_{DD} +0.5	V
DC Input Current, per Pin	I_{in}	±10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{EE} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0 or V_{EE})

Parameter	Symbol	Value	Unit
DC Supply Voltage — V_{DD} to Analog Ground	V_{DD}	+5.0 to +8.0	Vdc
V_{EE} to Analog Ground	V_{EE}	−2.8 to −8.0	
Clock Frequency	f_{Clk}	32 to 400	kHz
Zero Offset Correction Capacitor	C_O	0.1 ± 20%	μF

ELECTRICAL CHARACTERISTICS (C_I = 0.1 μF mylar, R_I = 470 kΩ@V_{ref} = 2.000 V, R_I = 27 kΩ@V_{ref} = 200.0 mV, C_O = 0.1 μF, R_C = 300 kΩ; all voltages referenced to Analog Ground, pin 1, unless otherwise indicated)

Characteristic	Symbol	V_{DD} Vdc	V_{EE} Vdc	−40°C Min	−40°C Max	25°C Min	25°C Typ#	25°C Max	85°C Min	85°C Max	Unit
Linearity-Output Reading (Note 1)	–										%rdg
(V_{ref} = 2.000 V)		5.0	−5.0	–	–	−0.05 −1 Count	±0.05	+0.05 +1 Count	–	–	
(V_{ref} = 200.0 mV)		5.0	−5.0	–	–	–	±0.05	–	–	–	
Stability — Output Reading											
(V_X = 199.0 mV, V_{ref} = 200.0 mV)	–	5.0	−5.0					3			LSD
Symmetry — Output Reading (Note 2)											
(V_{ref} = 2.000 V)	–	5.0	−5.0					4			LSD
Zero-Output Reading											
(V_X = 0 V, V_{ref} = 2.000 V)	–	5.0	−5.0	–	–	–	0	0	–	–	LSD
Bias Current — Analog Input	–	5.0	−5.0	–	–	–	±20	±100	–	–	pA
Reference Input		5.0	−5.0	–	–	–	±20	±100	–	–	
Analog Ground		5.0	−5.0	–	–	–	±20	±500	–	–	
Common Mode Rejection (f_{clk} = 32 kHz,											
V_X = 1.4 V, V_{ref} = 2.000 V)	–	5.0	−5.0	–	–	–	65	–	–	–	dB
Input Voltage* Pins 9, 10 "0" Level	V_{IL}										V
(V_O = 4.5 or 0.5 V)		5.0	–	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 V)		10	–	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 V)		15	–	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}										V
(V_O = 0.5 or 4.5 V)		5.0	–	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 V)		10	–	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 V)		15	–	11.0	–	11.0	8.25	–	11.0	–	
Output Voltage — Pins 14 to 23											V
(V_{SS} = 0 V) "0" Level	V_{OL}	5.0	−5.0	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	−5.0	4.95	–	4.95	5.0	–	4.95	–	
(V_{SS} = −5.0 V) "0" Level	V_{OL}	5.0	−5.0	–	−4.95	–	−5.0	−4.95	–	−4.95	
"1" Level	V_{OH}	5.0	−5.0	4.95	–	4.95	5.0	–	4.95	–	
Output Current — Pins 14 to 23											mA
(V_{SS} = 0 V)											
(V_{OH} = 4.6 V) Source	I_{OH}	5.0	−5.0	−0.25	–	−0.2	−0.36	–	−0.14	–	
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	−5.0	0.64	–	0.51	0.88	–	0.36	–	
(V_{SS} = −5.0 V)											
(V_{OH} = 4.5 V) Source	I_{OH}	5.0	−5.0	−0.62	–	−0.5	−0.9	–	−0.35	–	
(V_{OL} = −4.5 V) Sink	I_{OL}	5.0	−5.0	1.6	–	1.3	2.25	–	0.9	–	
Input Current — DU, Pin 9	I_{DU}	5.0	−5.0	–	±0.3	–	±0.00001	±0.3	–	±1.0	μA
Quiescent Current	I_Q	5.0	−5.0	–	3.7	–	0.9	2.0	–	1.6	mA
(V_{DD} to V_{EE}, I_{SS} = 0)		8.0	−8.0	–	7.4	–	1.8	4.0	–	3.2	
DC Supply Rejection											
(V_{DD} to V_{EE}, I_{SS} = 0, V_{ref} = 2.000 V)	–	5.0	−5.0	–	–	–	0.5	–	–	–	mV/V

Notes: 1. Accuracy — The accuracy of the meter at full scale is the accuracy of the setting of the reference voltage. Zero is recalculated during each conversion cycle. The meaningful specification is linearity. In other words, the deviation from correct reading for all inputs other than positive full scale and zero is defined as the linearity specification.

2. Symmetry — Defined as the difference between a negative and positive reading of the same voltage at or near full scale.

*Referenced to V_{SS} for Pin 9. Referenced to V_{EE} for Pin 10.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

TYPICAL CHARACTERISTICS

FIGURE 1 – TYPICAL ROLLOVER ERROR versus POWER SUPPLY SKEW

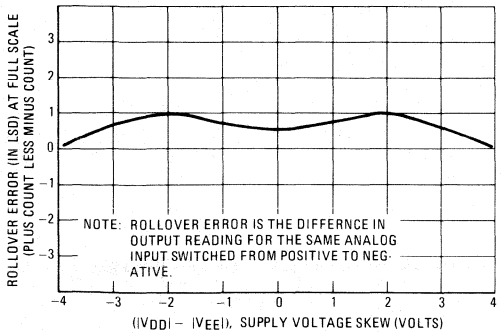


FIGURE 2 – TYPICAL QUIESCENT POWER SUPPLY CURRENT versus TEMPERATURE

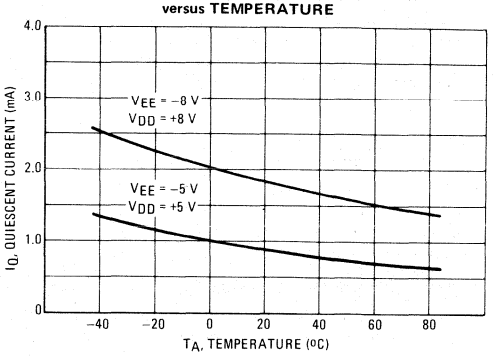


FIGURE 3 – TYPICAL N-CHANNEL SINK CURRENT AT $V_{DD}-V_{SS}$ = 5 VOLTS

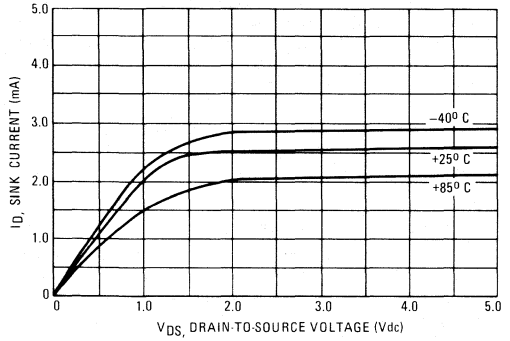


FIGURE 4 – TYPICAL P-CHANNEL SOURCE CURRENT AT $V_{DD}-V_{SS}$ = 5 VOLTS

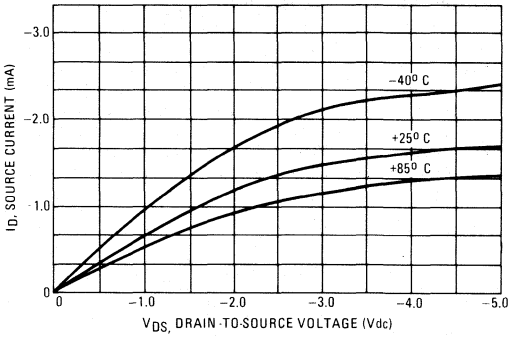


FIGURE 5 – TYPICAL CLOCK FREQUENCY versus RESISTOR (R_C)

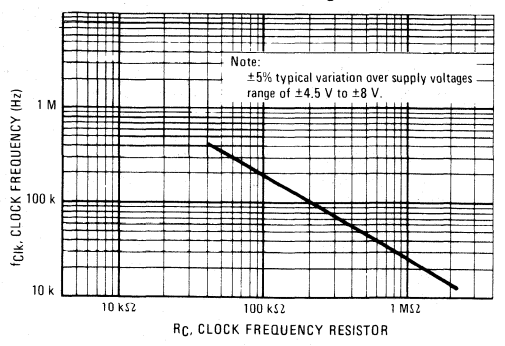
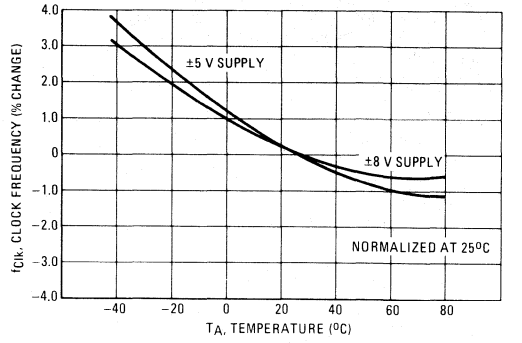


FIGURE 6 – TYPICAL % CHANGE OF CLOCK FREQUENCY versus TEMPERATURE



CONVERSION RATE = $\frac{\text{CLOCK FREQUENCY}}{16{,}400} \pm 1.5\%$
MULTIPLEX RATE = $\frac{\text{CLOCK FREQUENCY}}{80}$

PIN DESCRIPTIONS

ANALOG GROUND (V_{AG}, Pin 1)

Analog ground at this pin is the input reference level for the unknown input voltage (V_X) and reference voltage (V_{ref}). This pin is a high impedance input. The allowable operating range for V_{AG} is from V_{EE} +2.8 V to V_{DD} −4.5 V.

REFERENCE VOLTAGE (V_{ref}, Pin 2)
UNKNOWN INPUT VOLTAGE (V_X, Pin 3)

This A/D system performs a ratiometric A/D conversion; that is, the unknown input voltage, V_X, is measured as a ratio of the reference voltage, V_{ref}. The full scale voltage is equal to that voltage applied to V_{ref}. Therefore, a full scale voltage of 1.999 V requires a reference voltage of 2.000 V while full scale voltage of 199.9 mV requires a reference voltage of 200 mV. Both V_X and V_{ref} are high impedance inputs. In addition to being a reference input, Pin 2 functions as a reset for the A/D converter. When Pin 2 is switched low (referenced to V_{EE}) for at least 5 clock cycles, the system is reset to the beginning of a conversion cycle.

EXTERNAL COMPONENTS (R_I, R_I/C_I, C_I; Pins 4, 5, 6)

These pins are for external components for the integration used in the dual ramp A/D conversion. A typical value for the capacitor is 0.1 μF (polystyrene or mylar) while the resistor should be 470 kΩ for 2.0 V full scale operation and 27 kΩ for 200 mV full scale operation. These values are for a 66 kHz clock frequency which will produce a conversion time of approximately 250 ms. The equations governing the calculation for the values for integrator components are as follows:

$$R_I = \frac{V_X(max)}{C_I} \times \frac{T}{\Delta V}$$

$$\Delta V = V_{DD} - V_X(max) - 0.5\ V$$

$$T = 4000 \times \frac{1}{f_{Clk}}$$

where:

R_I is in kΩ
V_{DD} is the voltage at Pin 24 referenced to V_{AG}
V_X is the voltage at Pin 3 referenced to V_{AG}, in V
f_{Clk} is the clock frequency at Pin 10 in kHz
C_I is in μF, ΔV is in Volts
T is the conversion time, in ms

Example:

$C_I = 0.1\ \mu F$
$V_{DD} = 5.0$ volts
$f_{Clk} = 66$ kHz
For $V_X(max) = 2.0$ volts
$R_I = 480\ k\Omega$ (use 470 kΩ ± 5%)

For $V_X(max) = 200$ mV
$R_I = 28\ k\Omega$ (use 27 kΩ ± 5%)

Note that for worst case conditions, the minimum allowable value for R_I is a function of C_I min, V_{DD} min, and f_{Clk} max. The worst-case condition does not allow $\Delta V + V_X$ to exceed V_{DD}. The 0.5 V factor in the above equation for ΔV is for safety margin.

OFFSET CAPACITOR (C01, C02; Pins 7, 8)

These pins are used for connecting the offset correction capacitor. The recommended value is 0.1 μF (polystyrene or mylar).

DISPLAY UPDATE INPUT (DU, Pin 9)

If a positive edge is received on this input prior to the ramp-down cycle, new data will be strobed into the output latches during that conversion cycle. When this pin is wired directly to the EOC output (Pin 14), every conversion will be displayed. When this pin is driven from an external source, the voltage should be referenced to V_{SS}.

CLOCK (Clk I, Clk O, Pins 10, 11)

The MC14433 device contains its own oscillator system clock. A single resistor connected between pins 10 and 11 sets the clock frequency. If increased stability is desired, these pins will support a crystal or LC circuit. The clock input, Pin 10, may also be driven from an external clock source which need have only standard CMOS output drive. For external clock inputs this pin is referenced to V_{EE}. A 300 kΩ resistor results in clock frequency of about 66 kHz. (See the typical characteristic curves.) For alternate circuits see *Figure 7*.

NEGATIVE POWER SUPPLY (V_{EE}, Pin 12)

This is the connection for the most negative power supply voltage. The typical current is 0.8 mA. Note the current for the output drive circuit is not returned through this pin, but through Pin 13. V_X-V_{EE} should be greater than 0.8 V.

NEGATIVE POWER SUPPLY FOR OUTPUT CIRCUITRY AND INPUT DU (V_{SS}, Pin 13)

This is the low voltage level for the output pins of the MC14433 (BCD, Digit Selects, EOC, $\overline{OR}$) and the DU input. When this pin is connected to analog ground, the output voltage is from analog ground to V_{DD}. When connected to V_{EE}, the output swing is from V_{EE} to V_{DD}. The allowable operating range for V_{SS} is between V_{DD} −3.0 volts and V_{EE}.

END OF CONVERSION (EOC, Pin 14)

The EOC output produces a positive pulse at the end of each conversion cycle. This pulse width is equivalent to one half the period of the system clock (Pin 11).

OVERRANGE ($\overline{OR}$, Pin 15)

The $\overline{OR}$ pin is low when V_X exceeds V_{ref}. Normally it is high.

DIGIT SELECT (DS4, DS3, DS2, DS1; Pins 16, 17, 18, 19)

The digit select output is high when the respective digit is selected. The most significant digit (½ digit) turns on immediately after an EOC pulse followed by the remaining digits, sequencing from MSD to LSD. An interdigit blanking time of two clock periods is included to ensure that the BCD data has settled. The multiplex rate is equal to the clock frequency divided by 80. Thus with a system clock rate of 66 kHz, the multiplex rate would be 0.8 kHz. Relative timing among digital select outputs and the EOC signal is shown in the Digit Select Timing Diagram, Figure 8.

BCD DATA OUTPUTS (Q0, Q1, Q2, Q3, Pins 20, 21, 22, 23)

Multiplexed BCD outputs contain 3 full digits of information during DS2, 3, 4, while during DS1, the ½ digit, overrange, underrange and polarity are available. The adjacent truth table shows the formats of the information during DS1.

POSITIVE POWER SUPPLY (V_{DD}, Pin 24)

The most positive supply voltage pin. $V_{DD} - V_X$ should be greater than 2.5 V. $V_{DD} - V_{EE}$ should be greater than 7.8 V. V_{DD} determines V_{OH} for the digital outputs, and V_{IH} for the digital inputs.

TRUTH TABLE (DS1 = 1)

Coded Condition of MSD	Q3	Q2	Q1	Q0	BCD to 7 Segment Decoding
+0	1	1	1	0	Blank
−0	1	0	1	0	Blank
+0 UR	1	1	1	1	Blank
−0 UR	1	0	1	1	Blank
+1	0	1	0	0	4 → 1 } Hook up
−1	0	0	0	0	0 → 1 } only seg b
+1 OR	0	1	1	1	7 → 1 } and c to
−1 OR	0	0	1	1	3 → 1 } MSD

Notes for Truth Table:

Q3 – ½ digit, low for "1", high for "0"

Q2 – Polarity: "1" = positive, "0" = negative

Q0 – Out of range condition exists if Q0 = 1. When used in conjunction with Q3 the type of out of range condition is indicated, i.e., Q3 = 0 → OR or Q3 = 1 → UR.

When only segment b and c of the decoder are connected to the ½ digit of the display 4, 0, 7 and 3 appear as 1.

The overrange indication (Q3 = 0 and Q0 = 1) occurs when the count is greater than 1999, e.g., 1.999 V for a reference of 2.000 V. The underrange indication, useful for autoranging circuits, occurs when the count is less than 180, e.g., 0.180 V for a reference of 2.000 V.

Caution: If the most significant digit is connected to a display other than a "1" only; such as a full digit display, segments other than b and c must be disconnected. The BCD to seven segment decoder must blank on BCD inputs 1010 to 1111.

FIGURE 7 — ALTERNATE OSCILLATOR CIRCUITS

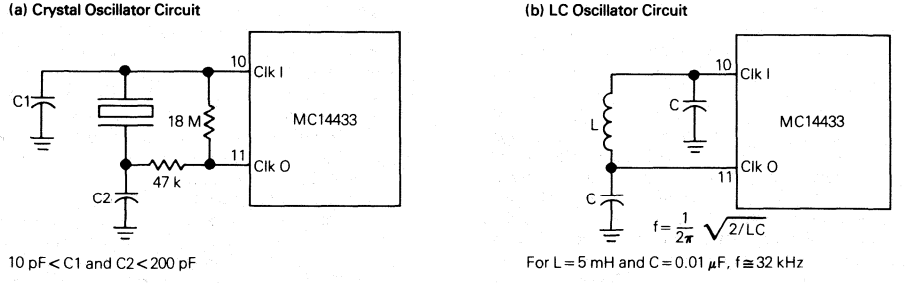


FIGURE 8 — DIGIT SELECT TIMING DIAGRAM

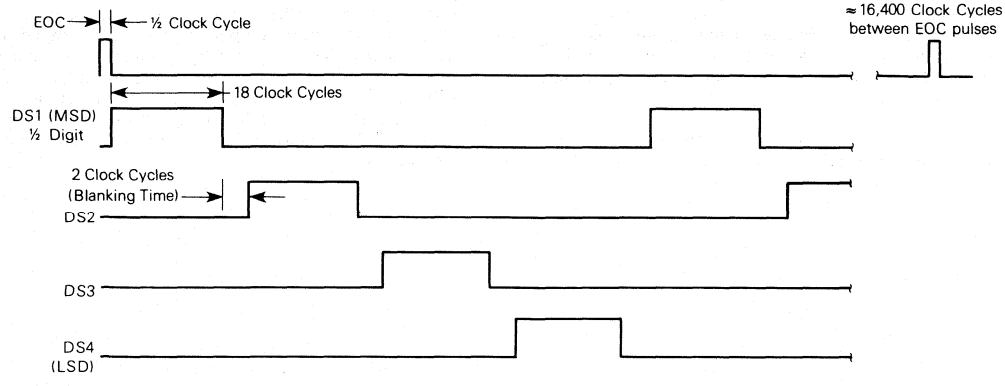


FIGURE 9 — INTEGRATOR WAVEFORMS AT PIN 6

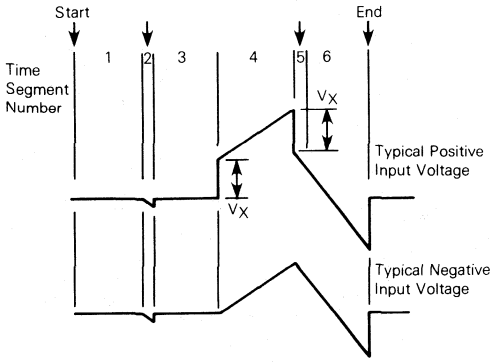
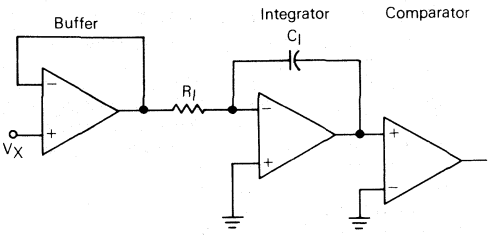


FIGURE 10 — EQUIVALENT CIRCUIT DIAGRAMS OF THE ANALOG SECTION DURING SEGMENT 4 OF THE TIMING CYCLE



CIRCUIT OPERATION

The MC14433 CMOS integrated circuit, together with a minimum number of external components, forms a modified dual ramp A/D converter. The device contains the customary CMOS digital logic providing counters, latches, and multiplexing circuitry as well as the CMOS analog circuitry providing operational amplifiers and comparators required to implement a complete single chip A/D. Autozero, high input impedances, and autopolarity are features of this system. Using CMOS technology, an A/D with a wide range of power supply voltage and low power consumption is now available with the MC14433.

During each conversion, the offset voltages of the internal amplifiers and comparators are compensated for by the system's autozero operation. Also each conversion 'ratiometrically' measures the unknown input voltage. In other words, the output reading is the ratio of the unknown voltage to the reference voltage with a ratio of 1 equal to the maximum count 1999. The entire conversion cycle requires slightly more than 16000 clock periods and may be divided into six different segments. The waveforms showing the conversion cycle with a positive input and a negative input are shown in Figure 9. The six segments of these waveforms are described below.

Segment 1 — The offset capacitor (C_O), which compensates for the input offset voltages of the buffer and integrator amplifiers, is charged during this period. Also, the integrator capacitor is shorted. This segment requires 4000 clock periods.

Segment 2 — The integrator output decreases to the comparator threshold voltage. At this time a number of counts equivalent to the input offset voltage of the comparator is stored in the offset latches for later use in the autozero process. The time for this segment is variable, and less than 800 clock periods.

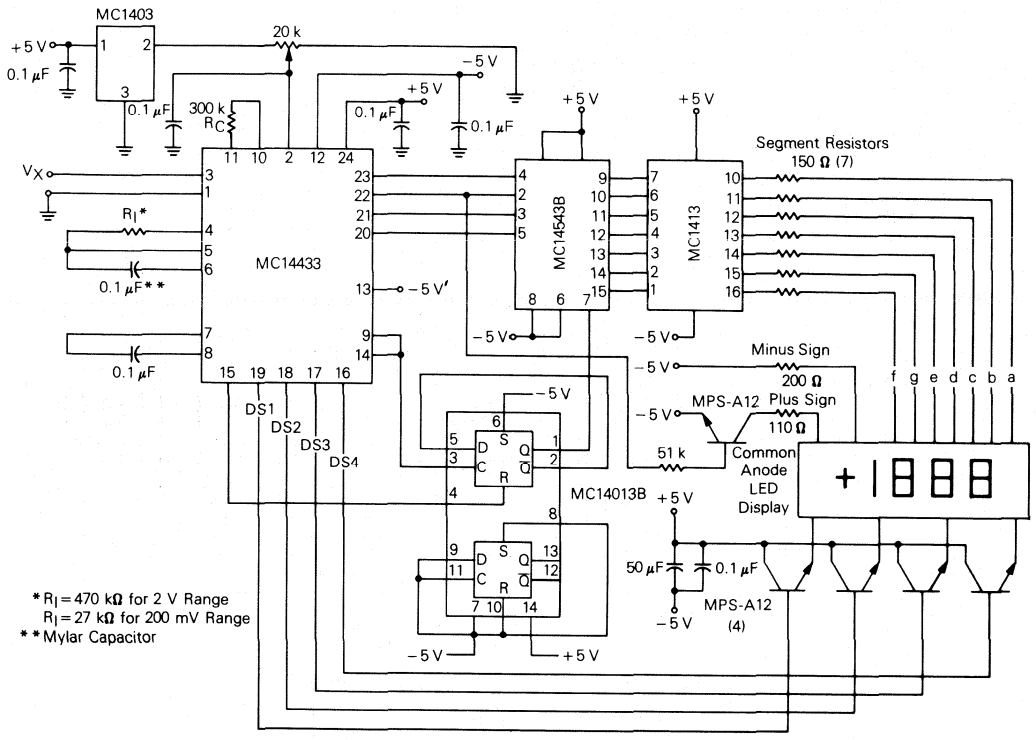
Segment 3 — This segment of the conversion cycle is the same as Segment 1.

Segment 4 — Segment 4 is an up-going ramp cycle with the unknown input voltage (V_X) as the input of the integrator. Figure 10 shows the equivalent configuration of the analog section of the MC14433 for a negative input voltage. When a positive input voltage is applied the buffer input is grounded and V_X is applied to the positive terminal which causes the integrator output to instantaneously jump by the magnitude of V_X as shown in the top waveform in Figure 9. This segment is exactly 4000 clock periods.

Segment 5 — This segment is a down-going ramp period with the reference voltage as the input to the integrator. Segment 5 of the conversion cycle has a time equal to the number of counts stored in the offset storage latches during Segment 2. As a result, the system zeros automatically.

Segment 6 — This is an extension of Segment 5. The time period for this portion is 4000 cycle periods. A BCD counter is reset to 0 at the beginning of Segment 6 and then begins to count up. When the output of the integrator causes the comparator to change state the BCD counter value is strobed into output latches to be multiplexed to the displays. The BCD counter continues to count, however, until it rolls over from 1999 to 0000. At this point the sequence counter is clocked back to sequence 1 and an end of conversion pulse is generated.

FIGURE 11 — 3½ DIGIT VOLTMETER—COMMON ANODE DISPLAYS, FLASHING OVERRANGE



APPLICATIONS INFORMATION

3½ DIGIT VOLTMETER — COMMON ANODE DISPLAYS, FLASHING OVERRANGE

An example of a 3½ digit voltmeter using the MC14433 is shown in the circuit diagram of Figure 11. The reference voltage for the system uses an MC1403 2.5 V reference IC. The full scale potentiometer can calibrate for a full scale of 199.9 mV or 1.999 V. When switching from 2 V to 200 mV operation, R_I is also changed, as shown on the diagram.

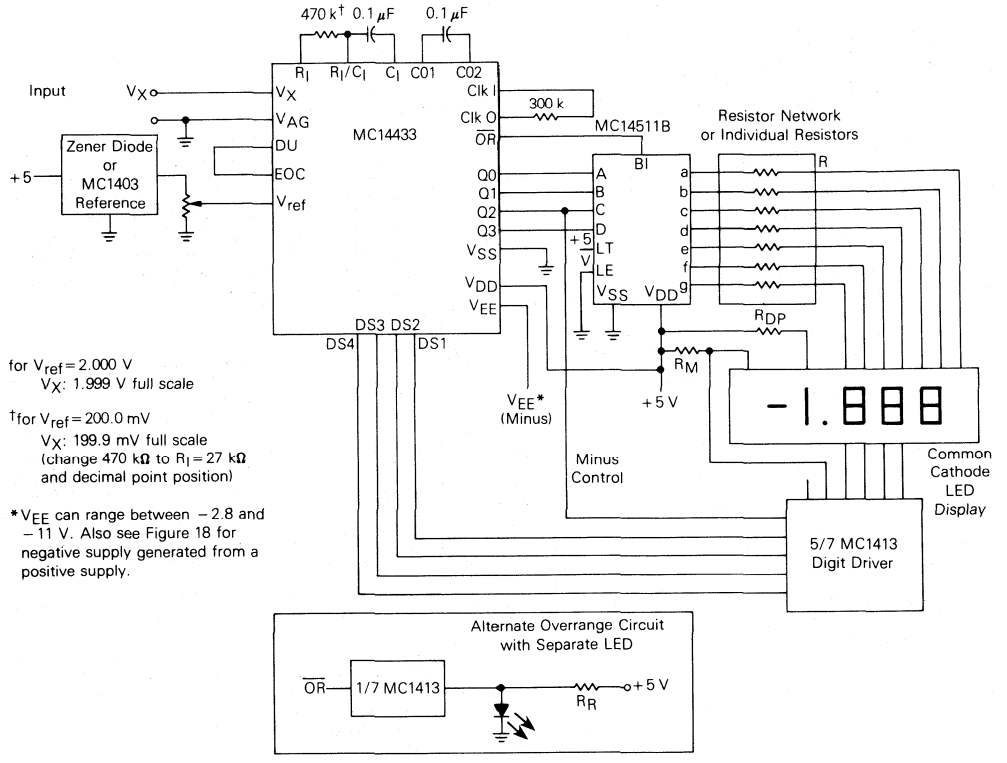
When using R_C equal to 300 kΩ, the clock frequency for the system is about 66 kHz. The resulting conversion time is approximately 250 ms.

When the input is overrange, the display flashes on and off. The flashing rate is one-half the conversion rate. This is done by dividing the EOC pulse rate by 2 with ½ MC14013B flip-flop and blanking the display using the blanking input of the MC14543B.

The display uses an LED display with common anode digit lines driven with an MC14543B decoder and an MC1413 LED driver. The MC1413 contains 7 Darlington transistor drivers and resistors to drive the segments of the display. The digit drive is provided by four MPS-A12 Darlington transistors operating in an emitter follower configuration. The MC14543B, MC14013B and LED displays are referenced to V_{EE} via Pin 13 of the MC14433. This places the full power supply voltage across the display. The current for the display may be adjusted by the value of the segment resistors shown as 150 ohms in the above figure.

The power supply for the system is shown as a dual ±5 V supply. However, the MC14433 will operate over a wide range of voltages, and balance between the +5 and −5 V supplies is *not* required. See the recommended operating conditions and Figure 1.

FIGURE 12 – 3½ DIGIT VOLTMETER WITH LOW COMPONENT COUNT



3½ DIGIT VOLTMETER WITH LOW COMPONENT COUNT USING COMMON CATHODE DISPLAYS

The 3½ digit voltmeter of Figure 12 is an example of the use of the MC14433 in a system with a minimum of components. This circuit uses only 11 components in addition to the MC14433 to operate the MC14433 and drive the LED displays.

In this circuit the MC14511B provides the segment drive for the 3½ digits. The MC1413 provides sink for digit current. (The MC1413 is a device with 7 Darlingtons with common emitters.) The worst case digit current is 7 times the segment current at ¼ duty cycle. The peak segment current is limited by the value of R. The current for the display flows from V_{DD} (+5 V) to ground and does not flow through the V_{EE} (negative) supply. The minus sign is controlled by one section of the MC1413 and is turned off by shunting the current through R_M to ground, bypassing the minus sign LED. The minus sign is derived from the Q2 output. The decimal point brightness is controlled by resistor R_{DP}. Since the brightness and the type and size of LED display are the choice of the designer, the values of resistors R, R_M, R_{DP}, and R_R that govern brightness are not given.

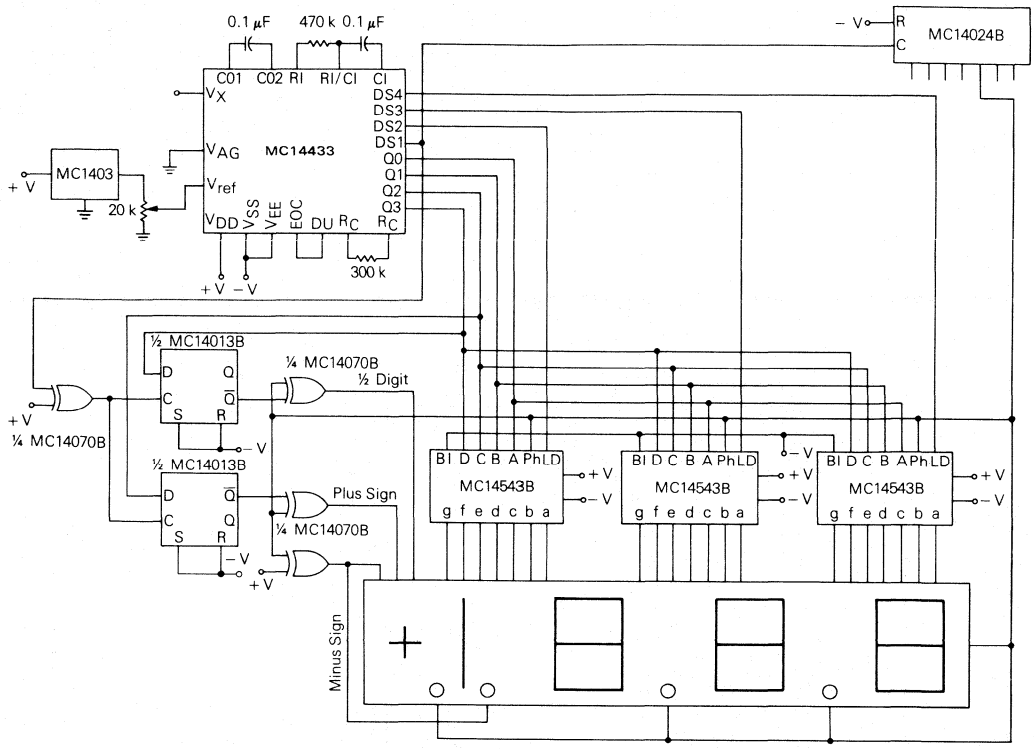
During an overrange condition the 3½ digit display is blanked at the BI pin on the MC14511B. The decimal point and minus sign will remain on during a negative overrange condition. In addition, an alternate overrange circuit with separate LED is shown.

3½ DIGIT VOLTMETER WITH LCD DISPLAY

A circuit for a 3½ digit voltmeter with a liquid crystal display is shown in Figure 13. Three MC14543B LCD latch/decoder/display drivers are used to demultiplex, decode the three digits, and drive the LCD. The half digit and polarity are demultiplexed with the MC14013B dual D flip-flop.

Since the LCD is best driven by an ac signal across the LCD, the low-frequency square wave drive for the LCD is derived from the MC14024B binary counter which divides the digit select output from the A/D. This low frequency square wave is connected to the backplane of the LCD and to the individual segments through the combination of the output cir-

FIGURE 13 — 3½ DIGIT VOLTMETER WITH LCD DISPLAY



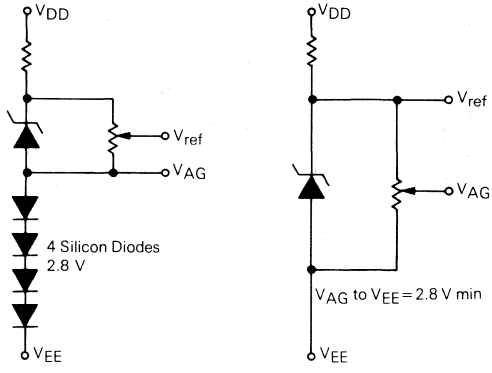
cuitry of the MC14543B and the exclusive OR gates at the outputs of the MC14013B. Alternatively the square wave can be derived from a 50/60 Hz input signal when available.

The minus sign and the decimal point to the right of the half digit are connected to the inverted low frequency square wave signal. Unused decimal points are tied directly to the low frequency square wave.

The system shown operates from two power supplies (plus and minus). Alternatively one supply can be used when V_{SS} is connected to V_{EE}. In this case a level must be set for analog ground, V_{AG}, which must be at least 2.8 V above V_{EE}. This circuit may be implemented with a resistor network, resistor/forward-biased diode network or resistor-zener diode network. For example, a 9 V supply can be used with 3 V between V_{AG} and V_{EE}, leaving 6 V for V_{DD} to V_{AG}. This system leaves a comfortable margin for battery degeneration (end of life). Two versions of this circuit for single supply operation is shown in Figure 14.

For panel meter operation from a single 5 V supply, a negative supply can be generated as shown in Figure 18.

FIGURE 14 — TWO CIRCUITS FOR GENERATION OF V_{ref} AND V_{AG} FROM A SINGLE SUPPLY



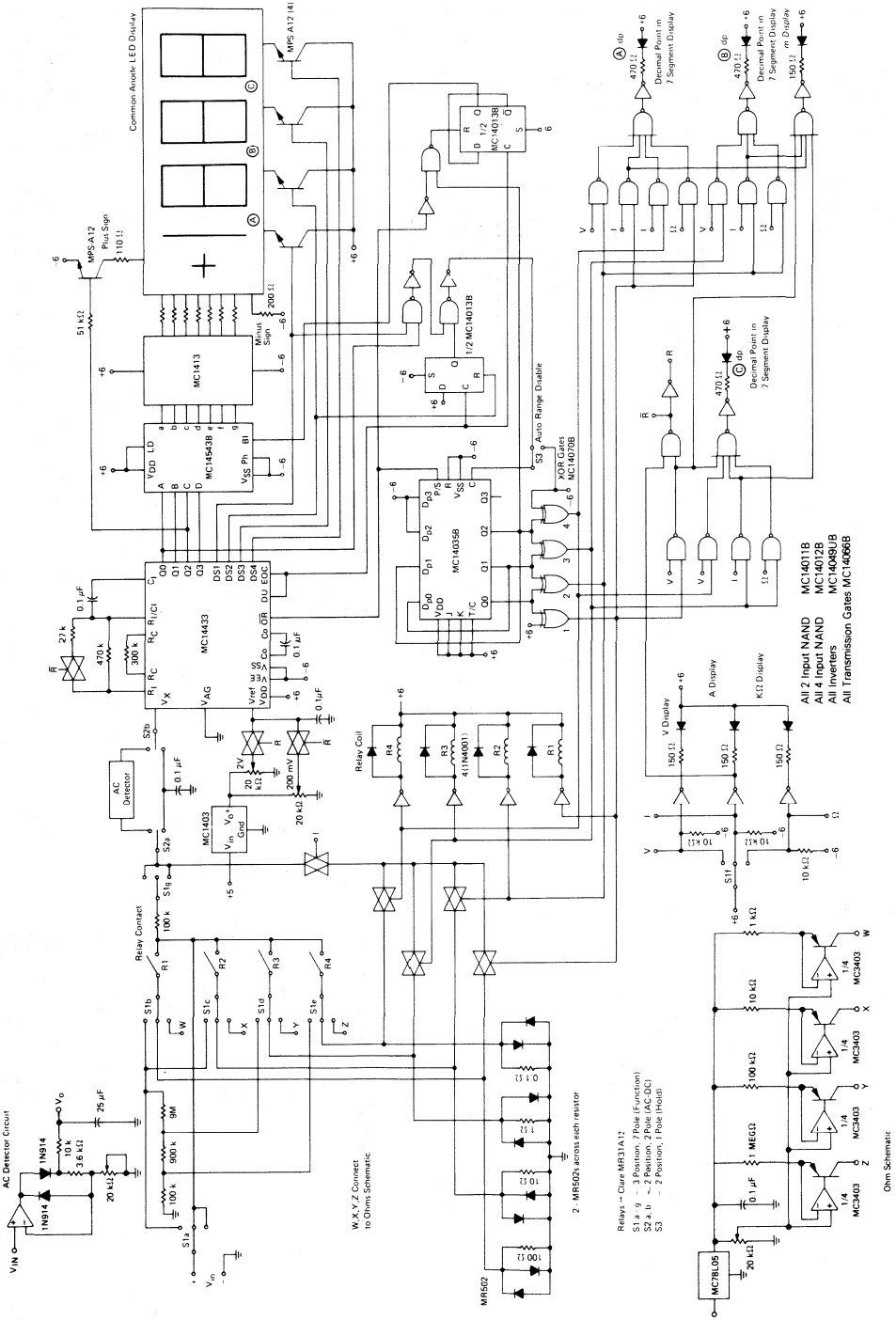


FIGURE 15 – 3½ DIGIT AUTORANGING MULTIMETER

3½ DIGIT AUTORANGING MULTIMETER

An autoranging multimeter including ac and dc voltage ranges from 200 mV to 200 V, ac and dc current from 2 mA to 2 A fullscale and resistance ranges from 2 kΩ to 2 MΩ fullscale is shown in Figure 15. In this multimeter only two input jacks are required for all ranges and functions, eliminating the need for changing leads on the instrument when changing ranges or functions. Although only four ranges are provided for each function, the technique used may be expanded to more ranges if desired. Range switching uses mechanical relays. However, the relays may be replaced with solid state analog switches.

The MC14433 provides the overrange and underrange control signals for the automatic ranging circuits.

PARALLEL BCD DATA OUTPUT CIRCUIT

The output of the MC14433 may be demultiplexed to produce parallel BCD data as shown in Figure 16. Two levels of latches are required for a complete demultiplexing of the data since the outputs of the MC14042B latches change sequentially with the DS1 to DS4 strobe pulses. To key output validity to one leading edge, i.e., that of the EOC signal of the MC14433, information is transferred to the second set of latches (MC14175B latches). A single set of latches can be used when reading of output is restricted to within 12,000 clock pulses after EOC. This requires synchronous system operation with respect to the BCD data bus.

In this system the output ground level is V_{SS}. In most cases, a two supply system with V_{SS} connected to V_{AG} is recommended. This allows connecting analog ground and digital ground together without destroying a power supply. This circuit works well with that of Figure 12.

FIGURE 16 — DEMULTIPLEXING FOR MC14433 BCD DATA

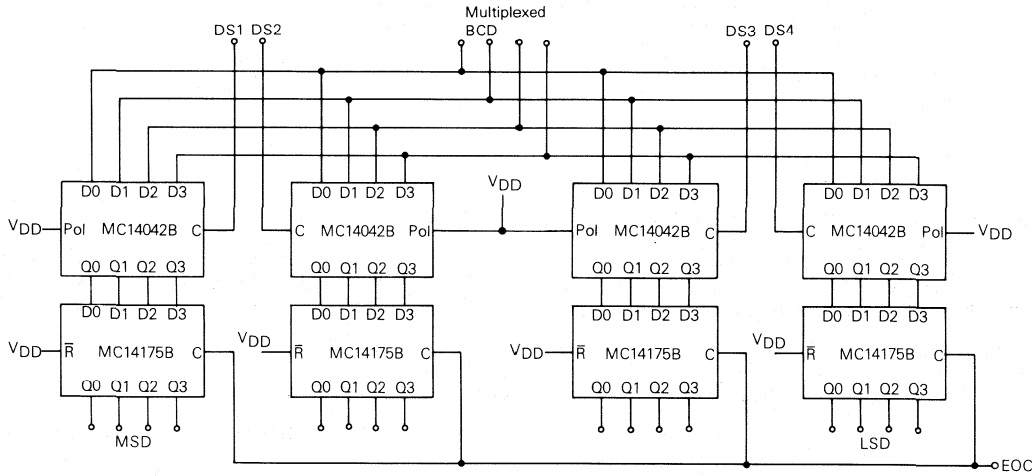
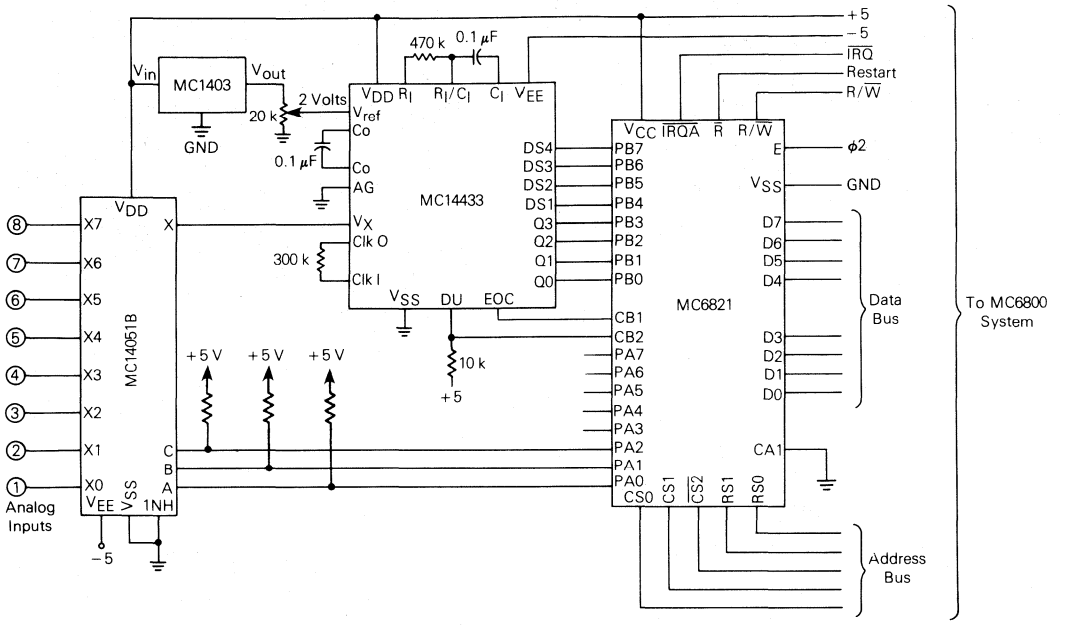


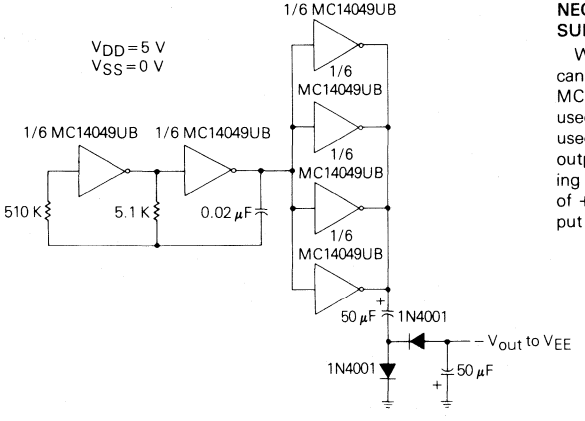
FIGURE 17 — CHANNEL DATA ACQUISITION HARDWARE



8 CHANNEL DATA ACQUISITION NETWORK

Figure 17 shows an 8-channel data acquisition network using the MC14433 and an MC6800 microprocessor system. The interface between the microprocessor data bus and the A/D system is done with an MC6821 PIA. One half of the PIA is used with the BCD and digit select outputs of the MC14433, while the second half of the PIA selects the channel to be measured via the MC14051B analog multiplexer. Control lines CB1 and CB2 are used for data flow control and are connected to DU and EOC of the MC14433.

FIGURE 18 — NEGATIVE SUPPLY GENERATED FROM POSITIVE SUPPLY



NEGATIVE SUPPLY GENERATED FROM POSITIVE SUPPLY

When only +5 V is available, a negative supply voltage can be generated with the circuit of Figure 18 using one MC14049UB. Two inverters from CMOS hex inverter are used as an oscillator (≈3 kHz) with the remaining inverters used as buffers for higher current output. The square wave output from the oscillator is level-translated to a negative going signal. This signal is rectified and filtered. A V_{DD} voltage of +5 V for the hex buffer will result in a −4.3 V no load output voltage while the output with a 2 mA load is ≈3.4 V.

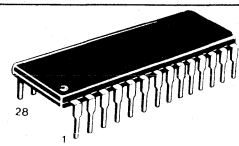
MC14442

CMOS LSI
(LOW-POWER SILICON GATE COMPLEMENTARY MOS)

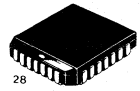
8-BIT A/D CONVERTER WITH PARALLEL INTERFACE

The MC14442 ADC is a 28-pin bus compatible 8-bit A/D converter with additional digital input capability. The device operates from a single 5 V supply and provides direct interface to the MPU data bus used with all Motorola M6800 family parts. It performs an 8-bit conversion in 32 machine cycles and allows up to 11 analog inputs. In addition, the part can accept up to 6 digital inputs. These inputs are designed to be either analog or digital inputs. All necessary logic for software configuration, channel selection, conversion control, and bus interface is included.

- Direct Interface to M6800 Family MPUs
- Dynamic Successive Approximation A/D
- 32 μs Conversion at $f_E = 1.0$ MHz
- Ratiometric Conversion
- Completely Programmable
- 5 Dedicated Analog Inputs
- 6 Inputs Usable for Either Analog or Digital Signals
- Completely TTL Compatible Inputs at Full Speed with Supply Voltage of 5 V ± 10%
- Monotonic Over Complete Input Range



P SUFFIX
PLASTIC DIP
CASE 710

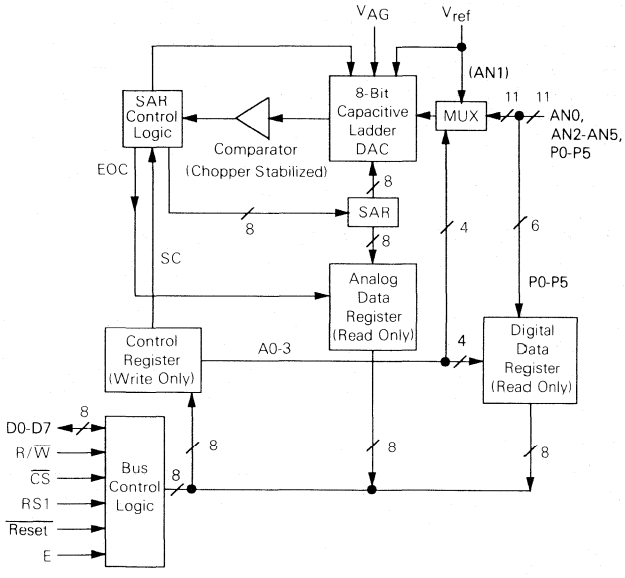


FN SUFFIX
PLCC
CASE 776

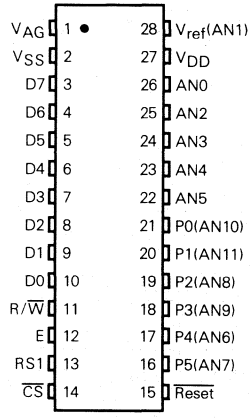
ORDERING INFORMATION

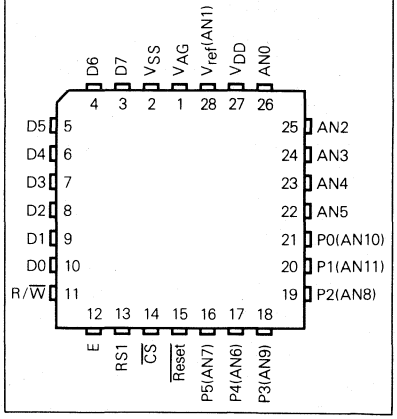
MC14442P	Plastic DIP
MC14442FN	PLCC

BLOCK DIAGRAM



PIN ASSIGNMENTS





MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage (Referenced to V_{SS})	−0.5 to +6.5	V
V_{in}	DC Input Voltage (Referenced to V_{SS})	−0.5 to V_{DD} +0.5	V
V_{out}	DC Output Voltage (Referenced to V_{SS})	−0.5 to V_{DD} +0.5	V
I_{in}	DC Input Current, per Pin	±10	mA
I_{out}	DC Output Current, per Pin	±10	mA
I_{DD}	DC Supply Current, V_{DD} and V_{SS} Pins	±20	mA
P_D	Power Dissipation, per Package	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 V ±10%, V_{SS} = 0 V, T_A = −40°C to 85°C unless otherwise noted)

Characteristic	Symbol	Conditions	Min	Max	Unit
Bus Control Inputs (R/$\overline{W}$, Enable, $\overline{Reset}$, RS1, $\overline{CS}$)					
Input High Voltage	V_{IH}		2.0	–	V
Input Low Voltage	V_{IL}		–	0.8	V
Input Leakage Current	I_{in}	V_{in} = 0 to 5.5 V	–	±1	μA
Data Bus (D0-D7)					
Input High Voltage	V_{IH}		2.0	–	V
Input Low Voltage	V_{IL}		–	0.8	V
Three-State (Off State) Input Leakage Current	I_{TSI}	V_{DD} = 5.5 V, $V_{SS} \le V_{in} \le V_{DD}$	–	±10	μA
Output High Voltage	V_{OH}	I_{OH} = −1.6 mA I_{OH} = −20 μA	2.4 V_{DD} − 0.1	– –	V
Output Low Voltage	V_{OL}	I_{OL} = 1.6 mA I_{OL} = 20 μA	– –	0.4 0.1	V
Peripheral Inputs (P0-P5)					
Input High Voltage	V_{IH}		2.0	–	V
Input Low Voltage	V_{IL}		–	0.8	V
Input Leakage Current	I_{in}	V_{DD} = 5.5 V, $V_{SS} \le V_{in} \le V_{DD}$	–	±1.0	μA
Current Requirements					
Supply Current	I_{DD}	V_{DD} = 5.5 V	–	10	mA
Input Current, V_{ref}	I_{ref}	V_{ref} = 4.5 to 5.5 V	–	800	μA

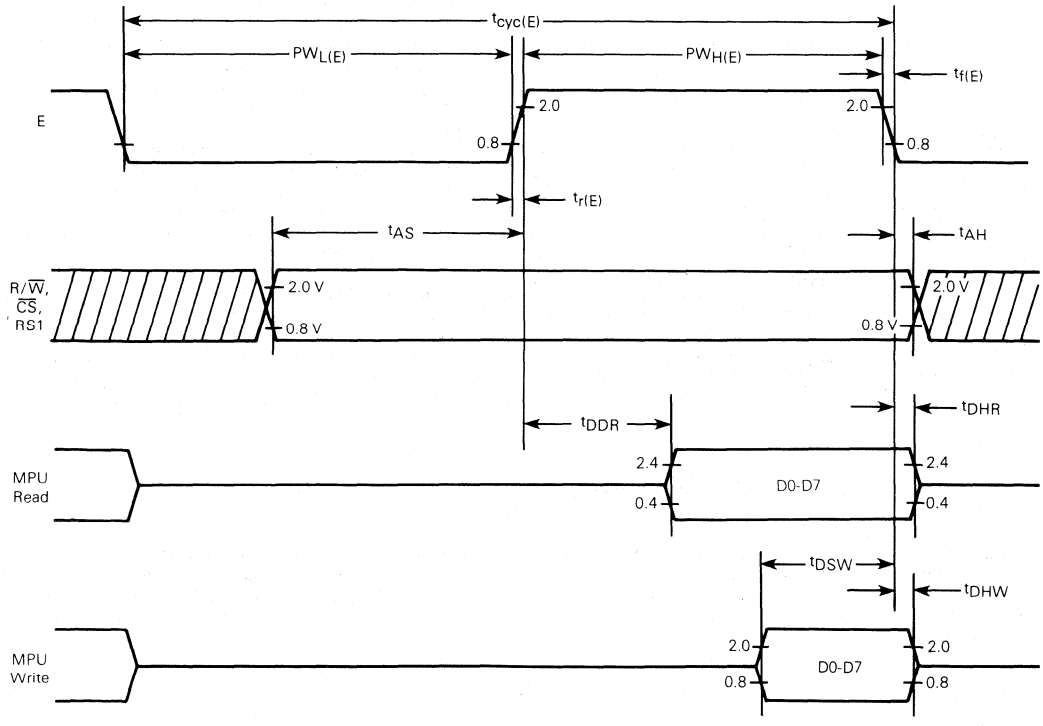
ANALOG CHARACTERISTICS (T_A = −40°C to 85°C)

Characteristic	Description	Min	Max	Unit
Analog Multiplexer				
Leakage Current	Leakage current between all deselected analog inputs and any selected analog input with all analog input voltages between V_{SS} and V_{DD}	–	±500	nA
A/D Converter (V_{SS} = 0 V, V_{AG} = 0 V, 4.5 V ≤ V_{ref} ≤ V_{DD} ≤ 5.5 V)				
Resolution	Number of bits resolved by the A/D	8	–	Bits
Nonlinearity	Maximum difference between an ideal and an actual ADC transfer function	–	± ½	LSB
Zero Error	Difference between the maximum input voltage of an ideal and an actual ADC for zero output code	–	± ½	LSB
Full-Scale Error	Difference between the minimum input voltage of an ideal and an actual ADC for full-scale output code	–	± ½	LSB
Total Unadjusted Error	Maximum sum of Nonlinearity, Zero Error, and Full-Scale Error	–	± ½	LSB
Quantization Error	Uncertainty due to converter resolution	–	± ½	LSB
Absolute Accuracy	Difference between the actual input voltage and the full-scale weighted equivalent of the binary output code, all error sources included	–	±1.0	LSB
Conversion Time	Total time to perform a single analog-to-digital conversion	–	32	E cycles
Sample Acquisition Time	Time required to sample the analog input	–	12	E cycles

AC CHARACTERISTICS ($T_A = -40°$ to $85°C$) (See Figure 1)

Characteristic	Signal	Symbol	Min	Max	Unit
Enable Clock Cycle Time ($1/f_E$)	E	$t_{cyc(E)}$	943	–	ns
Enable Clock Pulse Width, High	E	$PW_{H(E)}$	440	–	ns
Enable Clock Pulse Width, Low	E	$PW_{L(E)}$	410	–	ns
Clock Rise Time	E	$t_{r(E)}$	–	25	ns
Clock Fall Time	E	$t_{f(E)}$	–	30	ns
Address Setup Time	RS1, R/$\overline{W}$, $\overline{CS}$	t_{AS}	145	–	ns
Data Delay (Read)	D0-D7	t_{DDR}	–	335	ns
Data Setup (Write)	D0-D7	t_{DSW}	185	–	ns
Address Hold Time	RS1, R/$\overline{W}$, $\overline{CS}$	t_{AH}	10	–	ns
Input Data Hold Time	D0-D7	t_{DHW}	10	–	ns
Output Data Hold Time	D0-D7	t_{DHR}	10	–	ns
Input Capacitance	P0-P5, AN0-AN10	C_{in}	–	55	pF
	R/$\overline{W}$, E, RS1, $\overline{CS}$, $\overline{RESET}$		–	15	
Three-State Output Capacitance	D0-D7	C_{out}	–	15	pF

FIGURE 1 — BUS TIMING



PIN FUNCTIONS

Pin No.	Pin Name	Function	Type
1	V_{AG}	A/D Converter Analog Ground	Supply
2	V_{SS}	Digital Ground	Supply
3	D7	Data Bus Bit 7 (MSB)	Input/Output
4	D6	Data Bus Bit 6	Input/Output
5	D5	Data Bus Bit 5	Input/Output
6	D4	Data Bus Bit 4	Input/Output
7	D3	Data Bus Bit 3	Input/Output
8	D2	Data Bus Bit 2	Input/Output
9	D1	Data Bus Bit 1	Input/Output
10	D0	Data Bus Bit 0 (LSB)	Input/Output
11	R/$\overline{W}$	Read/Write	Input
12	E	Enable Clock (ϕ2)	Input
13	RS1	Register Select	Input
14	$\overline{CS}$	Chip Select	Input
15	$\overline{Reset}$	Reset	Input
16	P5(AN7)	Digital Port or Analog Channel 7	Input
17	P4(AN6)	Digital Port or Analog Channel 6	Input
18	P3(AN9)	Digital Port or Analog Channel 9	Input
19	P2(AN8)	Digital Port or Analog Channel 8	Input
20	P1(AN11)	Digital Port or Analog Channel 11	Input
21	P0(AN10)	Digital Port or Analog Channel 10	Input
22	AN5	Analog Channel 5	Input
23	AN4	Analog Channel 4	Input
24	AN3	Analog Channel 3	Input
25	AN2	Analog Channel 2	Input
26	AN0	Analog Channel 0	Input
27	V_{DD}	Supply Voltage	Supply
28	V_{ref} (AN1)	A/D Converter Positive Reference Voltage (Analog Channel 1)	Input

MC14442 MPU INTERFACE SIGNALS

Bidirectional Data Bus (D0-D7) – The bidirectional data lines D0-D7 comprise the bus over which data is transferred in parallel to and from the MPU. The data bus output drivers are three-state devices that remain in the high-impedence state except during an MPU read of an ADC data register.

Enable Clock (E) – The enable clock provides two functions for the MC14442. First, it serves to synchronize data transfers into and out of the ADC. The timing of all other external signals is referenced to the leading or trailing edge of the enable clock. Secondly, the enable clock is used internally to derive the necessary SAR A/D conversion clocks. Because this conversion is a dynamic process, enable clock must be a continuous signal into the ADC during an A/D conversion.

Read/Write (R/$\overline{W}$) – The R/$\overline{W}$ signal is provided to the MC14442 to control the direction of data transfers to and from the MPU. A low state on this line is required to transfer data from the MPU to the ADC control register. A high state is required on R/$\overline{W}$ to transfer data out of either of the ADC data registers.

Reset ($\overline{Reset}$) – The reset line supplies the means of externally forcing the MC14442 into a known state. When a low is applied to the $\overline{Reset}$ pin, the start conversion bit of the control register is cleared. Analog channel 0 is automatically selected by the analog multiplexer. The A/D status bit is also cleared. Any A/D results present in the Analog Data register are not affected by a reset. Reset forces the data bus output drivers to the high-impedance state. The internal byte pointer (discussed in the following pages) is set to point to the most significant byte of any subsequently selected internal register. In order to attain an internally stable reset state, the $\overline{Reset}$ pin must be low for at least one complete enable clock cycle.

Chip Select ($\overline{CS}$) – Chip select is an active low input used by the MPU system to enable the ADC for data transfers. No data may be passed to or from the ADC through the data bus pins unless $\overline{CS}$ is in a low state. A selection of MPU address lines and the M6800 VMA signal or its equivalent should be utilized to provide chip select to the MC14442.

MC14442 ANALOG INPUTS AND DIGITAL INPUTS
(Refer to the ADC Block Diagram)

Dedicated Analog Channels (AN0, AN2-AN5) – These input pins serve as dedicated analog channels subject to A/D conversions. These channels are fed directly into the internal 12-to-1 analog multiplexer which feeds a single analog voltage to the A/D converter.

Shared Analog Channels (AN6-AN11) – These input pins are also connected to the analog multiplexer and may be used as analog channels for A/D conversion. However, these pins may also serve as digital input pins as described next.

Shared Digital Inputs (P0-P5) – P0-P5 comprise a 6-bit digital input port whose bits may also serve as analog channels. The state of these inputs may be read at any time from the ADC digital data register. The function of these pins is not programmed, but instead is simply assigned by the system designer on a pin-by-pin basis.

CAUTION: Digital values read from the P0-P5 bit locations do not guarantee the presence of true digital input levels on these pins. P0-P5 pass through a TTL-compatible input buffer and into the digital data register. These buffers are designed with enough hysteresis to prevent internal oscillations if an analog voltage between 0.8 and 2 V is present on one or more of these six pins.

MC14442 SUPPLY VOLTAGE PINS

Positive Supply Voltage (V_{DD}) – V_{DD} is used internally to supply power to all digital logic and to the chopper stabilized comparator. Because the output buffers connected to this supply must drive capacitive loads, ac noise on this supply line is unavoidable internally. Analog circuits using this supply within the MC14442 were designed with high V_{DD} supply rejection; however, it is recommended that a filtering capacitance be used externally between V_{DD} and V_{SS} to filter noise caused by transient current spikes.

Ground Supply Voltage (V_{SS}) – V_{SS} should be tied to system digital ground or the negative terminal of the V_{DD} power source. Again, the output buffers cause internal noise on this supply, so analog circuits were designed with high V_{SS} rejection.

Positive A/D Reference Voltage (V_{ref}) – This is the voltage used internally to provide reference to the analog comparator and the digital-to-analog converter used by the SAR A/D. The analog-to-digital conversion result will be ratiometric to $V_{ref} - V_{AG}$ (full scale). Hence V_{ref} should be a very noise-free supply. Ideally V_{ref} should be single-point connected to the voltage supply driving the system's transducers. V_{ref} may be connected to V_{DD}, but degradation of absolute A/D accuracy may result due to switching noise on V_{DD}.

V_{ref} can be accessed via Analog Channel 1 (AN1).

A/D Ground Reference Voltage (V_{AG}) – This supply is the ground reference for the internal DAC and several reference voltages supplied to the comparator. It should also be noise-free to guarantee A/D accuracy. Absolute accuracy may be degraded if V_{AG} is wired to V_{SS} at the ADC package unless V_{SS} has been sufficiently filtered to remove switching noise. Ideally V_{AG} should be single-point grounded to the system analog ground supply.

MC14442 INTERNAL REGISTERS

The MC14442 ADC has three 16-bit internal registers. Each register is divided into two 8-bit bytes: a most significant (MS) byte (bits 8-15) and a least significant (LS) byte (bits 0-7). Each of these bytes may not be addressed externally, but instead are normally addressed by a single 16-bit instruction such as the M6800 LDX instruction. An internal byte pointer selects the appropriate register byte during the two E cycles of a normal 16-bit access. In keeping with the M6800 X register format, the pointer points first to the MS byte of any selected register. After the E cycle in which the MS byte is accessed, the pointer will switch to the LS byte and remain there for as long as chip select is low. The pointer moves back to the MS byte on the falling edge of E after the first complete E cycle in which the ADC is not selected. (See Figure 2a for more detail.) The MS byte of any register may also be accessed by a simple 8-bit instruction as shown in Figure 2b. However, the LS byte of all registers may be accessed only by 16-bit instructions as described above. By connecting the ADC register select (RS1) to the MPU address line A1, the three registers may be accessed sequentially by 16-bit operations.

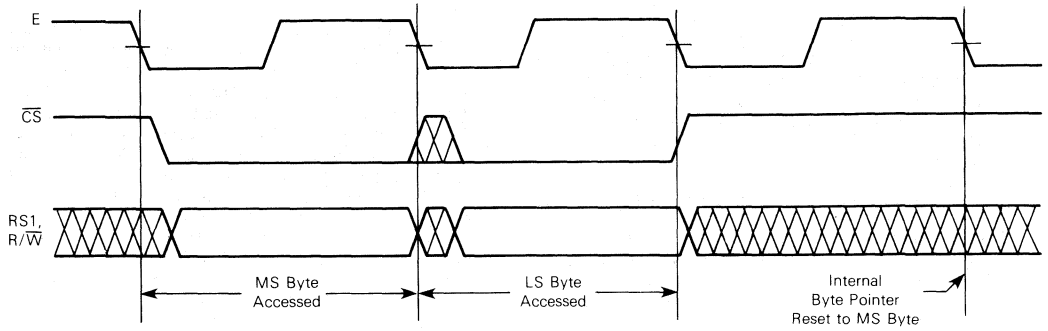
CAUTION: RS1 should **not** be connected to address line A0 and the addressing of the ADC should be such that RS1 does not change states during a 16-bit access.

INTERNAL REGISTER ADDRESSING

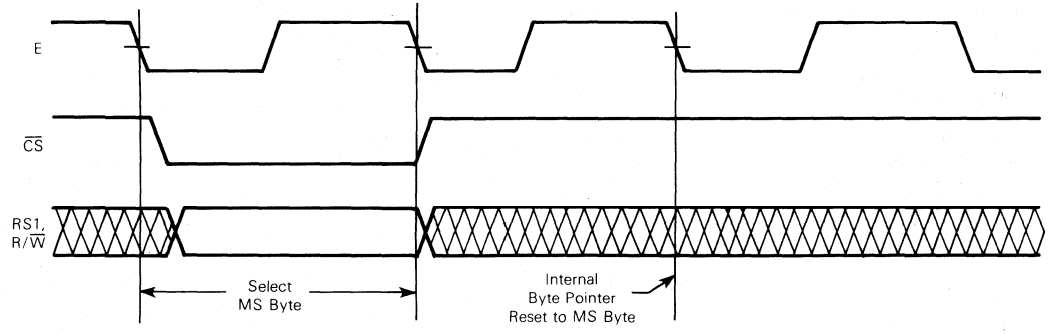
Addressing Signals				ADC Response
$\overline{Reset}$	$\overline{CS}$	R/$\overline{W}$	RS1	
0	X	X	X	Reset
1	0	0	0	No Response
1	0	0	1	MPU Write to Control Register
1	0	1	0	MPU Read from Analog Data Register
1	0	1	1	MPU Read from Digital Data Register
1	1	X	X	Chip Deselected (No Response)

FIGURE 2 — ADC ACCESS TIMING

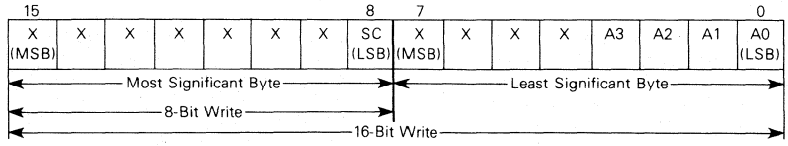
a — Typical 16-Bit ADC Access



b — Typical 8-Bit ADC Access



MC14442 CONTROL REGISTER
(Write Only)



Analog Multiplexer Address (A0-A3) – These four address bits are decoded by the analog multiplexer and used to select the appropriate analog channel as shown below.

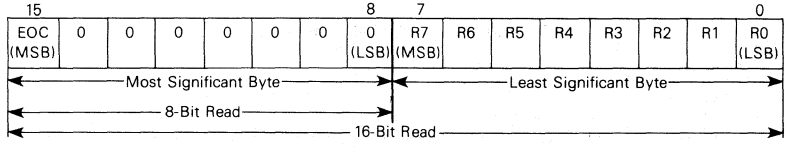
Hexadecimal Address (A3 = MSB)	Select
0	AN0
1	V_{ref}(AN1)
2-5	A2-AN5
6 or E	AN6
7 or F	AN7
8 or C	AN8
9 or D	AN9
A	AN10
B	AN11

Start A/D Conversion (SC) – When the SC bit is set to a logical 1, an A/D conversion on the specified analog channel will begin immediately after the completion of the control register write.

Unused Bits (X) – Bits 4-7 and 9-15 of the ADC Control Register are not used internally.

NOTE: A 16-bit control register write is required to change the analog multiplexer address. However, 8-bit writes to the MC14442 can be used to initiate an A/D conversion if the analog MUX is already selecting the desired channel. This is useful when repeated conversions on a particular analog channel are necessary.

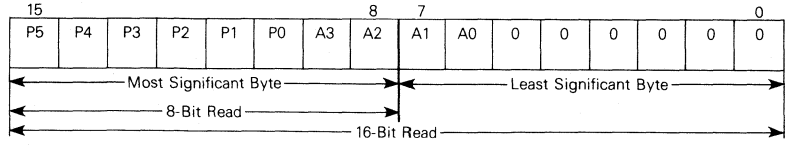
MC14442 ANALOG DATA REGISTER
(Read Only)



A/D Result (R0-R7) – The LS byte of the analog data register contains the result of the A/D conversion. R7 is the MSB, and the converter follows the standard convention of assigning a code of $FF to a full-scale analog voltage. There are no special overflow or underflow indications.

A/D Status (EOC) – The A/D status bit is set whenever a conversion is successfully completed by the ADC. The status bit is cleared by either an 8-bit or a 16-bit MPU write to the ADC control register. The remainder of the bits in the MS byte of the analog data register are always set to a logical 0 to simplify MPU interrogation of the ADC status. For example, a single M6800 TST instruction can be used to determine the status of the A/D conversion.

MC14442 DIGITAL DATA REGISTER
(Read Only)



Logical Zero (0) – These bits are always read as logical zero.

Analog Multiplexer Address (A0-A3) – The number of the analog channel presently addressed is given by these bits.

Shared Digital Port (P0-P5) – The voltage present on these pins is interpreted as a digital signal and the corresponding states are read from these bits.

WARNING: A digital value will be given for each pin even if some or all of the pins are being used as analog inputs.

ANALOG SUBSYSTEM
(See Block Diagram)

General Description

The analog subsystem of the MC14442 is composed of a 12-channel analog multiplexer, an 8-bit capacitive DAC (digital-to-analog converter), a chopper-stabilized comparator, a successive approximation register, and the necessary control logic to generate a successive approximation routine.

The analog multiplexer selects one of twelve channels and directs it to the input of the capacitive DAC. A fully-capacitive DAC is utilized because of the excellent matching characteristics of thin-oxide capacitors in the silicon-gate CMOS process. The DAC actually serves several functions. During the sample phase, the analog input voltage is applied to the DAC which acts as a sample-and-hold circuit. During the conversion phase, the capacitor array serves as a digital-to-analog converter. The comparator is the heart of the ADC; it compares the unknown analog input to the output of the DAC, which is driven by a conventional successive-approximation register. The chopper-stabilized comparator was designed for low offset voltage characteristics as well as V_{DD} and V_{SS} power supply rejection.

Device Operation

An A/D conversion is initiated by writing a logical 1 into the SC bit of the ADC control register. The MC14442 allows 2 enable clock cycles for the write into the control register even if only one byte is written. In this case, the second E cycle does not affect any internal registers. During the next 12½ enable cycles following a write command, the analog multiplexer channel is selected and the analog input voltage is stored on the sample and hold DAC. It is recommended that an input source impedance of 10 KΩ or less be used to allow complete charging of the capacitive DAC.

During cycle 13 the A/D is disconnected from the multiplexer output and the successive approximation A/D routine begins. Since the analog input voltage is being held on an internal capacitor for the entire conversion period, it is required that the enable clock run continuously until the A/D conversion is completed. The new 8-bit result is latched into the analog data register on the rising edge of cycle 32. At this point the end of conversion bit (EOC) is set in the analog data register MS byte. (See Figure 3, A/D Timing Sequence.)

NOTE: The digital data register or the analog data register may be read even if an A/D conversion is in progress. If the analog data register is read during an A/D conversion, valid results from the previous conversion are obtained. However, the EOC bit will be clear (logic 0) if an A/D conversion is in progress.

FIGURE 3 — A/D TIMING SEQUENCE

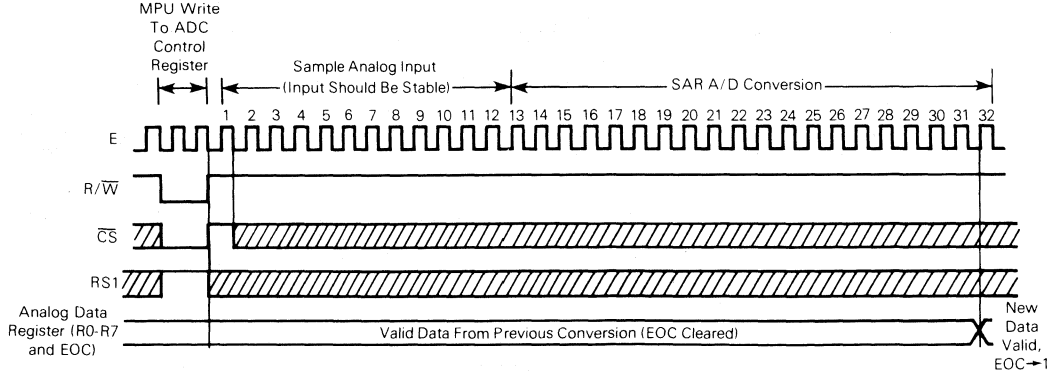
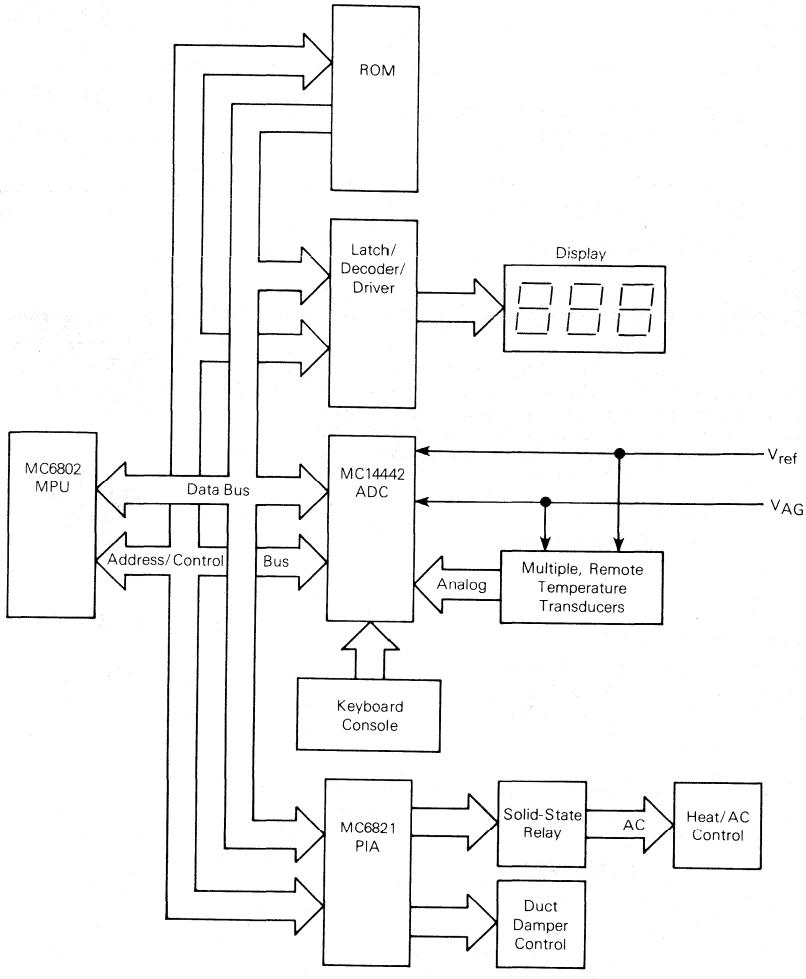


FIGURE 4 — TYPICAL MC14442 APPLICATION IN A CLIMATE CONTROLLER



MC14443
MC14447

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

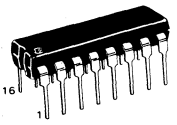
ANALOG-TO-DIGITAL CONVERTER LINEAR SUBSYSTEM

ANALOG-TO-DIGITAL CONVERTER LINEAR SUBSYSTEM

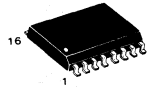
The MC14443 and the MC14447 are 6-channel, single-slope, 8-10 bit analog-to-digital converter linear subsystems for microprocessor-based data and control systems. Contained in both devices are a one-of-8 decoder, an 8-channel analog multiplexer, a buffer amplifier, a precision voltage-to-current converter, a ramp start circuit, and a comparator. The output driver of the MC14443's comparator is an open-drain N-channel which provides a sinking current. The output driver of the MC14447's comparator is a standard B-Series P-Channel, N-Channel pair.

A processor system (such as the MC68HC05 series) provides the addressing, timing, counting, and arithmetic operations required for implementing a full analog-to-digital converter system. A system made up of a processor and the linear subsystem has features such as automatic zeroing and variable scaling (weighting) of six separate analog channels.

- Quiescent Current 0.8 mA Typical at V_{DD} = 5 V
- Single Supply Operation +4.5 to +18 Volts
- Direct Interface to CMOS MPUs
- Typical Resolution — 8 Bits
- Typical Conversion Cycle as Fast as 300 μs
- Ratiometric Conversion Minimizes Error
- Analog Input Voltage Range: V_{SS} to V_{DD} — 2 V
- Chip Complexity: MC14443 — 150 FETs
  MC14447 — 151 FETs



P SUFFIX
PLASTIC DIP
CASE 648

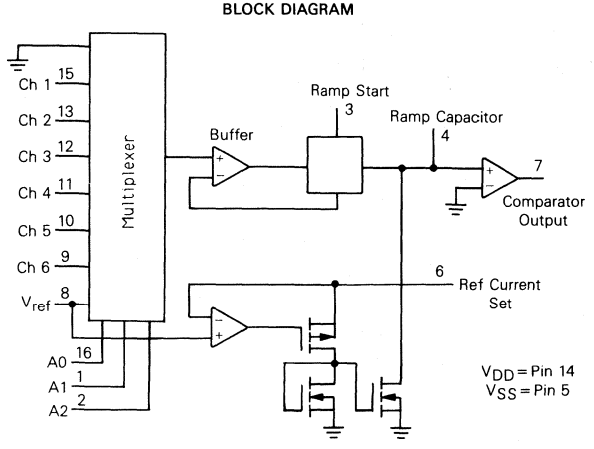


DW SUFFIX
SOG
CASE 751G

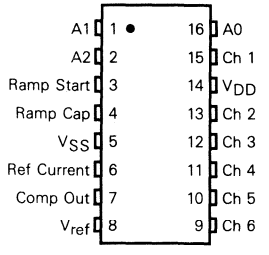
ORDERING INFORMATION

MC14443P, MC14447P	Plastic DIP
MC14443DW only	SOG Package

BLOCK DIAGRAM



PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	V
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD}+0.5	V
DC Input Current, per Pin	I_{in}	±10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS})

Characteristic	Symbol	V_{DD} V	−40°C Min	−40°C Max	25°C Min	25°C Typ #	25°C Max	85°C Min	85°C Max	Unit
Output Voltage—Comparator "0" Level	V_{OL}	5.0	–	0.05	–	0.01	0.05	–	0.05	V
V_{in} @ Pin 4 = 0 V		10	–	0.05	–	0.01	0.05	–	0.05	
		15	–	0.05	–	0.01	0.05	–	0.05	
V_{in} @ Pin 4 = 1.0 V "1" Level	V_{OH}	5.0	4.95	–	4.95	4.99	–	4.95	–	V
(R_{pullup} = 10 kΩ, MC14443 only)		10	9.95	–	9.95	9.99	–	9.95	–	
		15	14.95	–	14.95	14.99	–	14.95	–	
Input Voltage-Address, Ramp Start "0" Level	V_{IL}									V
(V_O = 4.5 or 0.5 V)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 V)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 V)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									V
(V_O = 0.5 or 4.5 V)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 V)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 V)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current—Comparator	I_{OH}									mA
V_{in} @ Pin 4 = 1.0 V (MC14447 only)										
(V_{OH} = 2.5 V)		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 V)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 V)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 V)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
V_{in} @ Pin 4 = 0 V	I_{OL}									mA
(V_{OL} = 0.4 V)		5.0	0.52	–	0.44	0.88	–	0.36	–	
(V_{OL} = 0.5 V)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 V)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current—Address, Ramp Start	I_{in}	15	–	±0.3	–	–	±0.3	–	±1.0	μA
Input Current—Analog Inputs	I_{in}	15	–	–	–	±0.1	±50	–	–	nA
Input Capacitance—Address, Ramp Start	C_{in}	15	–	–	–	5.0	7.5	–	–	pF
V_{in} = 0 V										
Quiescent Current	I_{DD}	5	–	–	–	0.8	1.5	–	–	mA
		10	–	–	–	1.5	–	–	–	
		15	–	–	–	1.7	3.0	–	–	
Crosstalk Between Any Two Input Channels	V_{Cr}	–	–	–	–	0	4.0	–	–	mV
Reference Current Range	I_R	–	–	–	10	–	50	–	–	μA
Channel Input Voltage Range	V_{AI}	5	–	–	0	–	3.0	–	–	V
		10	–	–	0	–	8.0	–	–	
		15	–	–	0	–	13.0	–	–	
Buffer Amplifier Output Offset	V_{BO}	5	–	–	–	0.285	–	–	–	V
		10	–	–	–	0.400	–	–	–	
		15	–	–	–	0.420	–	–	–	
Comparator Threshold	V_{TC}	5	–	–	0	0.195	V_{BO}	–	–	V
		10	–	–	0	0.275	V_{BO}	–	–	
		15	–	–	0	0.290	V_{BO}	–	–	
Reference Voltage Range	V_{ref}	5	–	–	2.0	–	3.0	–	–	V
		10	–	–	2.0	–	8.0	–	–	
		15	–	–	2.0	–	13.0	–	–	
Conversion Linearity	L_C									% Full
C > 100 pF, V_{AI} = 0 to 2.5 V, V_{ref} = 2.5 V		5	–	–	−0.5	–	+0.5	–	–	Scale
V_{AI} = 0 to 7.0 V, V_{ref} = 7.0 V		10	–	–	−0.5	–	+0.5	–	–	
V_{AI} = 0 to 12.0 V, V_{ref} = 12.0 V		15	–	–	−0.5	–	+0.5	–	–	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

APPLICATION INFORMATION FOR 10-BIT RESOLUTION

DETERMINING R_{ref} AND C_{ramp}

The maximum time for the ramp capacitor to discharge from the largest voltage (V_{ref}) is equal to the time required to fill a 10-bit counter. An MPU such as the MC146805E2, running at 5 MHz, could fill the counter in about 1.8 ms; i.e.,

LOOP INC COUNT	3 cycles
TST PIA	3
BNZ LOOP	3
	9 cycles

$$t = 1024 \times 9 \text{ cycles} \times 200 \text{ ns/cycle} = 1.843 \text{ ms}$$

For $V_{DD} = 5$ V and $V_{ref} = 2.5$ V:

$C = I_R(t)/V_{ref}$ where I_R = reference current, t = time, V_{ref} = reference voltage

$C_{max} = (50\ \mu A)\ (1.843 \text{ ms})/2.5 \text{ V} = 0.037\ \mu F$

$C_{min} = (10\ \mu A)\ (1.843 \text{ ms})/2.5 \text{ V} = 0.0074\ \mu F$

Choose $C_{ramp} = 0.022\ \mu F$ with a reference current of 30 μA. Use a polystyrene capacitor.

$R_{ref} = (V_{DD} - V_{ref})/I_R = (5 - 2.5)/30 = 83\ k\Omega$

choose 82 kΩ for R_{ref}

DETERMINING THE TOTAL CONVERSION TIME

Mux prop delay, t_M	360 ns
Ramp start prop delay, t_{TS}	80 ns
Comparator prop delay, $t_{PLH/HL}$	1200 ns
Capacitor discharge time	1.843 ms
Capacitor charge time, use 150 μA for charging current	0.366 ms*
Approx. total time	2.2 ms

*Ramp start must be low at least 0.366 ms for this example.

ACQUIRING 10 BITS OF RESOLUTION

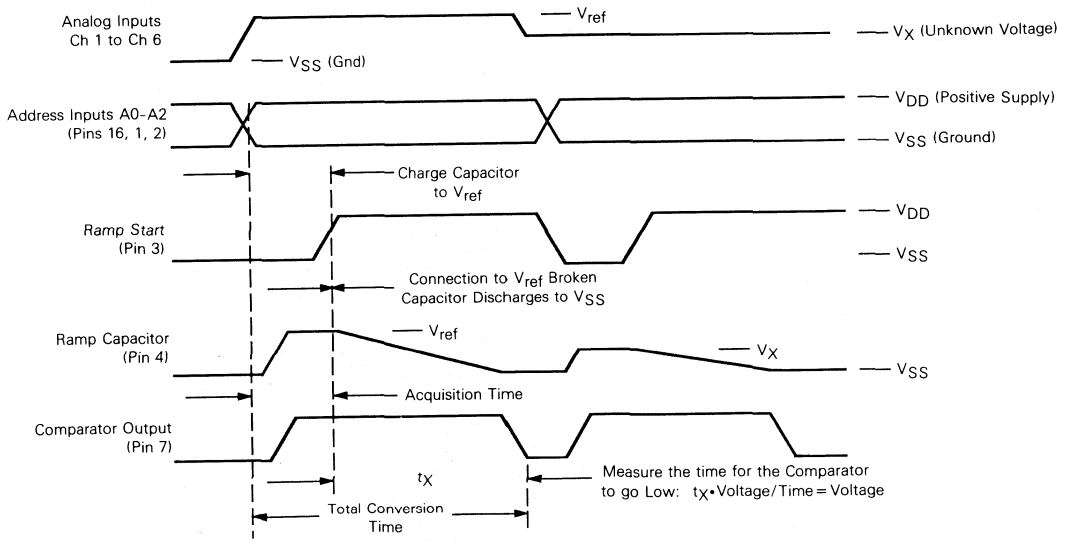
For 10 bits of resolution, the MPU must perform 2^{10} or 1024 counts during the longest A/D conversion discharge cycle. Therefore, 1.843 ms/1024 = 1.8 μs/bit. For ± 1 LSB of accuracy, the MPU must sample the signal at pin 7 every 1.8 μs; this is a sample rate of 555 ks/s.

For a 2.5 V reference, the resolution per bit is 2.5 V/1024 = 2.44 mV/bit. Therefore, the 2.5 V reference must have < 2.44 mV of noise.

If the MC14443/7 is maintained near 25°C, the nonlinearity is $\pm 0.5\%$ of the full scale reading.

A 0.1 μF shunting capacitor at the supply pins is recommended.

TIMING DIAGRAM



MC144110
MC144111

CMOS LSI
(LOW POWER COMPLEMENTARY MOS)

DIGITAL-TO-ANALOG CONVERTERS WITH SERIAL INTERFACE

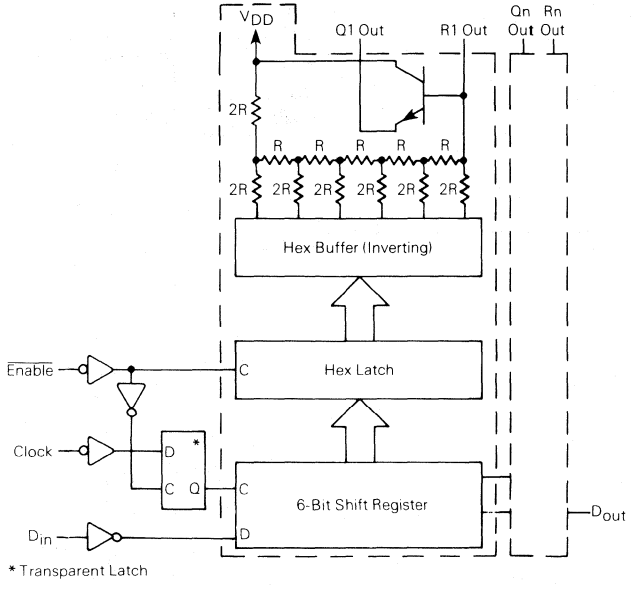
DIGITAL-TO-ANALOG CONVERTERS WITH SERIAL INTERFACE

The MC144110 and MC144111 are low-cost six-bit D/A converters with serial interface ports to provide communication with CMOS microprocessors and microcomputers. The MC144110 contains six static D/A converters; the MC144111 contains four converters.

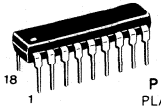
Due to a unique feature of these DACs, the user is permitted easy scaling of the analog outputs of a system. Over a 5 to 15 volt supply range, these DACs may be directly interfaced to CMOS MPUs operating at 5 volts.

- Direct R-2R Network Outputs
- Buffered Emitter-Follower Outputs
- Serial Data Input
- Digital Data Output Facilitates Cascading
- Direct Interface to CMOS μP
- Wide Operating Voltage Range: 4.5 to 15 Volts
- Wide Operating Temperature Range: 0 to 85°C
- Software Information is Contained in Document M68HC11RM/AD

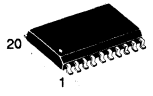
BLOCK DIAGRAM



MC144110

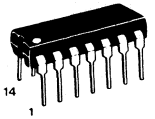


P SUFFIX
PLASTIC DIP
CASE 707

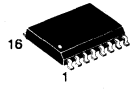


DW SUFFIX
SOG
CASE 751D

MC144111



P SUFFIX
PLASTIC DIP
CASE 646



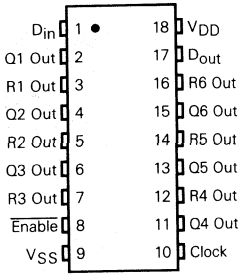
DW SUFFIX
SOG
CASE 751G

ORDERING INFORMATION

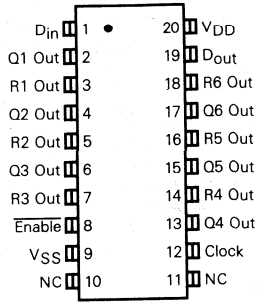
MC144110P	Plastic DIP
MC144110DW	SOG Package
MC144111P	Plastic DIP
MC144111DW	SOG Package

PIN ASSIGNMENTS

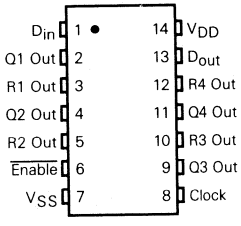
MC144110P



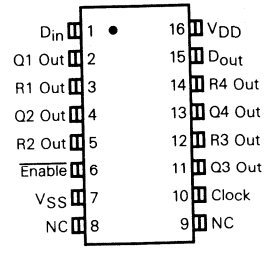
MC144110DW



MC144111P



MC144111DW



NC = No Connection

MAXIMUM RATINGS* (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	V
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD}+0.5	V
DC Input Current, per Pin	I	±10	mA
Power Dissipation (Per Output)	P_{OH}		mW
T_A=70°C, MC144110		30	
MC144111		50	
T_A=85°C, MC144110		10	
MC144111		20	
Power Dissipation (Per Package)	P_D		mW
T_A=70°C, MC144110		100	
MC144111		150	
T_A=85°C, MC144110		25	
MC144111		50	
Storage Temperature Range	T_{stg}	−65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation is is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

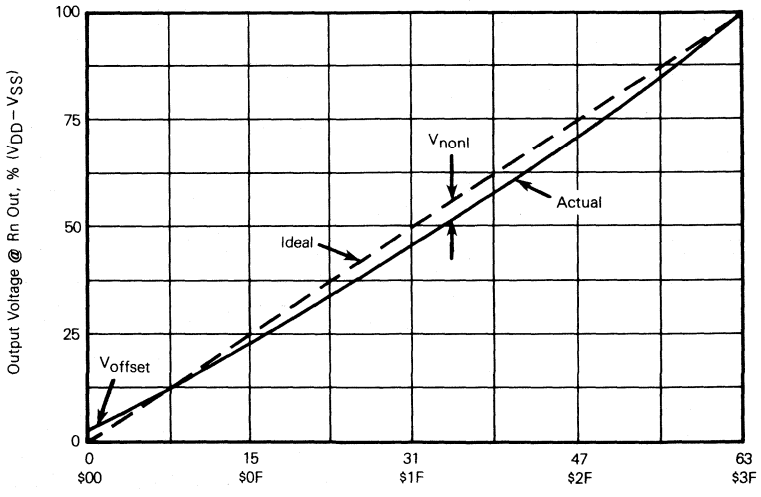
ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A=0° to 85°C unless otherwise indicated)

Symbol	Parameter	Test Conditions	V_{DD}	Min	Max	Unit
V_{IH}	High-Level Input Voltage (D_{in}, $\overline{Enable}$, Clock)		5	3.0	–	V
			10	3.5	–	
			15	4.0	–	
V_{IL}	Low-Level Input Voltage (D_{in}, $\overline{Enable}$, Clock)		5	–	0.8	V
			10	–	0.8	
			15	–	0.8	
I_{OH}	High-Level Output Current (D_{out})	$V_{out}=V_{DD}-0.5$ V	5	−200	–	μA
I_{OL}	Low-Level Output Current (D_{out})	V_{out}=0.5 V	5	200	–	μA
I_{DD}	Quiescent Supply Current	I_{out}=0 μA MC144110	15	–	12	mA
		MC144111	15	–	8	
I_{in}	Input Leakage Current (D_{in}, $\overline{Enable}$, Clock)	$V_{in}=V_{DD}$ or 0 V	15	–	±1	μA
V_{nonl}	Nonlinearity Voltage (Rn Out)	See Figure 1	5	–	100	mV
			10	–	200	
			15	–	300	
V_{step}	Step Size (Rn Out)	See Figure 2	5	19	137	mV
			10	39	274	
			15	58	411	
V_{offset}	Offset Voltage from V_{SS}	D_{in}=$00, See Figure 1	–	–	1	LSB
I_E	Emitter Leakage Current	$V_{Rn\ Out}$=0 V	15	–	10	μA
h_{FE}	DC Current Gain	I_E=0.1 to 10.0 mA, T_A=25°C	–	40	–	–
V_{BE}	Base-to-Emitter Voltage Drop	I_E=1.0 mA	–	0.4	0.7	V

SWITCHING CHARACTERISTICS (Voltages Referenced to V_{SS}, $T_A = 0$ to 85°C, $C_L = 50$ pF, Input $t_r = t_f = 20$ ns Unless Otherwise Indicated)

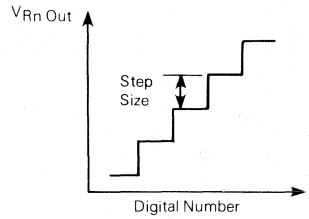
Symbol	Parameter	V_{DD}	Min	Max	Unit
t_{wH}	Positive Pulse Width, Clock (Figures 3 and 4)	5 10 15	2 1.5 1	– – –	µs
t_{wL}	Negative Pulse Width, Clock (Figures 3 and 4)	5 10 15	5 3.5 2	– – –	µs
t_{su}	Setup Time, $\overline{\text{Enable}}$ to Clock (Figures 3 and 4)	5 10 15	5 3.5 2	– – –	µs
t_{su}	Setup Time, D_{in} to Clock (Figures 3 and 4)	5 10 15	1000 750 500	– – –	ns
t_h	Hold Time, Clock to $\overline{\text{Enable}}$ (Figures 3 and 4)	5 10 15	5 3.5 2	– – –	µs
t_h	Hold Time, Clock to D_{in} (Figures 3 and 4)	5 10 15	5 3.5 2	– – –	µs
t_r, t_f	Input Rise and Fall Times	5-15	–	2	µs
C_{in}	Input Capacitance	5-15	–	7.5	pF

FIGURE 1 — D/A TRANSFER FUNCTION



LINEARITY ERROR (integral linearity). A measure of how straight a device's transfer function is, it indicates the worst-case deviation of linearity of the actual transfer function from the best-fit straight line. It is normally specified in parts of an LSB.

FIGURE 2 — DEFINITION OF STEP SIZE



$$\text{Step size} = \frac{V_{DD}}{64} \pm 0.75\frac{V_{DD}}{64}$$

(For any adjacent pair of digital numbers)

FIGURE 3 — SERIAL INPUT, POSITIVE CLOCK

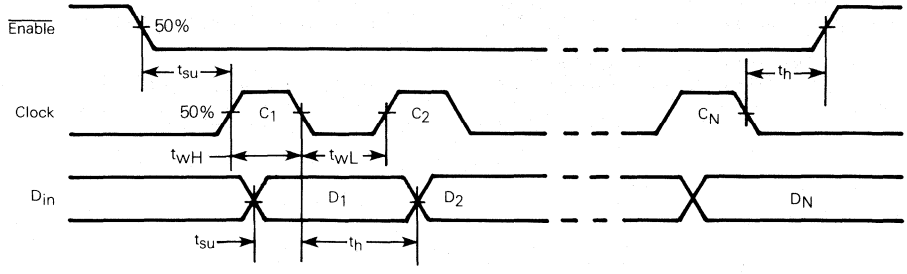
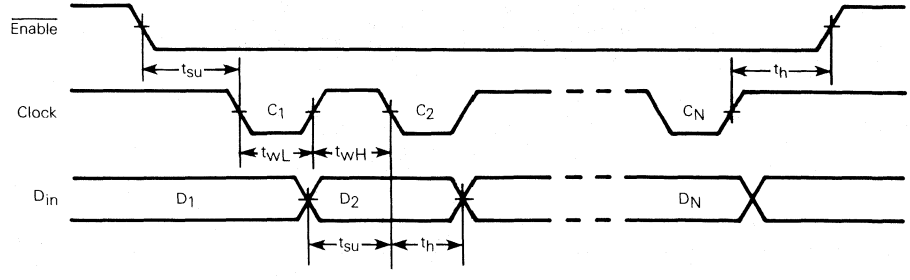


FIGURE 4 — SERIAL INPUT, NEGATIVE CLOCK



PIN DESCRIPTIONS

INPUTS

D_{in}, DATA INPUT — Six-bit words are entered serially, MSB first, into digital data input, D_{in}. Six words are loaded into the MC144110 during each D/A cycle; four words are loaded into the MC144111.

The last 6-bit word shifted in determines the output level of pins Q1 Out and R1 Out. The next-to-last 6-bit word affects pins Q2 Out and R2 Out, etc.

$\overline{\text{Enable}}$, NEGATIVE LOGIC ENABLE — The $\overline{\text{Enable}}$ pin must be low (active) during the serial load. On the low-to-high transition of $\overline{\text{Enable}}$, data contained in the shift register is loaded into the latch.

Clock, SHIFT REGISTER CLOCK — Data is shifted into the register on the high-to-low transition of Clock. Clock is fed into the D-input of a transparent latch, which is used for inhibiting the clocking of the shift register when $\overline{\text{Enable}}$ is high.

The number of Clock cycles required for the MC144110 is usually 36. The MC144111 usually uses 24 cycles. See Table 1 for additional information.

OUTPUTS

D_{out}, DATA OUTPUT — The digital data output is primarily used for cascading the DACs and may be fed into D_{in} of the next stage.

R1 Out through Rn Out, RESISTOR NETWORK OUTPUTS — These are the R-2R resistor network outputs. These outputs may be fed to high-impedance input FET op amps to bypass the on-chip bipolar transistors. The R value of the resistor network ranges from 7 to 15 kΩ.

Q1 Out through Qn Out, NPN TRANSISTOR OUTPUTS — Buffered DAC outputs utilize an emitter-follower configuration for current-gain, thereby allowing interface to low-impedance circuits.

SUPPLY PINS

V_{SS}, NEGATIVE SUPPLY VOLTAGE — This pin is usually ground.

V_{DD}, POSITIVE SUPPLY VOLTAGE — The voltage applied to this pin is used to scale the analog output swing from 4.5 to 15 volts, peak-to-peak.

TABLE 1 — NUMBER OF CHANNELS vs CLOCKS REQUIRED

Number of Channels Required	Number of Clock Cycles	Outputs Used on MC144110	Outputs Used on MC144111
1	6	Q1/R1	Q1/R1
2	12	Q1/R1, Q2/R2	Q1/R1, Q2/R2
3	18	Q1/R1, Q2/R2, Q3/R3	Q1/R1, Q2/R2, Q3/R3
4	24	Q1/R1, Q2/R2, Q3/R3, Q4/R4	Q1/R1, Q2/R2, Q3/R3, Q4/R4
5	30	Q1/R1, Q2/R2, Q3/R3, Q4/R4, Q5/R5	Not Applicable
6	36	Q1/R1, Q2/R2, Q3/R3, Q4/R4, Q5/R5, Q6/R6	Not Applicable

MC145040
MC145041

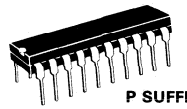
8-Bit A/D Converters With Serial Interface

CMOS

The MC145040 and MC145041 are low-cost 8-bit A/D Converters with serial interface ports to provide communication with microprocessors and microcomputers. The converters operate from a single power supply with a maximum nonlinearity of ± ½ LSB with a 5 V reference and ±1 LSB with a 2.5 V reference. No external trimming is required.

The MC145040 allows an external clock input (A/D CLK) to operate the dynamic A/D conversion sequence. The MC145041 has an internal clock and an end-of-conversion signal (EOC) is provided.

- Operating Supply Voltage Range: V_{DD} = 4.5 to 5.5 Volts
- Successive Approximation Conversion Time:
  MC145040 — 10 μs (with 2 MHz A/D CLK)
  MC145041 — 20 μs Maximum (Internal Clock)
- 11 Analog Input Channels with Internal Sample and Hold
- 0- to 5-Volt Analog Input Range with Single 5-Volt Supply
- Ratiometric Conversion
- Separate V_{ref} and V_{AG} Pins for Noise Immunity
- Monotonic Over Voltage and Temperature
- No External Trimming Required
- Direct Interface to Motorola SPI and National MICROWIRE Serial Data Ports
- TTL/NMOS-Compatible Inputs May Be Driven with CMOS
- Outputs are CMOS, NMOS, or TTL Compatible
- Very Low Reference Current Requirement
- Low Power Consumption: 11 mW
- Internal Test Mode for Self Test



P SUFFIX
PLASTIC DIP
CASE 738

DW SUFFIX
SOG
CASE 751D

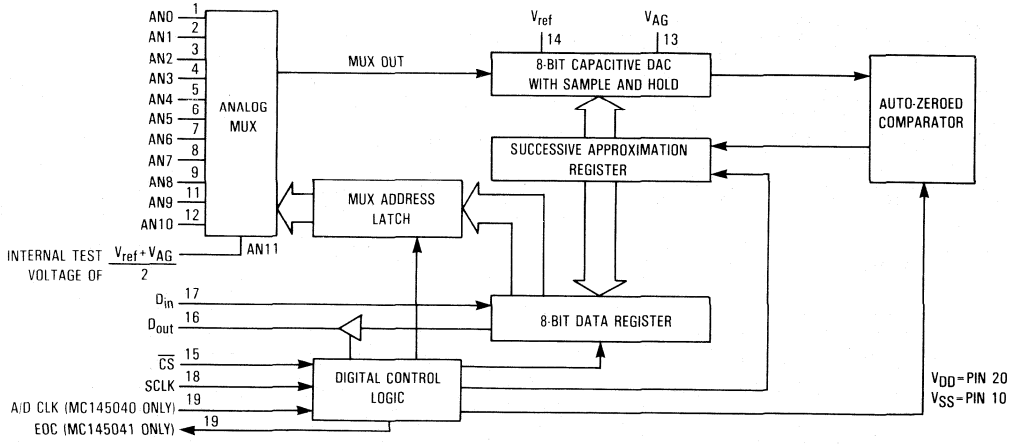
FN SUFFIX
PLCC
CASE 775

ORDERING INFORMATION

MC14XXXX_

Suffix	
1	−40 to 125°C
2	−40 to 85°C
P	Plastic DIP
DW	SOG
FN	PLCC

BLOCK DIAGRAM



MICROWIRE is a trademark of National Semiconductor.

MAXIMUM RATINGS* (For all product grades)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage (Referenced to V_{SS})	−0.5 to +7.0	V
V_{ref}	DC Reference Voltage	V_{AG} to V_{DD}+0.1	V
V_{AG}	Analog Ground	V_{SS}−0.1 to V_{ref}	V
V_{in}	DC Input Voltage, Any Analog or Digital Input	V_{SS}−1.5 to V_{DD}+1.5	V
V_{out}	DC Output Voltage	V_{SS}−0.5 to V_{DD}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{DD},I_{SS}	DC Supply Current, V_{DD} and V_{SS} Pins	±50	mA
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Operation Ranges below.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}.) Unused outputs must be left open.

OPERATION RANGES (Applicable to Guaranteed Limits for all product grades)

Symbol	Parameter	Suffix		Unit
		P1, DW1, FN1	P2, DW2, FN2	
V_{DD}	DC Supply Voltage (Referenced to V_{SS})	4.5 to 5.5	4.5 to 5.5	V
V_{ref}	DC Reference Voltage (Note 1)	V_{AG}+2.5 to V_{DD}	V_{AG}+2.5 to V_{DD}	V
V_{AG}	Analog Ground (Note 1)	V_{SS} to V_{ref}−2.5	V_{SS} to V_{ref}−2.5	V
V_{AI}	Analog Input Voltage (Note 2)	V_{AG} to V_{ref}	V_{AG} to V_{ref}	V
V_{in}, V_{out}	Digital Input Voltage, Output Voltage	V_{SS} to V_{DD}	V_{SS} to V_{DD}	V
T_A	Operating Temperature	−40 to +125	−40 to +85	°C

NOTES:
1. Reference voltages down to 1.0 V ($V_{ref}-V_{AG}$=1.0 V) are functional, but the A/D Converter Electrical Characteristics are not guaranteed.
2. $V_{SS} \le V_{AI} \le V_{AG}$ produces an output of $00 and $V_{ref} \le V_{AI} \le V_{DD}$ produces an output of $FF. See V_{AG} and V_{ref} pin descriptions.

DC ELECTRICAL CHARACTERISTICS
(Voltages Referenced to V_{SS}, Full Temperature and Voltage Ranges Per Operation Ranges Table)

Symbol	Parameter	Test Conditions	Guaranteed Limit	Unit
V_{IH}	Minimum High-Level Input Voltage (D_{in}, SCLK, $\overline{CS}$, A/D CLK)		2.0	V
V_{IL}	Maximum Low-Level Input Voltage (D_{in}, SCLK, $\overline{CS}$, A/D CLK)		0.8	V
V_{OH}	Minimum High-Level Output Voltage (D_{out}) (EOC) (D_{out}, EOC)	I_{out} = −200 μA I_{out} = −100 μA I_{out} = −20 μA	2.4 2.4 V_{DD}−0.1	V
V_{OL}	Maximum Low-Level Output Voltage (D_{out}) (EOC) (D_{out}, EOC)	I_{out} = +1.6 mA I_{out} = +1.0 mA I_{out} = 20 μA	0.4 0.4 0.1	V
I_{in}	Maximum Input Leakage Current (D_{in}, SCLK, $\overline{CS}$, A/D CLK)	V_{in} = V_{SS} or V_{DD}	±2.5	μA
I_{OZ}	Maximum Three-State Leakage Current (D_{out})	V_{out} = V_{SS} or V_{DD}	±10	μA
I_{DD}	Maximum Power Supply Current	V_{in} = V_{SS} or V_{DD}, All Outputs Open MC145040: A/D CLK = 2 MHz	2	mA
I_{ref}	Maximum Static Analog Reference Current (V_{ref})	V_{ref} = V_{DD} V_{AG} = V_{SS}	10	μA
I_{AI}	Maximum Analog Mux Input Leakage Current between all deselected inputs and any selected input. (AN0-AN10)	V_{AI} = V_{SS} to V_{DD}, P1, DW1, FN1 P2, DW2, FN2 Suffix	±1000 ±400	nA

A/D CONVERTER ELECTRICAL CHARACTERISTICS

(MC145040: 1 MHz ≤ A/D CLK ≤ 2 MHz, Full Temperature and Voltage Ranges Per Operaton Ranges Table)

Characteristics	Definition and Test Conditions	Guaranteed Limits: 2.5 V ≤ V_{ref} < 4.5 V*	Guaranteed Limits: 4.5 V ≤ V_{ref} ≤ 5.5 V*	Unit
Resolution	Number of bits resolved by the A/D converter	8	8	Bits
Maximum Nonlinearity	Maximum difference between an ideal and an actual ADC transfer function	±1	± ½	LSB
Maximum Zero Error	Difference between the maximum input voltage of an ideal and an actual ADC for zero output code	±1	± ½	LSB
Maximum Full-Scale Error	Difference between the minimum input voltage of an ideal and an actual ADC for full-scale output code	±1	± ½	LSB
Maximum Total Unadjusted Error	Maximum sum of Nonlinearity, Zero Error, and Full-Scale Error	±1	± ½	LSB
Maximum Quantization Error	Uncertainty due to converter resolution	± ½	± ½	LSB
Absolute Accuracy	Difference between the actual input voltage and the full-scale weighted equivalent of the binary output code, all error sources included	±1 ½	±1	LSB
Maximum Conversion Time	Total time to perform a single analog-to-digital conversion — MC145040	20	20	A/D CLK cycles
	MC145041	20	20	µs
Data Transfer Time	Total time to transfer digital serial data into and out of the device	8	8	SCLK cycles
Maximum Sample Acquisition Time	Analog input acquisition time window			µs
	MC145040: A/D CLK = 2 MHz, SCLK = 1 MHz	10	10	
	MC145041: SCLK = 1 MHz	16	16	
Minimum Total Cycle Time	Total time to transfer serial data, sample the analog input, and perform the conversion			µs
	MC145040: A/D CLK = 2 MHz, SCLK = 1 MHz	24	24	
	MC145041: SCLK = 1 MHz	40	40	
Maximum Sample Rate	Rate at Which Analog Inputs May be Sampled			ks/s
	MC145040: A/D CLK = 2 MHz, SCLK = 1 MHz	41	41	
	MC145041: SCLK = 1 MHz	25	25	

*V_{ref} referenced to V_{AG}.

AC ELECTRICAL CHARACTERISTICS ($t_r = t_f = 6$ ns, Full Temperature and Voltage Ranges Per Operation Ranges Table)

Figure	Symbol	Parameter		Guaranteed Limit	Unit
1	f	Maximum Clock Frequency (50% Duty Cycle), SCLK		1.1	MHz
1 (same as SCLK)	f	Clock Frequency (50% Duty Cycle), A/D CLK (MC145040)	Minimum	1.0	MHz
			Maximum	2.1	
1,7	t_{PLH}, t_{PHL}	Maximum Propagation Delay, SCLK to D_{out}		400	ns
1,7	t_h	Minimum Hold Time, SCLK to D_{out}		10	ns
2,7	t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, $\overline{CS}$ to D_{out}		150	ns
2,7	t_{PZL}, t_{PZH}	Maximum Propagation Delay, $\overline{CS}$ to D_{out}	MC145040	3 A/D CLK cycles	+ 400 ns
			MC145041	3.4	µs
3	t_{su}	Minimum Setup Time, D_{in} to SCLK		400	ns
3	t_h	Minimum Hold Time, SCLK to D_{in}		0	ns
4,7,8	t_d	Maximum Delay Time, EOC to D_{out} (MSB)	MC145041	400	ns
5	t_{su}	Minimum Setup Time, $\overline{CS}$ to SCLK	MC145040	3 A/D CLK cycles	+ 800 ns
			MC145041	3.8	µs
5	t_h	Minimum Hold Time, 8th SCLK to $\overline{CS}$		0	ns
6,8	t_{PHL}	Maximum Propagation Delay, 8th SCLK to EOC		500	ns
1	t_r, t_f	Maximum Input Rise and Fall Times, Any Digital Input		100	ns
1,4,6,7,8	t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output		300	ns
—	C_{in}	Maximum Input Capacitance	AN0-AN10	55	pF
			A/D CLK, SCLK, $\overline{CS}$, D_{in}	15	
—	C_{out}	Maximum Three-State Output Capacitance	D_{out}	15	pF

SWITCHING WAVEFORMS

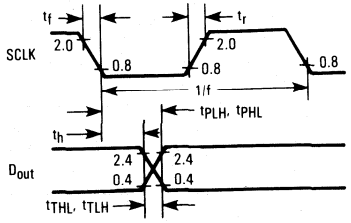


Figure 1

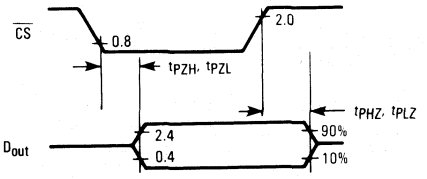


Figure 2

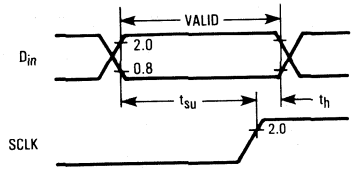


Figure 3

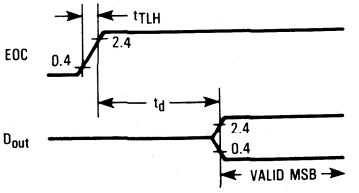


Figure 4

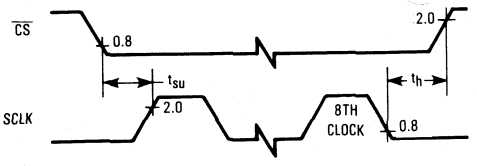


Figure 5

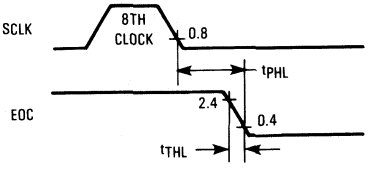


Figure 6

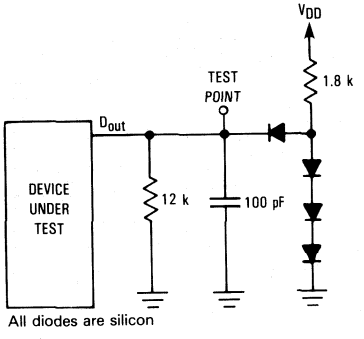


Figure 7. Test Circuit

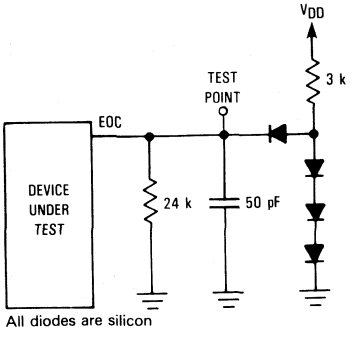


Figure 8. Test Circuit

PIN DESCRIPTIONS

DIGITAL INPUTS AND OUTPUTS

$\overline{CS}$ (Pin 15)

Active-low chip select input. $\overline{CS}$ provides three-state control of D_{out}. $\overline{CS}$ at a high logic level forces D_{out} to a high-impedance state. In addition, the device recognizes the falling edge of $\overline{CS}$ as a serial interface reset to provide synchronization between the MPU and the A/D converter's serial data stream. To prevent a spurious reset from occurring due to noise on the $\overline{CS}$ input, a delay circuit has been included such that a $\overline{CS}$ signal of duration $\leq$1 A/D CLK period (MC145040) or $\leq$500 ns (MC145041) is ignored. A valid $\overline{CS}$ signal is acknowledged when the duration is $\geq$3 A/D CLK periods (MC145040) or $\geq$3 μs (MC145041).

CAUTION

A reset aborts a conversion sequence, therefore high-to-low transitions on $\overline{CS}$ must be avoided during the conversion sequence.

D_{out} (Pin 16)

Serial data output of the A/D conversion result. The 8-bit serial data stream begins with the most significant bit and is shifted out on the high-to-low transition of SCLK. D_{out} is a three-state output as controlled by $\overline{CS}$. However, D_{out} is forced into a high-impedance state after the eighth SCLK, independent of the state of $\overline{CS}$. See Figures 9, 10, 11, or 12.

D_{in} (Pin 17)

Serial data input. The 4-bit serial data stream begins with the most significant address bit of the analog mux and is shifted in on the low-to-high transition of SCLK.

SCLK (Pin 18)

Serial data clock. The serial data register is completely static, allowing SCLK rates down to DC in a continuous or intermittent mode. SCLK need not be synchronous to the A/D CLK (MC145040) or the internal clock (MC145041). Eight SCLK cycles are required for each simultaneous data transfer, the low-to-high transition shifting in the new address and the high-to-low transition shifting out the previous conversion result. The address is acquired during the first four SCLK cycles, with the interval produced by the remaining four cycles being used to begin charging the on-chip sample-and-hold capacitors. After the eighth SCLK, the SCLK input is inhibited (on-chip) until the conversion is complete.

A/D CLK (Pin 19, MC145040 only)

A/D clock input. This pin clocks the dynamic A/D conversion sequence, and may be asynchronous and unrelated to SCLK. This signal must be free running, and may be obtained from the MPU system clock. Deviations from a 50% duty cycle can be tolerated if each half period is > 238 ns.

EOC (Pin 19, MC145041 only)

End-of-conversion output. EOC goes low on the negative edge of the eighth SCLK. The low-to-high transition of EOC indicates the A/D conversion is complete and the data is ready for transfer.

ANALOG INPUTS AND TEST MODE

AN0 through AN10 (Pins 1-9, 11, 12)

Analog multiplexer inputs. The input AN0 is addressed by loading $0 into the serial data input, D_{in}. AN1 is addressed by $1, AN2 by $2 . . . AN10 via $A. The mux features a break-before-make switching structure to minimize noise injection into the analog inputs. The source impedance driving these inputs must be $\leq$10 kΩ. NOTE: $B addresses an on-chip test voltage of $(V_{ref} + V_{AG})/2$, and produces an output of $80 if the converter is functioning properly. However, a $\pm$1 LSB deviation from $80 occurs in the presence of sufficient system noise (external to the chip) on V_{DD}, V_{SS}, V_{ref}, or V_{AG}.

POWER AND REFERENCE PINS

V_{SS} and V_{DD} (Pins 10 and 20)

Device supply pins. V_{SS} is normally connected to digital ground; V_{DD} is connected to a positive digital supply voltage. $V_{DD} - V_{SS}$ variations over the range of 4.5 to 5.5 volts do not affect the A/D accuracy. Excessive inductance in the V_{DD} or V_{SS} lines, as on automatic test equipment, may cause A/D offsets > ½ LSB.

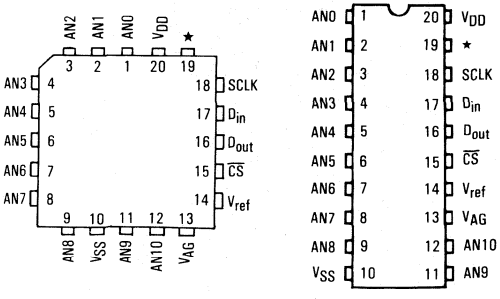
V_{AG} and V_{ref} (Pins 13 and 14)

Analog reference voltage pins which determine the lower and upper boundary of the A/D conversion. Analog input voltages $\geq V_{ref}$ produce an output of $FF and input voltages $\leq V_{AG}$ produce an output of $00. CAUTION: The analog input voltage must be $\geq V_{SS}$ and $\leq V_{DD}$. The A/D conversion result is ratiometric to $V_{ref} - V_{AG}$ as shown by the formula:

$$V_{in} = \left[\frac{\text{output code}}{\$FF} \times (V_{ref} - V_{AG})\right] + \underset{\text{error}}{\text{quantizing}} + \underset{\text{error}}{\text{linearity}}$$

V_{ref} and V_{AG} should be as noise-free as possible to avoid degradation of the A/D conversion. Noise on either of these pins will couple 1:1 to the analog input signal, i.e. a 20 mV change in V_{ref} can cause a 20 mV error in the conversion result. Ideally V_{ref} and V_{AG} should be single-point connected to the voltage supply driving the system's transducers.

PIN ASSIGNMENTS



★NOTE:
A/D CLK (MC145040)
EOC (MC145041)

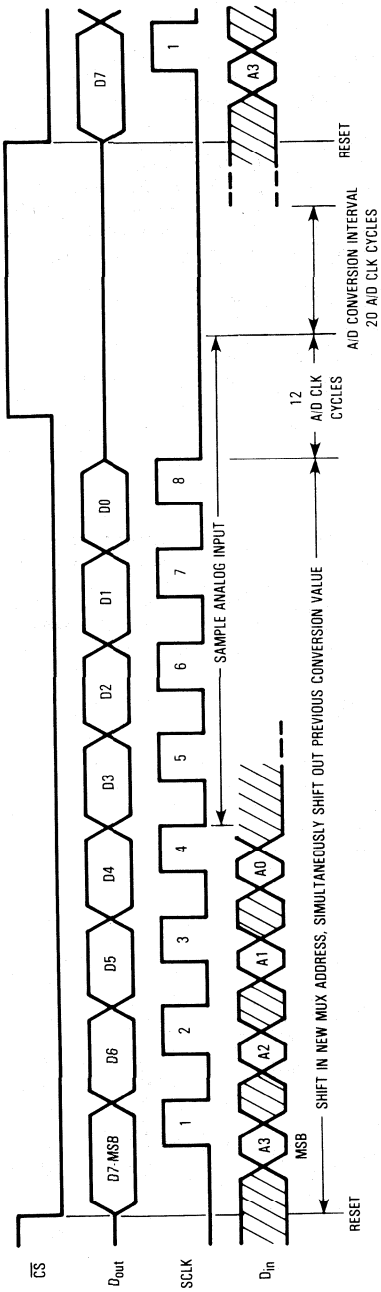


Figure 9. MC145040 Timing Diagram Utilizing $\overline{CS}$ to Three-State D_{out}

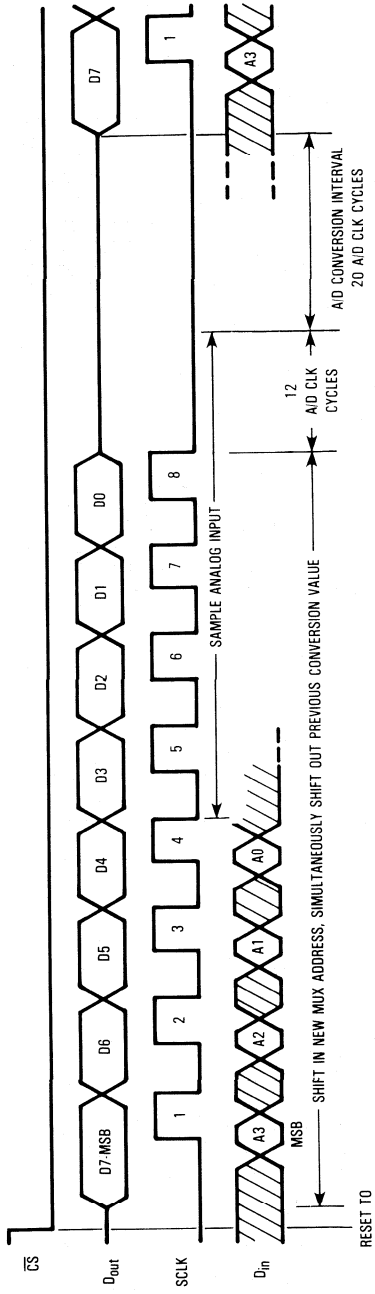


Figure 10. MC145040 Timing Diagram Not Utilizing $\overline{CS}$, A/D Conversion Interval Controls Three-State

NOTES:
D7, D6, D5 . . . D0 = The result of the previous A/D conversion.
A3, A2, A1, A0 = The mux address for the next A/D conversion.

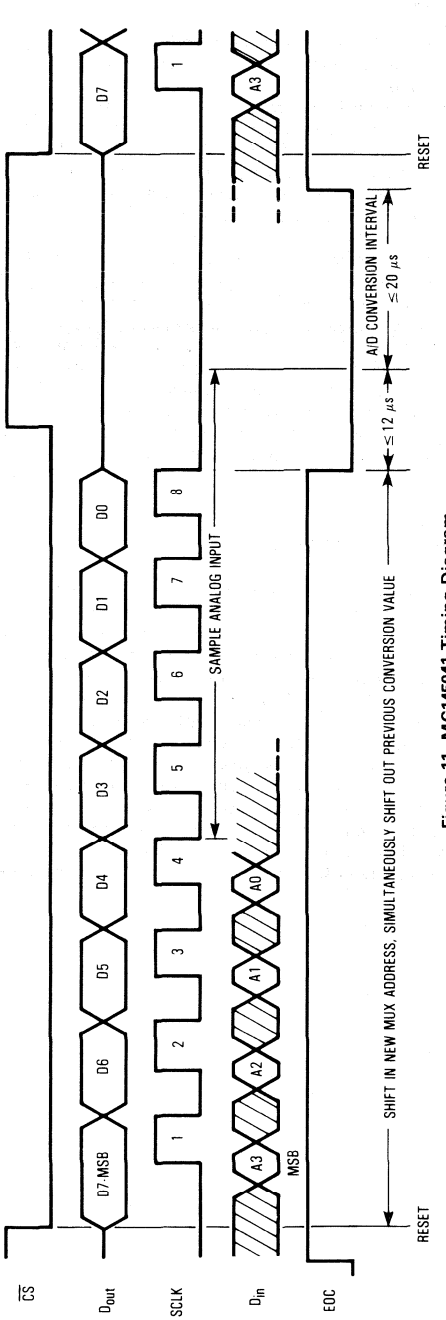


Figure 11. MC145041 Timing Diagram Utilizing $\overline{CS}$ to Three-State D_{out}

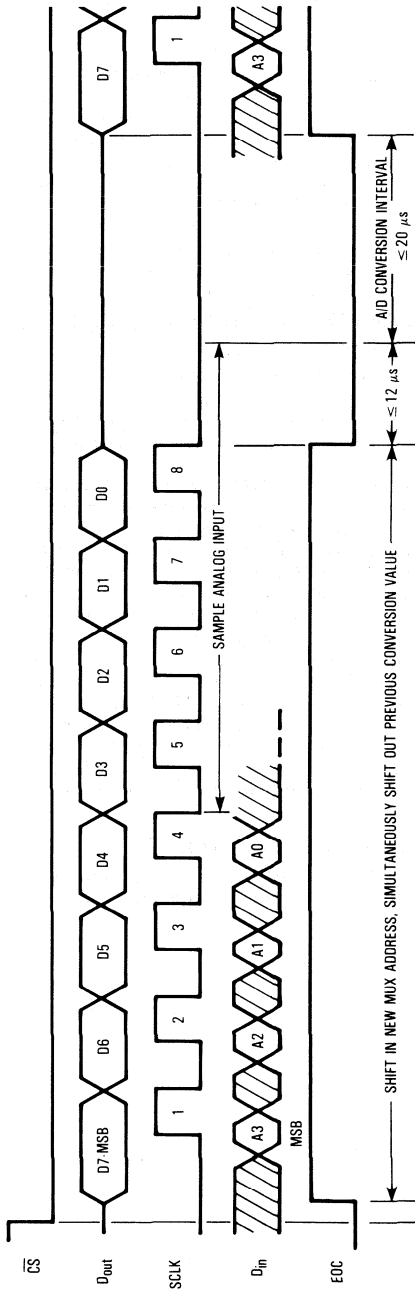


Figure 12. MC145041 Timing Diagram Not Utilizing $\overline{CS}$, A/D Conversion Interval Controls Three-State

NOTES:
D7, D6, D5 . . . D0 = The result of the previous A/D conversion.
A3, A2, A1, A0 = The mux address for the next A/D conversion.

MC145050
MC145051

Advance Information

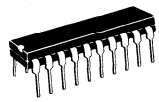
10-Bit A/D Converters with Serial Interface

CMOS

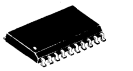
These ratiometric 10-bit ADCs have serial interface ports to provide communication with MCUs and MPUs. *Either a 10- or 16-bit format can be used.* The 16-bit format can be one continuous 16-bit stream or two intermittent 8-bit streams. The converters operate from a single power supply with no external trimming required. Reference voltages down to 2.5 V are accommodated.

The MC145050 has the same pin out as the 8-bit MC145040 which allows an external clock (ADCLK) to operate the dynamic A/D conversion sequence. The MC145051 has the same pin out as the 8-bit MC145041 which has an internal clock oscillator and an end-of-conversion (EOC) output.

- 11 Analog Input Channels with Internal Sample-and-Hold
- Operating Temperature Range: −40° to 125°C
- Successive Approximation Conversion Time:
  MC145050—21 μs (with 2.1 MHz ADCLK)
  MC145051—88 μs Maximum
- Maximum Sample Rate:
  MC145050—38 ks/s
  MC145051—10.7 ks/s
- Analog Input Range with 5-Volt Supply: 0 to 5 V
- Monotonic with No Missing Codes
- Direct Interface to Motorola SPI and National MICROWIRE Serial Data Ports
- Digital Inputs/Outputs are TTL, NMOS, and CMOS Compatible
- Low Power Consumption: 14 mW
- Chip Complexity: 1630 Elements (FETs, Capacitors, etc.)



P SUFFIX
PLASTIC
CASE 738

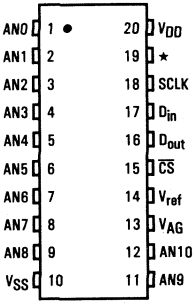


DW SUFFIX
SOG
CASE 751D

ORDERING INFORMATION

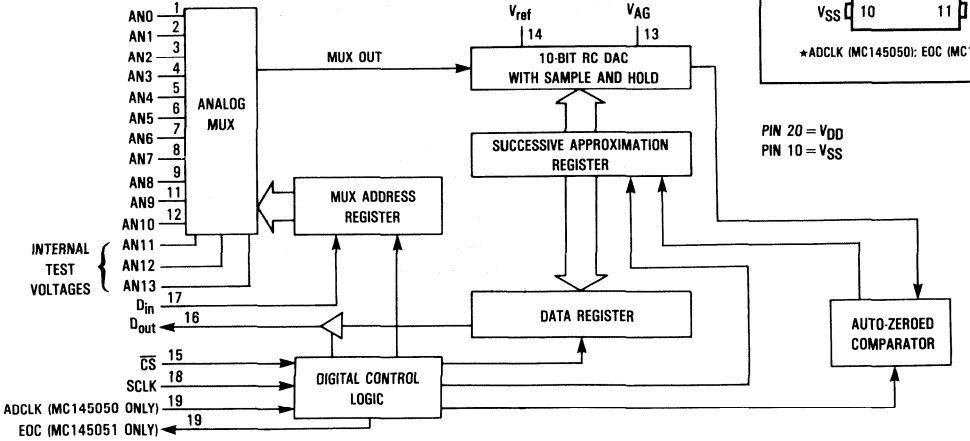
MC14505xP	Plastic DIP
MC14505xDW	SOG Package

PIN ASSIGNMENT



★ADCLK (MC145050); EOC (MC145051)

BLOCK DIAGRAM



PIN 20 = V_{DD}
PIN 10 = V_{SS}

MICROWIRE is a trademark of National Semiconductor Corp.
This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage (Referenced to V_{SS})	−0.5 to +6.0	V
V_{ref}	DC Reference Voltage	V_{AG} to V_{DD}+0.1	V
V_{AG}	Analog Ground	V_{SS}−0.1 to V_{ref}	V
V_{in}	DC Input Voltage, Any Analog or Digital Input	V_{SS}−0.5 to V_{DD}+0.5	V
V_{out}	DC Output Voltage	V_{SS}−0.5 to V_{DD}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{DD}, I_{SS}	DC Supply Current, V_{DD} and V_{SS} Pins	±50	mA
T_{stg}	Storage Temperature	−65 to 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Operation Ranges below.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

OPERATION RANGES (Applicable to Guaranteed Limits)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage, Referenced to V_{SS}	4.5 to 5.5	V
V_{ref}	DC Reference Voltage (Note 1)	V_{AG}+2.5 to V_{DD}+0.1	V
V_{AG}	Analog Ground (Note 1)	V_{SS}−0.1 to V_{ref}−2.5	V
V_{AI}	Analog Input Voltage (Note 2)	V_{AG} to V_{ref}	V
V_{in}, V_{out}	Digital Input Voltage, Output Voltage	V_{SS} to V_{DD}	V
T_A	Ambient Operating Temperature	−40 to 125	°C

NOTES:
1. Reference voltages down to 1.0 V ($V_{ref} - V_{AG} = 1.0$ V) are functional, but the A/D converter electrical characteristics are not guaranteed.
2. Analog input voltages greater than V_{ref} convert to full scale. Input voltages less than V_{AG} convert to zero. See V_{ref} and V_{AG} pin descriptions.

DC ELECTRICAL CHARACTERISTICS

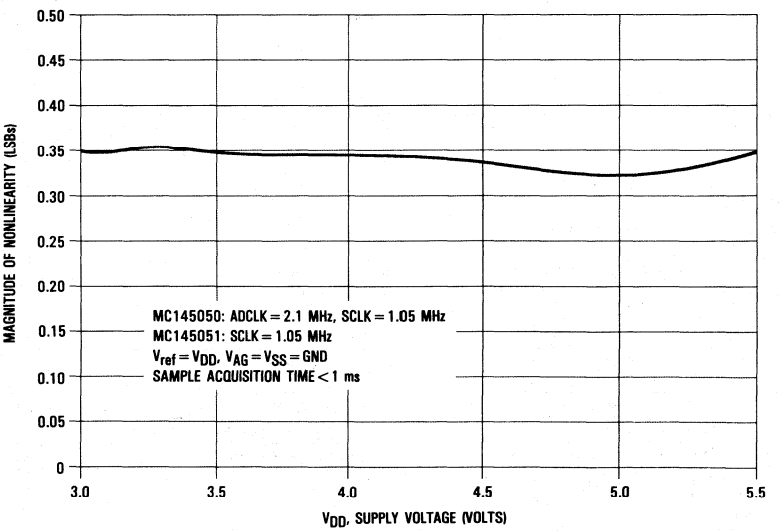
(Voltages Referenced to V_{SS}, Full Temperature and Voltage Ranges per Operation Ranges table, unless otherwise indicated)

Symbol	Parameter	Test Conditions	Guaranteed Limit	Unit
V_{IH}	Minimum High-Level Input Voltage (D_{in}, SCLK, $\overline{CS}$, ADCLK)		2.0	V
V_{IL}	Maximum Low-Level Input Voltage (D_{in}, SCLK, $\overline{CS}$, ADCLK)		0.8	V
V_{OH}	Minimum High-Level Output Voltage (D_{out}, EOC)	I_{out} = −1.6 mA I_{out} = −20 μA	2.4 V_{DD}−0.1	V
V_{OL}	Maximum Low-Level Output Voltage (D_{out}, EOC)	I_{out} = +1.6 mA I_{out} = 20 μA	0.4 0.1	V
I_{in}	Maximum Input Leakage Current (D_{in}, SCLK, $\overline{CS}$, ADCLK)	$V_{in} = V_{SS}$ or V_{DD}	±2.5	μA
I_{OZ}	Maximum Three-State Leakage Current (D_{out})	$V_{out} = V_{SS}$ or V_{DD}	±10	μA
I_{DD}	Maximum Power Supply Current	$V_{in} = V_{SS}$ or V_{DD}, All Outputs Open	2.5	mA
I_{ref}	Maximum Static Analog Reference Current (V_{ref})	$V_{ref} = V_{DD}$, $V_{AG} = V_{SS}$	100	μA
I_{AI}	Maximum Analog Mux Input Leakage Current between all deselected inputs and any selected input (AN0-AN10)	$V_{AI} = V_{SS}$ to V_{DD}	±1	μA

A/D CONVERTER ELECTRICAL CHARACTERISTICS

(Full Temperature and Voltage Ranges per Operation Ranges table; MC145050: 500 kHz ≤ ADCLK ≤ 2.1 MHz unless otherwise noted.)

Characteristic	Definition and Test Conditions	Guaranteed Limit	Unit
Resolution	Number of bits resolved by the A/D converter	10	Bits
Maximum Nonlinearity	Maximum difference between an ideal and an actual ADC transfer function	±1	LSB
Maximum Zero Error	Difference between the maximum input voltage of an ideal and an actual ADC for zero output code	±1	LSB
Maximum Full-Scale Error	Difference between the minimum input voltage of an ideal and an actual ADC for full-scale output code	±1	LSB
Maximum Total Unadjusted Error	Maximum sum of nonlinearity, zero error, and full-scale error	±1	LSB
Maximum Quantization Error	Uncertainty due to converter resolution	±1/2	LSB
Absolute Accuracy	Difference between the actual input voltage and the full-scale weighted equivalent of the binary output code, all error sources included	±1-1/2	LSB
Maximum Conversion Time	Total time to perform a single analog-to-digital conversion MC145050 MC145051	44 88	ADCLK cycles μs
Data Transfer Time	Total time to transfer digital serial data into and out of the device	10 to 16	SCLK cycles
Sample Acquisition Time	Analog input acquisition time window	6	SCLK cycles
Minimum Total Cycle Time	Total time to transfer serial data, sample the analog input, and perform the conversion MC145050: ADCLK = 2.1 MHz, SCLK = 2.1 MHz MC145051: SCLK = 2.1 MHz	 26 93	μs
Maximum Sample Rate	Rate at which analog inputs may be sampled MC145050: ADCLK = 2.1 MHz, SCLK = 2.1 MHz MC145051: SCLK = 2.1 MHz	 38 10.7	ks/s



NOTE: This "typical" graph is not to be used for design purposes but is intended as an indication of the IC's potential performance.

Graph 1. Typical Nonlinearity vs Supply Voltage

AC ELECTRICAL CHARACTERISTICS

(Full Temperature and Voltage Ranges per Operation Ranges table)

Figure	Symbol	Parameter		Guaranteed Limit	Unit
1	f	Clock Frequency, SCLK Note: Refer to t_{wH}, t_{wL} below	(10-bit xfer) Min (11- to 16-bit xfer) Min (10- to 16-bit xfer) Max	0 Note 1 2.1	MHz
1	f	Clock Frequency, ADCLK Note: Refer to t_{wH}, t_{wL} below	Minimum Maximum	500 2.1	kHz MHz
1	t_{wH}	Minimum Clock High Time	ADCLK SCLK	190 190	ns
1	t_{wL}	Minimum Clock Low Time	ADCLK SCLK	190 190	ns
1, 7	t_{PLH}, t_{PHL}	Maximum Propagation Delay, SCLK to D_{out}		240	ns
1, 7	t_h	Minimum Hold Time, SCLK to D_{out}		10	ns
2, 7	t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, $\overline{CS}$ to D_{out} High-Z		150	ns
2, 7	t_{PZL}, t_{PZH}	Maximum Propagation Delay, $\overline{CS}$ to D_{out} Driven	MC145050 MC145051	2 ADCLK cycles + 300 4.3	ns μs
3	t_{su}	Minimum Setup Time, D_{in} to SCLK		100	ns
3	t_h	Minimum Hold Time, SCLK to D_{in}		0	ns
4, 7, 8	t_d	Maximum Delay Time, EOC to D_{out} (MSB)	MC145051	100	ns
5	t_{su}	Minimum Setup Time, $\overline{CS}$ to SCLK	MC145050 MC145051	2 ADCLK cycles + 425 4.425	ns μs
—	t_{CSd}	Minimum Time Required Between 10th SCLK Falling Edge (≤0.8 V) and $\overline{CS}$ to Allow a Conversion	MC145050 MC145051	44 Note 2	ADCLK cycles
—	t_{CAs}	Maximum Delay Between 10th SCLK Falling Edge (≤2 V) and $\overline{CS}$ to Abort a Conversion	MC145050 MC145051	36 9	ADCLK cycles μs
5	t_h	Minimum Hold Time, Last SCLK to $\overline{CS}$		0	ns
6, 8	t_{PHL}	Maximum Propagation Delay, 10th SCLK to EOC	MC145051	4.35	μs
1	t_r, t_f	Maximum Input Rise and Fall Times	SCLK ADCLK D_{in}, $\overline{CS}$	1 250 10	ms ns μs
1, 4, 6-8	t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output		300	ns
—	C_{in}	Maximum Input Capacitance	AN0-AN10 ADCLK, SCLK, $\overline{CS}$, D_{in}	55 15	pF
—	C_{out}	Maximum Three-State Output Capacitance	D_{out}	15	pF

NOTES:

1. After the 10th SCLK falling edge (≤2 V), at least 1 SCLK rising edge (≥2 V) must occur within 38 ADCLKs (MC145050) or 18.5 μs (MC145051).
2. On the MC145051, a $\overline{CS}$ edge may be received immediately after an active transition on the EOC pin.

SWITCHING WAVEFORMS

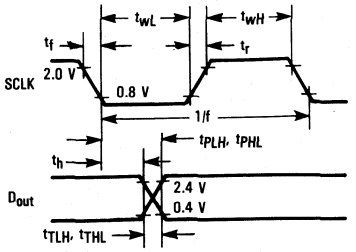


Figure 1

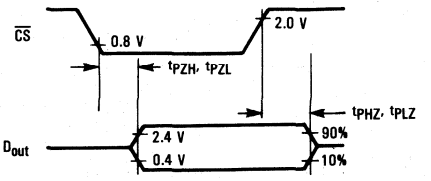


Figure 2

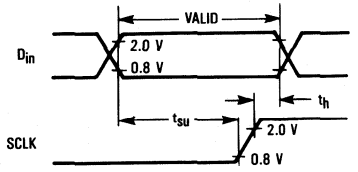
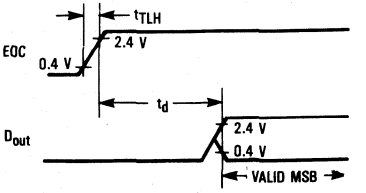


Figure 3



NOTE: D_{out} is driven only when $\overline{CS}$ is active (low).

Figure 4

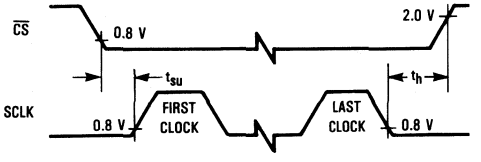


Figure 5

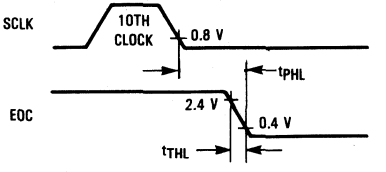


Figure 6

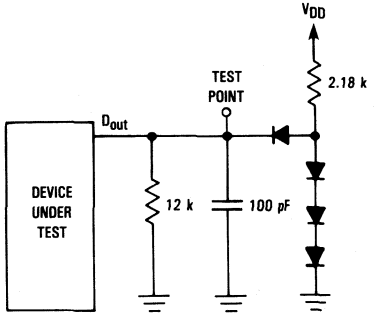


Figure 7. Test Circuit

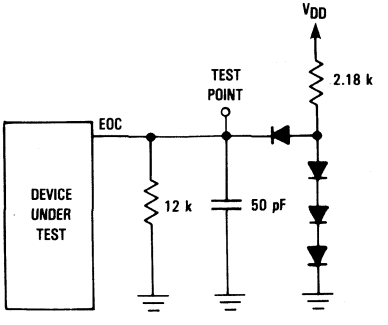


Figure 8. Test Circuit

PIN DESCRIPTIONS

DIGITAL INPUTS AND OUTPUTS

The various serial bit-stream formats for the MC145050/51 are illustrated in the timing diagrams of Figures 9 through 14. Table 1 assists selection of the appropriate diagram. Note that the ADCs accept 16 clocks which makes them SPI (serial peripheral interface) compatible.

Table 1. Timing Diagram Selection

No. of Clocks in Serial Transfer	Using $\overline{CS}$	Serial Transfer Interval	Figure No.
10	Yes	Don't Care	9
10	No	Don't Care	10
11 to 16	Yes	Shorter than Conversion	11
16	No	Shorter than Conversion	12
11 to 16	Yes	Longer than Conversion	13
16	No	Longer than Conversion	14

$\overline{CS}$ (Pin 15)

Active-Low Chip Select Input. Chip select initializes the chip to perform conversions and provides 3-state control of the data output pin (D_{out}). While inactive high, $\overline{CS}$ forces D_{out} to the high-impedance state and disables the data input (D_{in}) and serial clock (SCLK) pins. A high-to-low transition on $\overline{CS}$ resets the serial data port and synchronizes it to the MPU data stream. $\overline{CS}$ can remain active during the conversion cycle and can stay in the active low state for multiple serial transfers or $\overline{CS}$ can be inactive high after each transfer. If $\overline{CS}$ is kept active low between transfers, the length of each transfer is limited to either 10 or 16 SCLK cycles. If $\overline{CS}$ is in the inactive high state between transfers, each transfer can be anywhere from 10 to 16 SCLK cycles long. See the SCLK pin description for a more detailed discussion of these requirements.

Spurious chip selects caused by system noise are minimized by the internal circuitry. Any transitions on the $\overline{CS}$ pin are recognized as valid only if the level is maintained for a setup time plus two falling edges of ADCLK after the transition.

NOTE

If $\overline{CS}$ is inactive high after the 10th SCLK cycle and then goes active low before the A/D conversion is complete, the conversion is aborted and the chip enters the initial state, ready for another serial transfer/conversion sequence. At this point, the output data register contains the result from the conversion before the aborted conversion. Note that the last step of the A/D conversion sequence is to update the output data register with the result. Therefore, if $\overline{CS}$ goes active low in an attempt to abort the conversion too close to the end of the conversion sequence, the result register may be corrupted and the chip could be thrown out of sync with the processor until $\overline{CS}$ is toggled again (refer to the AC Electrical Characteristics in the spec tables).

D_{out} (Pin 16)

Serial Data Output of the A/D Conversion Result. This output is in the high-impedance state when $\overline{CS}$ is inactive high. When the chip recognizes a valid active low on $\overline{CS}$, D_{out} is taken out of the high-impedance state and is driven with the MSB of the previous conversion result. (For the first transfer after power-up, data on D_{out} is undefined for the entire transfer.) The value on D_{out} changes to the second most significant result bit upon the first falling edge of SCLK. The remaining result bits are shifted out in order, with the LSB appearing on D_{out} upon the ninth falling edge of SCLK. Note that the order of the transfer is MSB to LSB. Upon the 10th falling edge of SCLK, D_{out} is immediately driven low (if allowed by $\overline{CS}$) so that transfers of more than 10 SCLKs read zeroes as the unused LSBs.

When $\overline{CS}$ is held active low between transfers, D_{out} is driven from a low level to the MSB of the conversion result for three cases: Case 1—upon the 16th SCLK falling edge if the transfer is longer than the conversion time (Figure 14); Case 2—upon completion of a conversion for a 16-bit transfer interval shorter than the conversion (Figure 12); Case 3—upon completion of a conversion for a 10-bit transfer (Figure 10).

D_{in} (Pin 17)

Serial Data Input. The four-bit serial input stream begins with the MSB of the analog mux address (or the user test mode) that is to be converted next. The address is shifted in on the first four rising edges of SCLK. After the four mux address bits have been received, the data on D_{in} is ignored for the remainder of the present serial transfer. See Table 2 *in* ***Applications Information***.

SCLK (Pin 18)

Serial Data Clock. This clock input drives the internal I/O state machine to perform three major functions: (1) drives the data shift registers to simultaneously shift in the next mux address from the D_{in} pin and shift out the previous conversion result on the D_{out} pin, (2) begins sampling the analog voltage onto the RC DAC as soon as the new mux address is available, and (3) transfers control to the A/D conversion state machine (driven by ADCLK) after the last bit of the previous conversion result has been shifted out on the D_{out} pin.

The serial data shift registers are completely static, allowing SCLK rates down to dc in a continuous or intermittent mode. There are some cases, however, that require a minimum SCLK frequency as discussed later in this section. SCLK need not be synchronous to ADCLK. At least ten SCLK cycles are required for each simultaneous data transfer. After the serial port has been initiated to perform a serial transfer*, the new

*The serial port can be initiated in three ways: (1) a recognized $\overline{CS}$ falling edge, (2) the end of an A/D conversion if the port is performing either a 10-bit or a 16-bit "shorter-than-conversion" transfer with $\overline{CS}$ active low between transfers, and (3) the 16th falling edge of SCLK if the port is performing 16-bit "longer-than-conversion" transfers with $\overline{CS}$ active low between transfers.

mux address is shifted in on the first four rising edges of SCLK, and the previous 10-bit conversion result is shifted out on the first nine falling edges of SCLK. After the fourth rising edge of SCLK, the new mux address is available; therefore, on the next edge of SCLK (the fourth falling edge), the analog input voltage on the selected mux input begins charging the RC DAC and continues to do so until the tenth falling edge of SCLK. After this tenth SCLK edge, the analog input voltage is disabled from the RC DAC and the RC DAC begins the "hold" portion of the A/D conversion sequence. Also upon this tenth SCLK edge, control of the internal circuitry is transferred to ADCLK which drives the successive approximation logic to complete the conversion. If 16 SCLK cycles are used during each transfer, then there is a constraint on the minimum SCLK frequency. Specifically, there must be at least one rising edge on SCLK before the A/D conversion is complete. If the SCLK frequency is too low and a rising edge does not occur during the conversion, the chip is thrown out of sync with the processor and $\overline{CS}$ needs to be toggled in order to restore proper operation. If 10 SCLKs are used per transfer, then there is no lower frequency limit on SCLK. Also note that if the ADC is operated such that $\overline{CS}$ is inactive high between transfers, then the number of SCLK cycles per transfer can be anything between 10 and 16 cycles, but the "rising edge" constraint is still in effect if more than 10 SCLKs are used. (If $\overline{CS}$ stays active low for multiple transfers, the number of SCLK cycles must be either 10 or 16.)

ADCLK (Pin 19, MC145050 Only)

This pin clocks the dynamic A/D conversion sequence, and may be asynchronous to SCLK. Control of the chip passes to ADCLK after the tenth falling edge of SCLK. Control of the chip is passed back to SCLK after the successive approximation conversion sequence is complete (44 ADCLK cycles), or after a valid chip select is recognized. ADCLK also drives the $\overline{CS}$ recognition logic. The chip ignores transitions on $\overline{CS}$ unless the state remains for a setup time plus two falling edges of ADCLK. The source driving ADCLK must be free running.

EOC (Pin 19, MC145051 Only)

End-of-Conversion Output. EOC goes low on the tenth falling edge of SCLK. A low-to-high transition on EOC occurs when the A/D conversion is complete and the data is ready for transfer.

ANALOG INPUTS AND TEST MODE

AN0 through AN10 (Pins 1-9, 11, 12)

Analog Multiplexer Inputs. The input AN0 is addressed by loading $0 into the mux address register. AN1 is addressed by $1, AN2 by $2, ..., AN10 by $A. Table 2 shows the input format for a 16-bit stream. The mux features a break-before-make switching structure to minimize noise injection into the analog inputs. The source resistance driving these inputs must be ≤ 10 kΩ.

There are three tests available that verify the functionality of all the control logic as well as the successive approximation comparator. These tests are performed by addressing $B, $C, or $D and they convert a voltage of $(V_{ref}+V_{AG})/2$, V_{AG}, or V_{ref}, respectively. The voltages are obtained internally by sampling V_{ref} or V_{AG} onto the appropriate elements of the RC DAC during the sample phase. Addressing $B, $C, or $D produces an output of $200 (half scale), $000, or $3FF (full scale), respectively, if the converter is functioning properly. However, deviation from these values occurs in the presence of sufficient system noise (external to the chip) on V_{DD}, V_{SS}, V_{ref}, or V_{AG}.

POWER AND REFERENCE PINS

V_{SS} and V_{DD} (Pins 10 and 20)

Device Supply Pins. V_{SS} is normally connected to digital ground; V_{DD} is connected to a positive digital supply voltage. Low frequency $(V_{DD}-V_{SS})$ variations over the range of 4.5 to 5.5 volts do not affect the A/D accuracy. (See the Operations Ranges table for restrictions on V_{ref} and V_{AG} relative to V_{DD} and V_{SS}.) Excessive inductance in the V_{DD} or V_{SS} lines, as on automatic test equipment, may cause A/D offsets $> \pm 1$ LSB. Use of a 0.1 μF bypass capacitor across these pins is recommended.

V_{AG} and V_{ref} (Pins 13 and 14)

Analog reference voltage pins which determine the lower and upper boundary of the A/D conversion. Analog input voltages $\geq V_{ref}$ produce a full scale output and input voltages $\leq V_{AG}$ produce an output of zero. CAUTION: The analog input voltage must be $\geq V_{SS}$ and $\leq V_{DD}$. The A/D conversion result is ratiometric to $V_{ref}-V_{AG}$. V_{ref} and V_{AG} must be as noise-free as possible to avoid degradation of the A/D conversion. Ideally, V_{ref} and V_{AG} should be single-point connected to the voltage supply driving the system's transducers. Use of a 0.2 μF bypass capacitor across these pins is strongly urged.

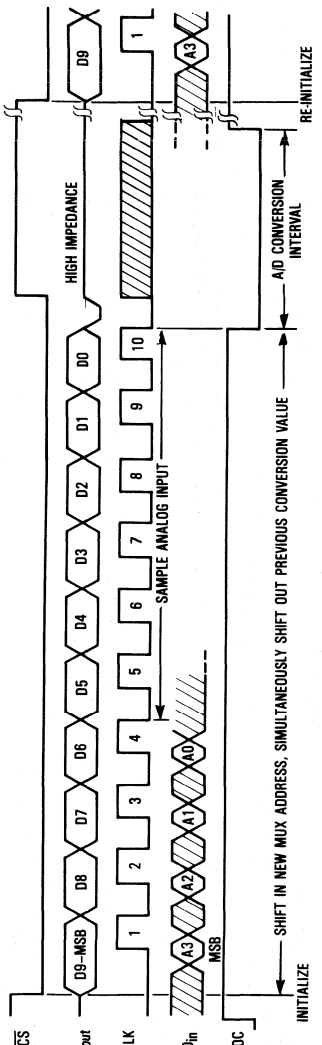


Figure 9. Timing for 10-Clock Transfer Using $\overline{CS}$*

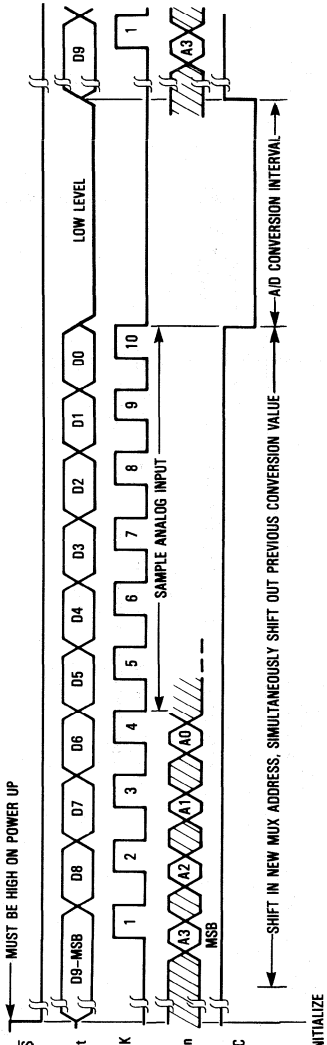


Figure 10. Timing for 10-Clock Transfer Not Using $\overline{CS}$*

NOTES:
D9, D8, D7, . . . , D0 = the result of the previous A/D conversion.
A3, A2, A1, A0 = the mux address for the next A/D conversion.
*This figure illustrates the behavior of the MC145051. The MC145050 behaves identically except there is no EOC signal and the conversion time is 44 ADCLK cycles (user-controlled time).

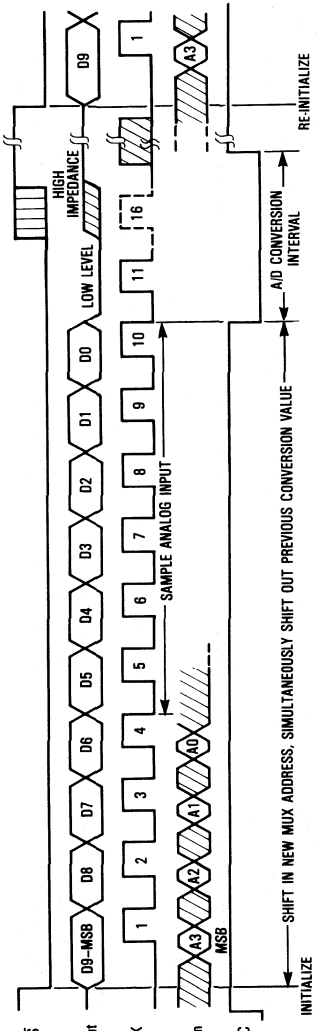


Figure 11. Timing for 11- to 16-Clock Transfer Using $\overline{CS}$* (Serial Transfer Interval Shorter Than Conversion)

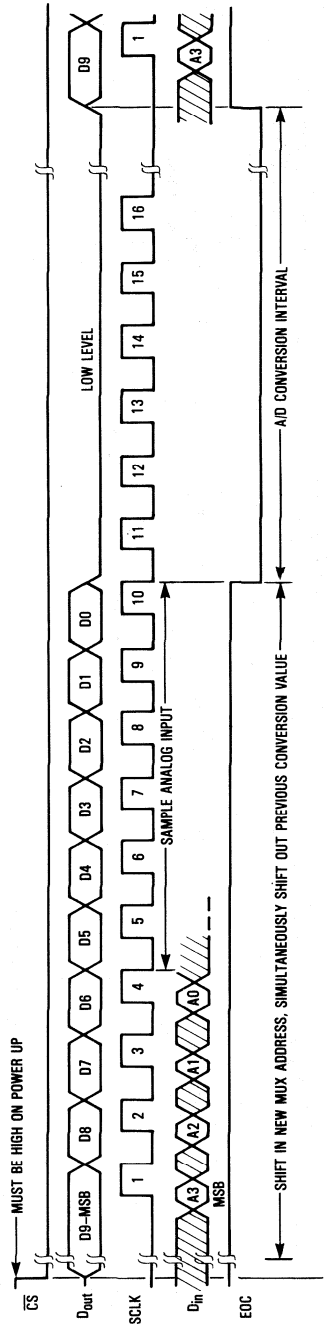


Figure 12. Timing for 16-Clock Transfer Not Using $\overline{CS}$* (Serial Transfer Interval Shorter Than Conversion)

NOTES:
D9, D8, D7, . . . , D0 = the result of the previous A/D conversion.
A3, A2, A1, A0 = the mux address for the next A/D conversion.
*This figure illustrates the behavior of the MC145051. The MC145050 behaves identically except there is no EOC signal and the conversion time is 44 ADCLK cycles (user-controlled time).

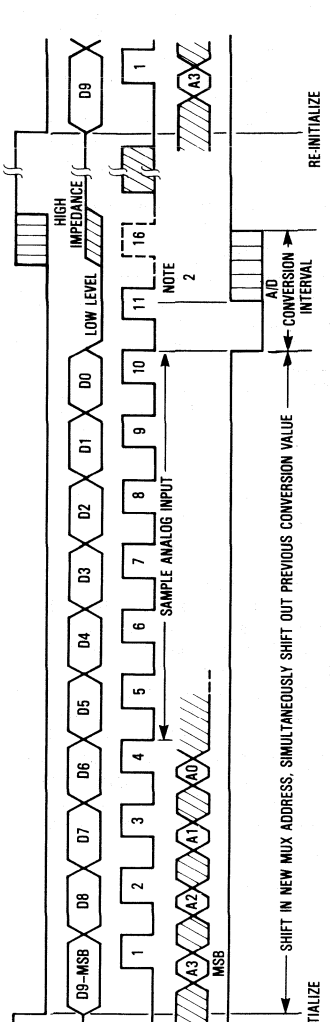


Figure 13. Timing for 11- to 16-Clock Transfer Using $\overline{CS}$*
(Serial Transfer Interval Longer Than Conversion)

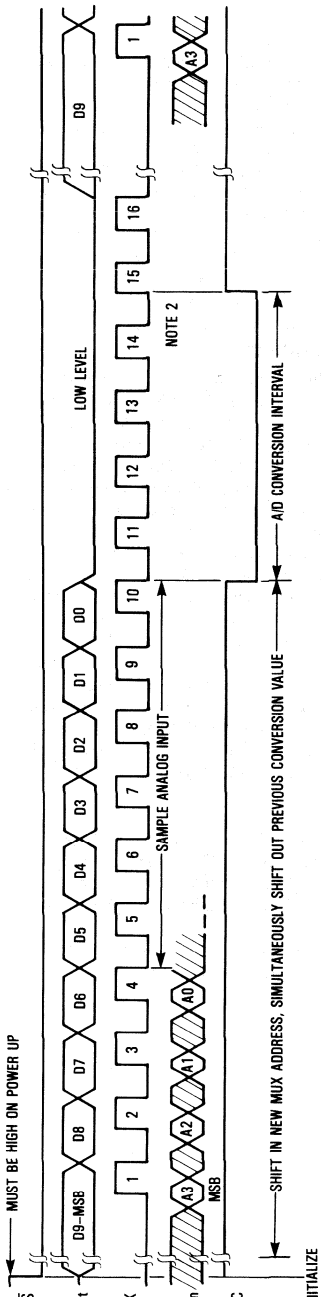


Figure 14. Timing for 16-Clock Transfer Not Using $\overline{CS}$*
(Serial Transfer Interval Longer Than Conversion)

NOTES:
D9, D8, D7, . . . , D0 = the result of the previous A/D conversion.
A3, A2, A1, A0 = the mux address for the next A/D conversion.

*NOTES:
1. This figure illustrates the behavior of the MC145051. The MC145050 behaves identically except there is no EOC signal and the conversion time is 44 ADCLK cycles (user-controlled time).
2. The 11th SCLK rising edge must occur before the conversion is complete. Otherwise the serial port is thrown out of sync with the microprocessor for the remainder of the transfer.

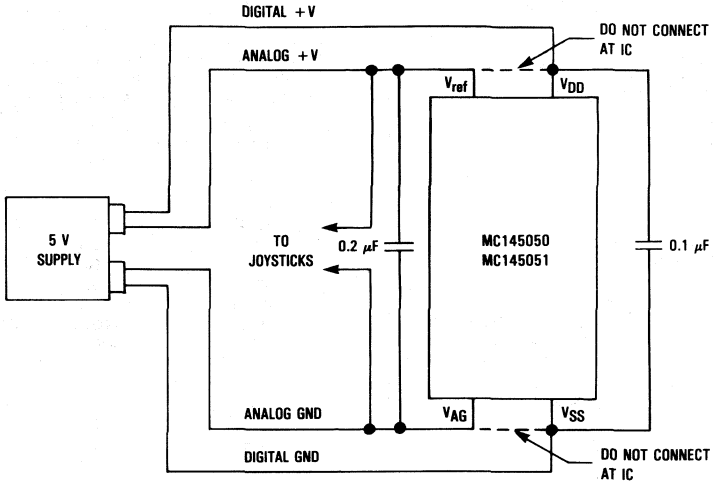


Figure 16. Alternate Configuration Using the Digital Supply for the Reference Voltage

Compatible Motorola MCUs/MPUs

This is not a complete listing of Motorola's MCUs/MPUs. Contact your Motorola representative if you need additional information.

Instruction Set	Memory (Bytes)		SPI ① SCI ②	Device Number
	ROM	EEPROM		
M6805	2096	—	—	MC68HC05C2
	2096	—	Yes	MC68HC05C3
	4160	—	Yes	MC68HC05C4
	4160 ③	—	Yes	MC68HSC05C4
	8K ③	—	Yes	MC68HSC05C8
	4160 ④	—	Yes	MC68HCL05C4
	8K ④	—	Yes	MC68HCL05C8
	7700	—	Yes	MC68HC05C8
	—	4160	—	MC68HC805C4
M68000	—	—	—	MC68HC000

① SPI = Serial Peripheral Interface.

② SCI = Serial Communications Interface.

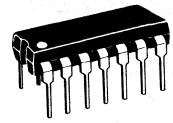
③ High speed.

④ Low power.

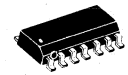
MC145053

Advance Information

10-Bit A/D Converter with Serial Interface
CMOS



P SUFFIX
PLASTIC
CASE 646



D SUFFIX
SOG
CASE 751A

ORDERING INFORMATION

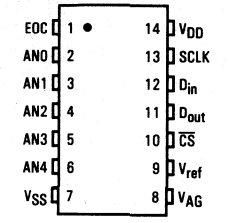
MC145053P	Plastic DIP
MC145053D	SOG Package

This ratiometric 10-bit ADC has a serial interface port to provide communication with MCUs and MPUs. *Either a 10- or 16-bit format can be used.* The 16-bit format can be one continuous 16-bit stream or two intermittent 8-bit streams. The converter operates from a single power supply with no external trimming required. Reference voltages down to 2.5 V are accommodated.

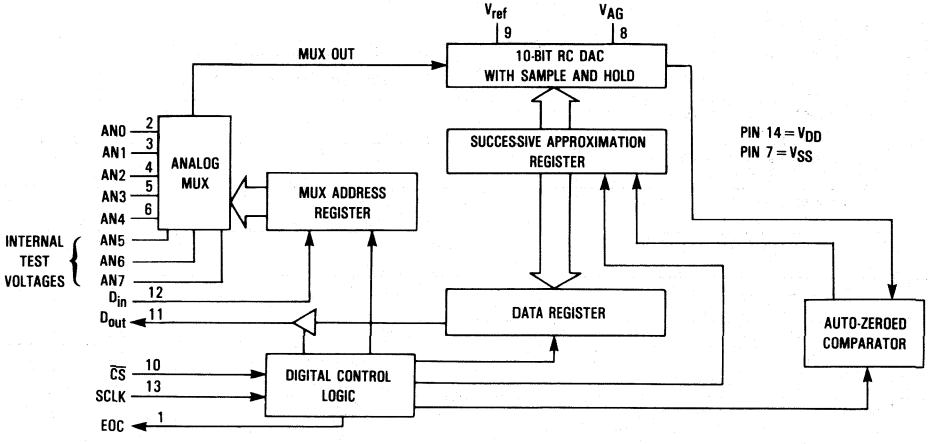
The MC145053 has an internal clock oscillator to operate the dynamic A/D conversion sequence and an end-of-conversion (EOC) output.

- 5 Analog Input Channels with Internal Sample-and-Hold
- Operating Temperature Range: −40° to 125°C
- Successive Approximation Conversion Time: 88 μs Maximum
- Maximum Sample Rate: 10.7 ks/s
- Analog Input Range with 5-Volt Supply: 0 to 5 V
- Monotonic with No Missing Codes
- Direct Interface to Motorola SPI and National MICROWIRE Serial Data Ports
- Digital Inputs/Outputs are TTL, NMOS, and CMOS Compatible
- Low Power Consumption: 14 mW
- Chip Complexity: 1630 Elements (FETs, Capacitors, etc.)

PIN ASSIGNMENT



BLOCK DIAGRAM



MICROWIRE is a trademark of National Semiconductor Corp.
This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage (Referenced to V_{SS})	−0.5 to +6.0	V
V_{ref}	DC Reference Voltage	V_{AG} to V_{DD}+0.1	V
V_{AG}	Analog Ground	V_{SS}−0.1 to V_{ref}	V
V_{in}	DC Input Voltage, Any Analog or Digital Input	V_{SS}−0.5 to V_{DD}+0.5	V
V_{out}	DC Output Voltage	V_{SS}−0.5 to V_{DD}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{DD}, I_{SS}	DC Supply Current, V_{DD} and V_{SS} Pins	±50	mA
T_{stg}	Storage Temperature	−65 to 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Operation Ranges below.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

OPERATION RANGES (Applicable to Guaranteed Limits)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage, Referenced to V_{SS}	4.5 to 5.5	V
V_{ref}	DC Reference Voltage (Note 1)	V_{AG}+2.5 to V_{DD}+0.1	V
V_{AG}	Analog Ground (Note 1)	V_{SS}−0.1 to V_{ref}−2.5	V
V_{AI}	Analog Input Voltage (Note 2)	V_{AG} to V_{ref}	V
V_{in}, V_{out}	Digital Input Voltage, Output Voltage	V_{SS} to V_{DD}	V
T_A	Ambient Operating Temperature	−40 to 125	°C

NOTES:
1. *Reference voltages down to 1.0 V ($V_{ref}-V_{AG}=1.0$ V) are functional, but the A/D converter electrical characteristics are not guaranteed.*
2. Analog input voltages greater than V_{ref} convert to full scale. Input voltages less than V_{AG} convert to zero. See V_{ref} and V_{AG} pin descriptions.

DC ELECTRICAL CHARACTERISTICS

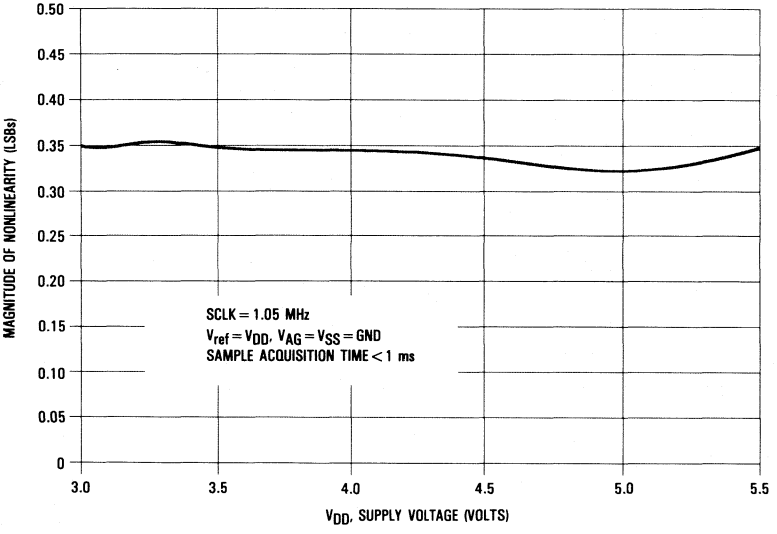
(Voltages Referenced to V_{SS}, Full Temperature and Voltage Ranges per Operation Ranges table, unless otherwise indicated)

Symbol	Parameter	Test Conditions	Guaranteed Limit	Unit
V_{IH}	Minimum High-Level Input Voltage (D_{in}, SCLK, $\overline{CS}$)		2.0	V
V_{IL}	Maximum Low-Level Input Voltage (D_{in}, SCLK, $\overline{CS}$)		0.8	V
V_{OH}	Minimum High-Level Output Voltage (D_{out}, EOC)	$I_{out}=-1.6$ mA $I_{out}=-20$ μA	2.4 V_{DD}−0.1	V
V_{OL}	Maximum Low-Level Output Voltage (D_{out}, EOC)	$I_{out}=+1.6$ mA $I_{out}=+20$ μA	0.4 0.1	V
I_{in}	Maximum Input Leakage Current (D_{in}, SCLK, $\overline{CS}$)	$V_{in}=V_{SS}$ or V_{DD}	±2.5	μA
I_{OZ}	Maximum Three-State Leakage Current (D_{out})	$V_{out}=V_{SS}$ or V_{DD}	±10	μA
I_{DD}	Maximum Power Supply Current	$V_{in}=V_{SS}$ or V_{DD}, All Outputs Open	2.5	mA
I_{ref}	Maximum Static Analog Reference Current (V_{ref})	$V_{ref}=V_{DD}$, $V_{AG}=V_{SS}$	100	μA
I_{AI}	Maximum Analog Mux Input Leakage Current between all deselected inputs and any selected input (AN0-AN4)	$V_{AI}=V_{SS}$ to V_{DD}	±1	μA

A/D CONVERTER ELECTRICAL CHARACTERISTICS

(Full Temperature and Voltage Ranges per Operation Ranges table)

Characteristic	Definition and Test Conditions	Guaranteed Limit	Unit
Resolution	Number of bits resolved by the A/D converter	10	Bits
Maximum Nonlinearity	Maximum difference between an ideal and an actual ADC transfer function	±1	LSB
Maximum Zero Error	Difference between the maximum input voltage of an ideal and an actual ADC for zero output code	±1	LSB
Maximum Full-Scale Error	Difference between the minimum input voltage of an ideal and an actual ADC for full-scale output code	±1	LSB
Maximum Total Unadjusted Error	Maximum sum of nonlinearity, zero error, and full-scale error	±1	LSB
Maximum Quantization Error	Uncertainty due to converter resolution	±1/2	LSB
Absolute Accuracy	Difference between the actual input voltage and the full-scale weighted equivalent of the binary output code, all error sources included	±1-1/2	LSB
Maximum Conversion Time	Total time to perform a single analog-to-digital conversion	88	μs
Data Transfer Time	Total time to transfer digital serial data into and out of the device	10 to 16	SCLK cycles
Sample Acquisition Time	Analog input acquisition time window	6	SCLK cycles
Minimum Total Cycle Time	Total time to transfer serial data, sample the analog input, and perform the conversion; SCLK = 2.1 MHz	93	μs
Maximum Sample Rate	Rate at which analog inputs may be sampled; SCLK = 2.1 MHz	10.7	ks/s



NOTE: This "typical" graph is not to be used for design purposes but is intended as an indication of the IC's potential performance.

Graph 1. Typical Nonlinearity vs Supply Voltage

AC ELECTRICAL CHARACTERISTICS

(Full Temperature and Voltage Ranges per Operation Ranges table)

Figure	Symbol	Parameter		Guaranteed Limit	Unit
1	f	Clock Frequency, SCLK Note: Refer to t_{wH}, t_{wL} below	(10-bit xfer) Min (11- to 16-bit xfer) Min (10- to 16-bit xfer) Max	0 Note 1 2.1	MHz
1	t_{wH}	Minimum Clock High Time, SCLK		190	ns
1	t_{wL}	Minimum Clock Low Time, SCLK		190	ns
1, 7	t_{PLH}, t_{PHL}	Maximum Propagation Delay, SCLK to D_{out}		240	ns
1, 7	t_h	Minimum Hold Time, SCLK to D_{out}		10	ns
2, 7	t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, $\overline{CS}$ to D_{out} High-Z		150	ns
2, 7	t_{PZL}, t_{PZH}	Maximum Propagation Delay, $\overline{CS}$ to D_{out} Driven		4.3	μs
3	t_{su}	Minimum Setup Time, D_{in} to SCLK		100	ns
3	t_h	Minimum Hold Time, SCLK to D_{in}		0	ns
4, 7, 8	t_d	Maximum Delay Time, EOC to D_{out} (MSB)		100	ns
5	t_{su}	Minimum Setup Time, $\overline{CS}$ to SCLK		4.425	μs
—	t_{CSd}	Minimum Time Required Between 10th SCLK Falling Edge ($\leq$0.8 V) and $\overline{CS}$ to Allow a Conversion		Note 2	
—	t_{CAs}	Maximum Delay Between 10th SCLK Falling Edge ($\leq$2 V) and $\overline{CS}$ to Abort a Conversion		9	μs
5	t_h	Minimum Hold Time, Last SCLK to $\overline{CS}$		0	ns
6, 8	t_{PHL}	Maximum Propagation Delay, 10th SCLK to EOC		4.35	μs
1	t_r, t_f	Maximum Input Rise and Fall Times	SCLK D_{in}, $\overline{CS}$	1 10	ms μs
1, 4, 6-8	t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output		300	ns
—	C_{in}	Maximum Input Capacitance	AN0-AN4 SCLK, $\overline{CS}$, D_{in}	55 15	pF
—	C_{out}	Maximum Three-State Output Capacitance	D_{out}	15	pF

NOTES:

1. After the 10th SCLK falling edge ($\leq$2 V), at least 1 SCLK rising edge ($\geq$2 V) must occur within 18.5 μs.
2. A $\overline{CS}$ edge may be received immediately after an active transition on the EOC pin.

SWITCHING WAVEFORMS

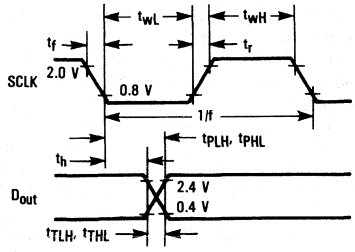


Figure 1

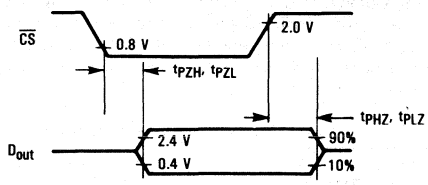


Figure 2

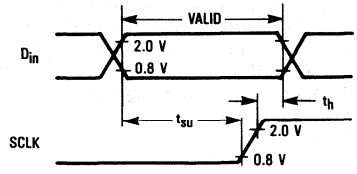
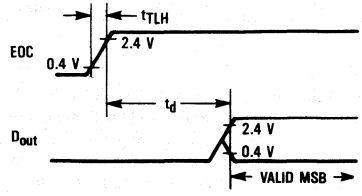


Figure 3



NOTE: D_{out} is driven only when $\overline{CS}$ is active (low).

Figure 4

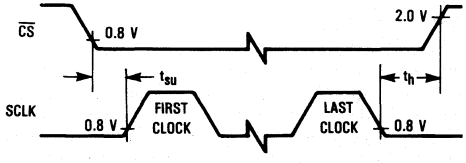


Figure 5

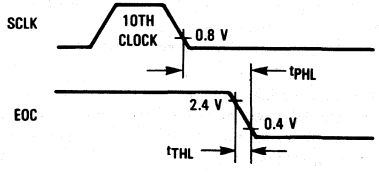


Figure 6

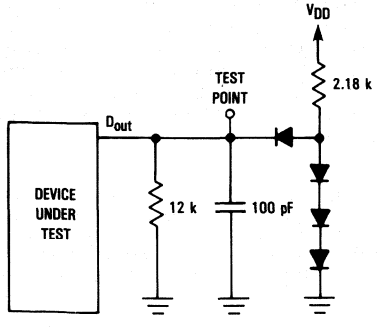


Figure 7. Test Circuit

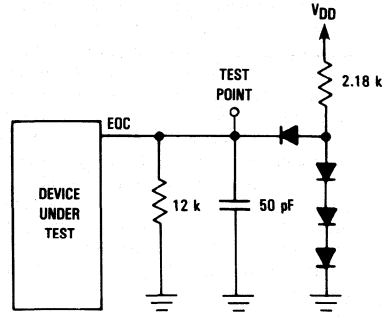


Figure 8. Test Circuit

PIN DESCRIPTIONS

DIGITAL INPUTS AND OUTPUTS

The various serial bit-stream formats for the MC145053 are illustrated in the timing diagrams of Figures 9 through 14. Table 1 assists selection of the appropriate diagram. Note that the ADC accepts 16 clocks which makes it SPI (serial peripheral interface) compatible.

Table 1. Timing Diagram Selection

No. of Clocks in Serial Transfer	Using $\overline{CS}$	Serial Transfer Interval	Figure No.
10	Yes	Don't Care	9
10	No	Don't Care	10
11 to 16	Yes	Shorter than Conversion	11
16	No	Shorter than Conversion	12
11 to 16	Yes	Longer than Conversion	13
16	No	Longer than Conversion	14

$\overline{CS}$ (Pin 10)

Active-Low Chip Select Input. Chip select initializes the chip to perform conversions and provides 3-state control of the data output pin (D_{out}). While inactive high, $\overline{CS}$ forces D_{out} to the high-impedance state and disables the data input (D_{in}) and serial clock (SCLK) pins. A high-to-low transition on $\overline{CS}$ resets the serial data port and synchronizes it to the MPU data stream. $\overline{CS}$ can remain active during the conversion cycle and can stay in the active low state for multiple serial transfers or $\overline{CS}$ can be inactive high after each transfer. If $\overline{CS}$ is kept active low between transfers, the length of each transfer is limited to either 10 or 16 SCLK cycles. If $\overline{CS}$ is in the inactive high state between transfers, each transfer can be anywhere from 10 to 16 SCLK cycles long. See the SCLK pin description for a more detailed discussion of these requirements.

Spurious chip selects caused by system noise are minimized by the internal circuitry. Any transitions on the $\overline{CS}$ pin are recognized as valid only if the level is maintained for about 4 μs after the transition.

NOTE

If $\overline{CS}$ is inactive high after the 10th SCLK cycle and then goes active low before the A/D conversion is complete, the conversion is aborted and the chip enters the initial state, ready for another serial transfer/conversion sequence. At this point, the output data register contains the result from the conversion before the aborted conversion. Note that the last step of the A/D conversion sequence is to update the output data register with the result. Therefore, if $\overline{CS}$ goes active low in an attempt to abort the conversion too close to the end of the conversion sequence, the result register may be corrupted and the chip could be thrown out of sync with the processor until $\overline{CS}$ is toggled again (refer to the AC Electrical Characteristics in the spec tables).

D_{out} (Pin 11)

Serial Data Output of the A/D Conversion Result. This output is in the high-impedance state when $\overline{CS}$ is inactive high. When the chip recognizes a valid active low on $\overline{CS}$, D_{out} is taken out of the high-impedance state and is driven with the MSB of the previous conversion result. (For the first transfer after power-up, data on D_{out} is undefined for the entire transfer.) The value on D_{out} changes to the second most significant result bit upon the first falling edge of SCLK. The remaining result bits are shifted out in order, with the LSB appearing on D_{out} upon the ninth falling edge of SCLK. Note that the order of the transfer is MSB to LSB. Upon the 10th falling edge of SCLK, D_{out} is immediately driven low (if allowed by $\overline{CS}$) so that transfers of more than 10 SCLKs read zeroes as the unused LSBs.

When $\overline{CS}$ is held active low between transfers, D_{out} is driven from a low level to the MSB of the conversion result for three cases: Case 1—upon the 16th SCLK falling edge if the transfer is longer than the conversion time (Figure 14); Case 2—upon completion of a conversion for a 16-bit transfer interval shorter than the conversion (Figure 12); Case 3—upon completion of a conversion for a 10-bit transfer (Figure 10).

D_{in} (Pin 12)

Serial Data Input. The four-bit serial input stream begins with the MSB of the analog mux address (or the user test mode) that is to be converted next. The address is shifted in on the first four rising edges of SCLK. After the four mux address bits have been received, the data on D_{in} is ignored for the remainder of the present serial transfer. See Table 2 in **Applications Information**.

SCLK (Pin 13)

Serial Data Clock. This clock input drives the internal I/O state machine to perform three major functions: (1) drives the data shift registers to simultaneously shift in the next mux address from the D_{in} pin and shift out the previous conversion result on the D_{out} pin, (2) begins sampling the analog voltage onto the RC DAC as soon as the new mux address is available, and (3) transfers control to the A/D conversion state machine after the last bit of the previous conversion result has been shifted out on the D_{out} pin.

The serial data shift registers are completely static, allowing SCLK rates down to dc in a continuous or intermittent mode. There are some cases, however, that require a minimum SCLK frequency as discussed later in this section. At least ten SCLK cycles are required for each simultaneous data transfer. After the serial port has been initiated to perform a serial transfer*, the new mux address is shifted in on the first four rising edges

*The serial port can be initiated in three ways: (1) a recognized $\overline{CS}$ falling edge, (2) the end of an A/D conversion if the port is performing either a 10-bit or a 16-bit "shorter-than-conversion" transfer with $\overline{CS}$ active low between transfers, and (3) the 16th falling edge of SCLK if the port is performing 16-bit "longer-than-conversion" transfers with $\overline{CS}$ active low between transfers.

of SCLK, and the previous 10-bit conversion result is shifted out on the first nine falling edges of SCLK. After the fourth rising edge of SCLK, the new mux address is available; therefore, on the next edge of SCLK (the fourth falling edge), the analog input voltage on the selected mux input begins charging the RC DAC and continues to do so until the tenth falling edge of SCLK. After this tenth SCLK edge, the analog input voltage is disabled from the RC DAC and the RC DAC begins the "hold" portion of the A/D conversion sequence. Also upon this tenth SCLK edge, control of the internal circuitry is transferred to the internal clock oscillator which drives the successive approximation logic to complete the conversion. If 16 SCLK cycles are used during each transfer, then there is a constraint on the minimum SCLK frequency. Specifically, there must be at least one rising edge on SCLK before the A/D conversion is complete. If the SCLK frequency is too low and a rising edge does not occur during the conversion, the chip is thrown out of sync with the processor and $\overline{CS}$ needs to be toggled in order to restore proper operation. If 10 SCLKs are used per transfer, then there is no lower frequency limit on SCLK. Also note that if the ADC is operated such that $\overline{CS}$ is inactive high between transfers, then the number of SCLK cycles per transfer can be anything between 10 and 16 cycles, but the "rising edge" constraint is still in effect if more than 10 SCLKs are used. (If $\overline{CS}$ stays active low for multiple transfers, the number of SCLK cycles must be either 10 or 16.)

EOC (Pin 1)

End-of-Conversion Output. EOC goes low on the tenth falling edge of SCLK. A low-to-high transition on EOC occurs when the A/D conversion is complete and the data is ready for transfer.

ANALOG INPUTS AND TEST MODES

AN0 through AN4 (Pins 2-6)

Analog Multiplexer Inputs. The input AN0 is addressed by loading $0 into the mux address register. AN1 is addressed by $1, AN2 by $2, AN3 by $3, and AN4 by $4. Table 2 shows the input format for a 16-bit stream. The mux features a break-before-make switching structure to minimize noise injection into the analog inputs. The source resistance driving these inputs must be ≤ 10 kΩ.

There are three tests available that verify the functionality of all the control logic as well as the successive approximation comparator. These tests are performed by addressing $B, $C, or $D and they convert a voltage of $(V_{ref}+V_{AG})/2$, V_{AG}, or V_{ref}, respectively. The voltages are obtained internally by sampling V_{ref} or V_{AG} onto the appropriate elements of the RC DAC during the sample phase. Addressing $B, $C, or $D produces an output of $200 (half scale), $000, or $3FF (full scale), respectively, if the converter is functioning properly. However, deviation from these values occurs in the presence of sufficient system noise (external to the chip) on V_{DD}, V_{SS}, V_{ref}, or V_{AG}.

POWER AND REFERENCE PINS

V_{SS} and V_{DD} (Pins 7 and 14)

Device Supply Pins. V_{SS} is normally connected to digital ground; V_{DD} is connected to a positive digital supply voltage. Low frequency $(V_{DD}-V_{SS})$ variations over the range of 4.5 to 5.5 volts do not affect the A/D accuracy. (See the Operations Ranges table for restrictions on V_{ref} and V_{AG} relative to V_{DD} and V_{SS}.) Excessive inductance in the V_{DD} or V_{SS} lines, as on automatic test equipment, may cause A/D offsets $> \pm 1$ LSB. Use of a 0.1 μF bypass capacitor across these pins is recommended.

V_{AG} and V_{ref} (Pins 8 and 9)

Analog reference voltage pins which determine the lower and upper boundary of the A/D conversion. Analog input voltages $\geq V_{ref}$ produce a full scale output and input voltages $\leq V_{AG}$ produce an output of zero. CAUTION: The analog input voltage must be $\geq V_{SS}$ and $\leq V_{DD}$. The A/D conversion result is ratiometric to $V_{ref}-V_{AG}$. V_{ref} and V_{AG} must be as noise-free as possible to avoid degradation of the A/D conversion. Ideally, V_{ref} and V_{AG} should be single-point connected to the voltage supply driving the system's transducers. Use of a 0.2 μF bypass capacitor across these pins is strongly urged.

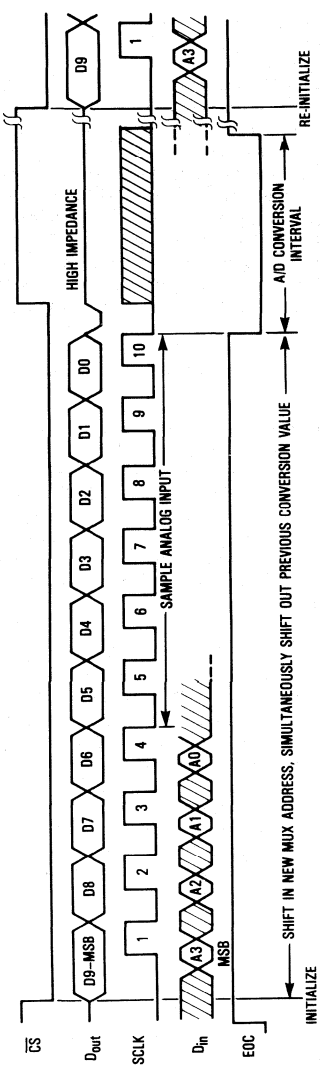


Figure 9. Timing for 10-Clock Transfer Using $\overline{CS}$

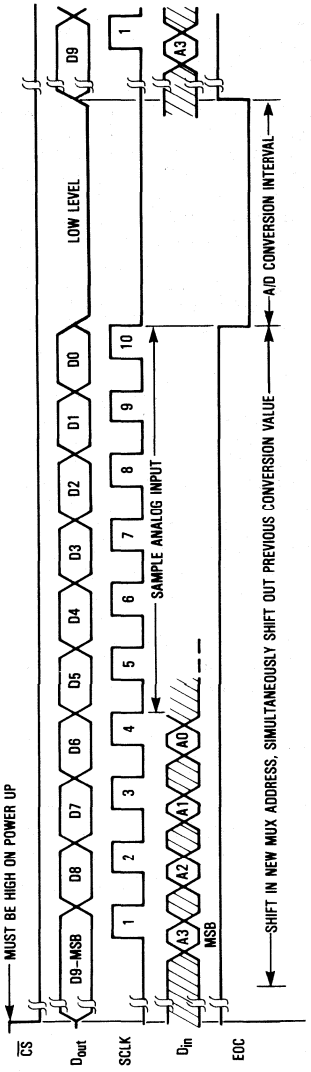


Figure 10. Timing for 10-Clock Transfer Not Using $\overline{CS}$

NOTES:
D9, D8, D7, D6, D5, . . . D0 = the result of the previous A/D conversion.
A3, A2, A1, A0 = the mux address for the next A/D conversion.

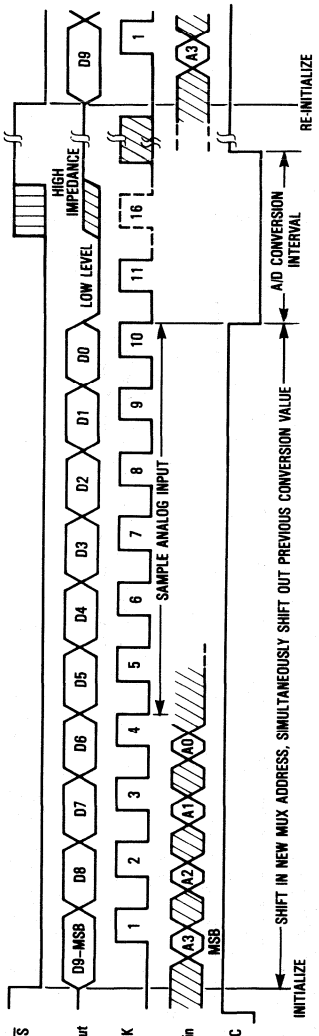


Figure 11. Timing for 11- to 16-Clock Transfer Using $\overline{CS}$
(Serial Transfer Interval Shorter Than Conversion)

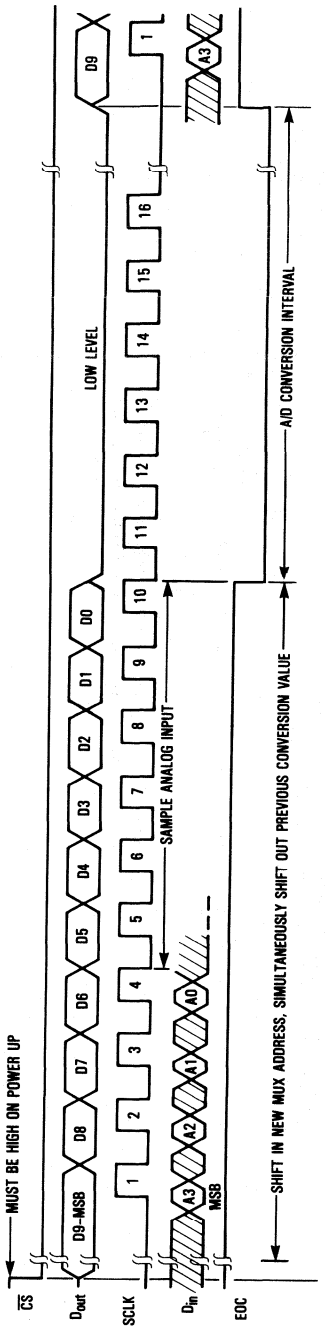


Figure 12. Timing for 16-Clock Transfer Not Using $\overline{CS}$
(Serial Transfer Interval Shorter Than Conversion)

NOTES:
D9, D8, D7, D6, D5, . . . , D0 = the result of the previous A/D conversion.
A3, A2, A1, A0 = the mux address for the next A/D conversion.

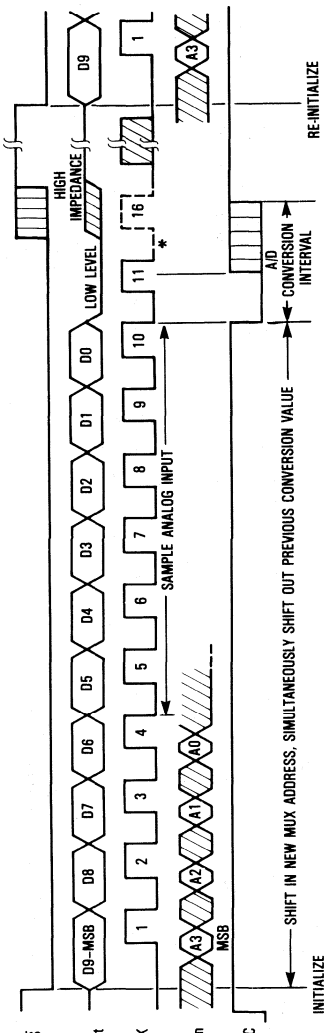


Figure 13. Timing for 11- to 16-Clock Transfer Using $\overline{CS}$
(Serial Transfer Interval Longer Than Conversion)

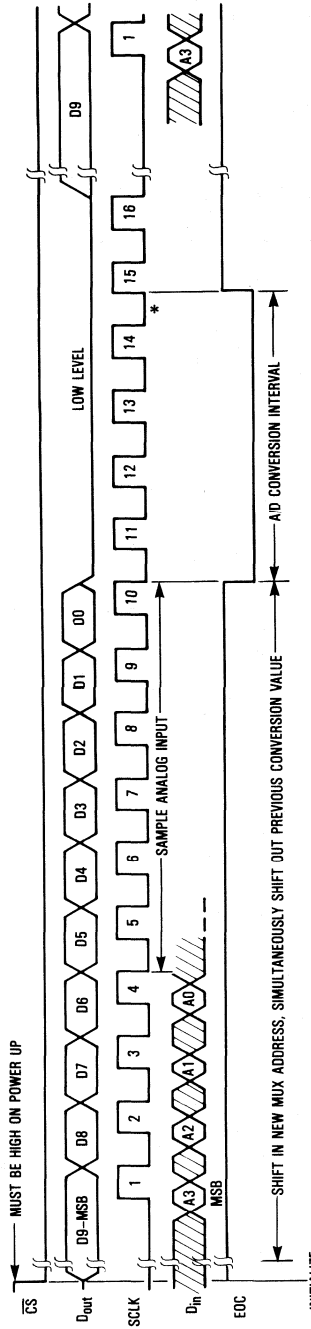


Figure 14. Timing for 16-Clock Transfer Not Using $\overline{CS}$
(Serial Transfer Interval Longer Than Conversion)

NOTES:
D9, D8, D7, D6, D5, . . . , D0 = the result of the previous A/D conversion.
A3, A2, A1, A0 = the mux address for the next A/D conversion.
*The 11th SCLK rising edge must occur before the conversion is complete. Otherwise the serial port is thrown out of sync with the microprocessor for the remainder of the transfer.

APPLICATIONS INFORMATION

DESCRIPTION

This example application of the MC145053 ADC interfaces four analog signals to a microprocessor.

Figure 15 illustrates how the MC145053 is used as a cost-effective means to simplify this type of circuit design. Utilizing one ADC, four analog inputs are interfaced to a CMOS or NMOS microprocessor with a serial peripheral interface (SPI) port. Processors with National Semiconductor's MICROWIRE serial port may also be used. Full duplex operation optimizes throughput for this system.

DIGITAL DESIGN CONSIDERATIONS

Motorola's MC68HC05C4 CMOS MCU may be chosen to reduce power supply size and cost. The NMOS MCUs may be used if power consumption is not critical. A V_{DD} to V_{SS} 0.1 μF bypass capacitor should be closely mounted to the ADC.

The MC145053 has the end-of-conversion (EOC) signal at output pin 1 to define when data is ready.

ANALOG DESIGN CONSIDERATIONS

Analog signal sources with output impedances of less than 10 kilohms may be directly interfaced to the ADC, eliminating the need for buffer amplifiers. Separate lines connect the V_{ref} and V_{AG} pins on the ADC with the controllers to provide isolation from system noise.

Although not indicated in Figure 15, the V_{ref} and sensor output lines may need to be shielded, depending on their length and electrical environment. This should be verified during prototyping with an oscilloscope. If shielding is required, a twisted pair or foil-shielded wire (not coax) is appropriate for this low frequency application. One wire of the pair or the shield must be V_{AG}.

A reference circuit voltage of 2.5 volts is used for the application shown in Figure 15. However, the reference circuitry may be simplified by tying V_{AG} to system ground and V_{ref} to the system's positive supply. (See Figure 16.)

A bypass capacitor of approximately 0.22 μF across the V_{ref} and V_{AG} pins is recommended. These pins are adjacent on the ADC package which facilitates mounting the capacitor very close to the ADC.

SOFTWARE CONSIDERATIONS

The software flow for acquisition is straightforward. The four analog inputs, AN0 through AN3, are scanned by reading the analog value of the previously addressed channel into the MCU and sending the address of the next channel to be read to the ADC, simultaneously.

The designer utilizing the MC145053 has the end-of-conversion signal (at pin 1) to define the conversion interval. EOC may be used to generate an interrupt, which is serviced by reading the serial data from the ADC. The software flow should then process and format the data.

When this ADC is used with a 16-bit (2-byte) transfer, there are two types of offsets involved. In the first type of offset, the channel information sent to the ADCs is offset by 12 bits. That is, in the 16-bit stream, only the first 4 bits (4 MSBs) contain the channel information. The balance of the bits are don't cares. This results in 3 don't-care nibbles, as shown in Table 2. The second type of offset is in the conversion result returned from the ADC; this is offset by 6 bits. In the 16-bit stream, the first 10 bits (10 MSBs) contain the conversion result. The last 6 bits are zeroes. The hexadecimal result is shown in the first column of Table 3. The second column shows the result after the offset is removed by a microprocessor routine.

Table 2. Programmer's Guide for 16-Bit Transfers: Input Code

Input Address in Hex	Channel To Be Converted Next	Comment
$0XXX	AN0	Pin 2
$1XXX	AN1	Pin 3
$2XXX	AN2	Pin 4
$3XXX	AN3	Pin 5
$4XXX	AN4	Pin 6
$5XXX	None	Not Allowed
$6XXX	None	Not Allowed
$7XXX	None	Not Allowed
$8XXX	None	Not Allowed
$9XXX	None	Not Allowed
$AXXX	None	Not Allowed
$BXXX	AN5	Half Scale Test: Output = $8000
$CXXX	AN6	Zero Test: Output = $0000
$DXXX	AN7	Full Scale Test: Output = $FFC0
$EXXX	None	Not Allowed
$FXXX	None	Not Allowed

Table 3. Programmer's Guide for 16-Bit Transfers: Output Code

Conversion Result Without Offset Removed	Conversion Result With Offset Removed	Value
$0000	$0000	Zero
$0040	$0001	Zero + 1 LSB
$0080	$0002	Zero + 2 LSBs
$00C0	$0003	Zero + 3 LSBs
$0100	$0004	Zero + 4 LSBs
$0140	$0005	Zero + 5 LSBs
$0180	$0006	Zero + 6 LSBs
$01C0	$0007	Zero + 7 LSBs
$0200	$0008	Zero + 8 LSBs
$0240	$0009	Zero + 9 LSBs
$0280	$000A	Zero + 10 LSBs
$02C0	$000B	Zero + 11 LSBs
•	•	•
•	•	•
•	•	•
$FF40	$03FD	Full Scale-2 LSB
$FF80	$03FE	Full Scale-1 LSB
$FFC0	$03FF	Full Scale

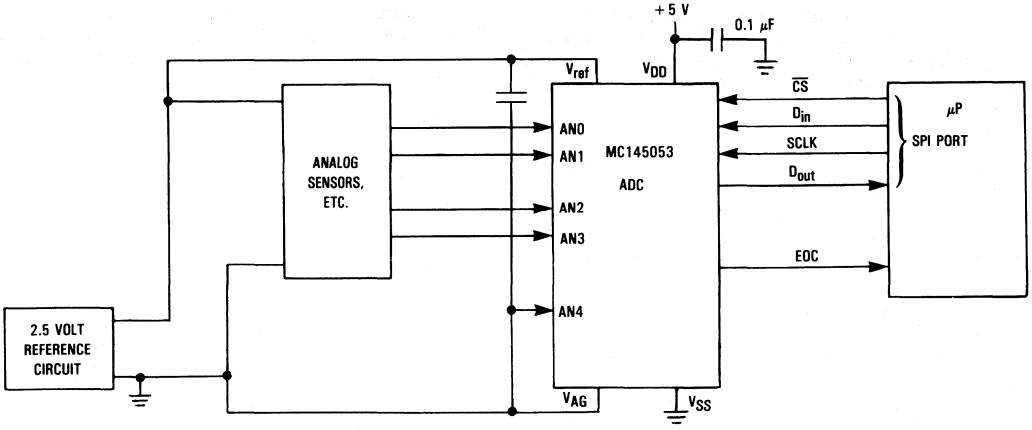


Figure 15. Example Application

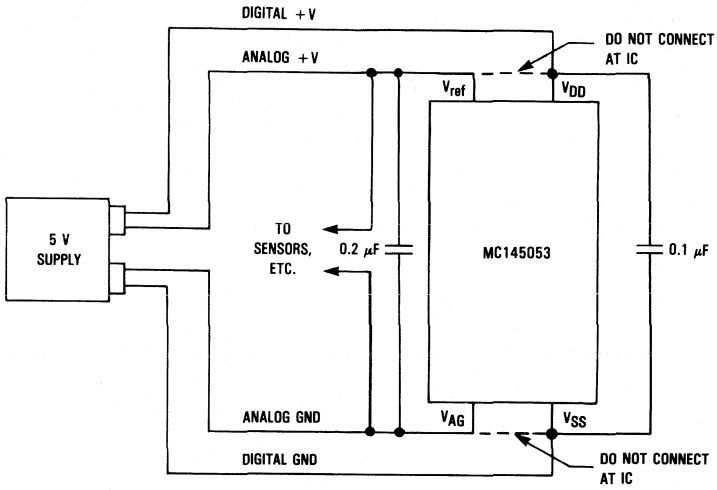


Figure 16. Alternate Configuration Using the Digital Supply for the Reference Voltage

Compatible Motorola MCUs/MPUs

This is not a complete listing of Motorola's MCUs/MPUs. Contact your Motorola representative if you need additional information.

Instruction Set	Memory (Bytes)		SPI ① SCI ②	Device Number
	ROM	EEPROM		
M6805	2096	—	—	MC68HC05C2
	2096	—	Yes	MC68HC05C3
	4160	—	Yes	MC68HC05C4
	4160 ③	—	Yes	MC68HSC05C4
	8K ③	—	Yes	MC68HSC05C8
	4160 ④	—	Yes	MC68HCL05C4
	8K ④	—	Yes	MC68HCL05C8
	7700	—	Yes	MC68HC05C8
	—	4160	—	MC68HC805C4
M68000	—	—	—	MC68HC000

① SPI = Serial Peripheral Interface.

② SCI = Serial Communications Interface.

③ High speed.

④ Low power.

Decoders/Display Drivers

Decoders/Display Drivers

		Page No.
MC14489	Multi-Character LED Display/Lamp Driver	3-3
MC14495-1	Hex-to-7 Segment Latch/Decoder/LED Driver	3-20
MC14499	7-Segment LED Display Decoder/Driver	3-25
MC145000	Serial Input Multiplexed LCD Driver (Master)	3-31
MC145001	Serial Input Multiplexed LCD Driver (Slave)	3-31
MC145453	LCD Driver with Serial Interface	3-42

SELECTOR GUIDE

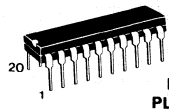
Display Type	Input Format	Drive Capability Per Package	On-Chip Latch	Display Control Inputs	Segment Drive Current	Device Number
LCD-Direct Drive	Serial Binary	33 Elements	Yes		20 μA	**MC145453**
LCD-1/4 Mux	Serial Binary	48 Elements	Yes		200 μA	**MC145000**
		44 Elements	Yes		200 μA	**MC145001**
LED-1/4 Mux	Serial Binary	4 Digits + Decimals	Yes		50 mA (Peak)	**MC14499**
LED-1/5 Mux	Serial Binary	5 Characters + Decimals or 25 Lamps	Yes	Blank, Dim	0 to 35 mA (Peak) Adjustable Current Source	**MC14489**
LED-Direct Drive	Parallel Hex	7 Segments + A thru F Indicator	Yes		10 mA On-Chip Limiting Resistor	**MC14495-1**

MC14489

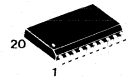
Advance Information

Multi-Character LED Display/Lamp Driver

CMOS



P SUFFIX
PLASTIC DIP
CASE 738



DW SUFFIX
SOG
CASE 751D

ORDERING INFORMATION

MC14489P	Plastic DIP
MC14489DW	SOG Package

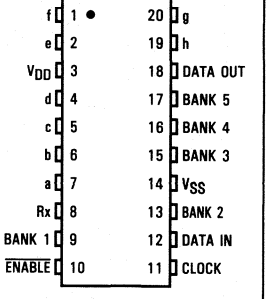
The MC14489 is a flexible light-emitting-diode driver which directly interfaces to individual lamps, 7-segment displays, or various combinations of both. LEDs wired with common cathodes are driven in a muliplexed-by-5 fashion. Communication with an MCU/MPU is established through a synchronous serial port. The MC14489 features data retention plus decode and scan circuitry, thus relieving processor overhead. A single, current-setting resistor is the only ancillary component required.

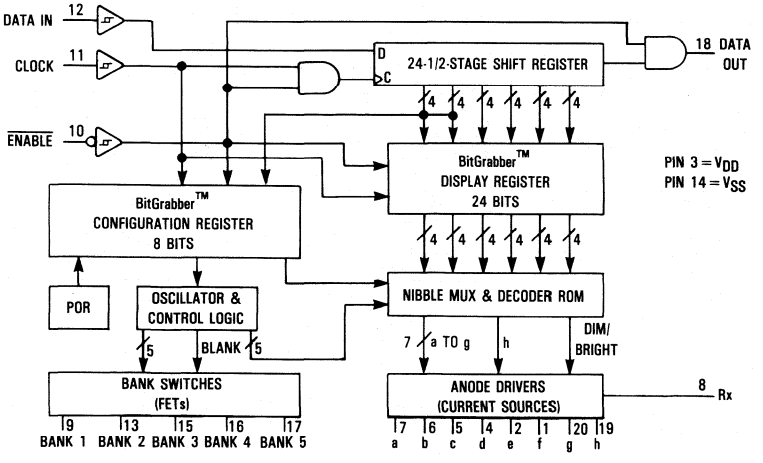
A single device can drive any one of the following: a 5-digit display plus decimals, a 4 1/2-digit display plus decimals and sign, or 25 lamps. A special technique allows driving 5 1/2 digits; see Figure 16. A configuration register allows the drive capability to be partitioned off to suit many additional applications. The on-chip decoder outputs 7-segment-format numerals 0 to 9, hexadecimal characters A to F, plus 15 letters and symbols.

The MC14489 is compatible with the Motorola/RCA SPI and National MICROWIRE serial data ports. The chip's new BitGrabber registers augment the serial interface by allowing random access without steering or address bits. A 24-bit transfer updates the display register. Changing the configuration register requires an 8-bit transfer.

- Operating Voltage Range of Drive Circuitry: 4.5 to 6 V
- Operating Junction Temperature Range: −40° to 130°C
- Current Sources Controlled by Single Resistor Provide Anode Drive
- Low-Resistance FET Switches Provide Direct Common Cathode Interface
- Low-Power Mode (Extinguishes the LEDs) and Brightness Controlled Via Serial Port
- Special Circuitry Minimizes EMI when Display is Driven and Eliminates EMI in Low-Power Mode
- Power-On Reset (POR) Blanks the Display on Power Up
- May Be Used with the New Double-Heterojunction LEDs for Optimum Efficiency
- Chip Complexity: 4300 Elements (FETs, Resistors, Capacitors, etc.)

PIN ASSIGNMENT





BitGrabber is a trademark of Motorola Inc. Patent pending on BitGrabber registers. MICROWIRE is a trademark of National Semiconductor Corp.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS* (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +6.0	V
V_{in}	DC Input Voltage	−0.5 to V_{DD}+0.5	V
V_{out}	DC Output Voltage	−0.5 to V_{DD}+0.5	V
I_{in}	DC Input Current—per Pin (includes Pin 8)	±15	mA
I_{out}	DC Output Current—Pins 1, 2, 4-7, 19, 20 Sourcing	−40	mA
	Sinking	10	
	Pins 9, 13, 15, 16, 17 Sinking	320	
	Pin 18	±15	
I_{DD}, I_{SS}	DC Supply Current, V_{DD} and V_{SS} Pins	±350	mA
T_J	Chip Junction Temperature	−40 to +130	°C
$R_{\theta JA}$	Device Thermal Resistance, Junction-to-Ambient (see Thermal Considerations section) Plastic DIP	90	°C/W
	SOG	100	
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_J = −40° to 130°C★ unless otherwise indicated)

Symbol	Parameter	Test Condition	V_{DD} V	Guaranteed Limit	Unit
V_{DD}	Power Supply Voltage Range of LED Drive Circuitry		—	4.5 to 6.0	V
V_{DD} (stby)	Minimum Standby Voltage	Bits Retained in Display and Configuration Registers, Data Port Fully Functional	—	3.0	V
V_{IL}	Maximum Low-Level Input Voltage (Data In, Clock, $\overline{Enable}$)		3.0	0.9	V
			6.0	1.8	
V_{IH}	Minimum High-Level Input Voltage (Data In, Clock, $\overline{Enable}$)		3.0	2.1	V
			6.0	4.2	
V_{Hys}	Minimum Hysteresis Voltage (Data In, Clock, $\overline{Enable}$)		3.0	0.2	V
			6.0	0.4	
V_{OL}	Maximum Low-Level Output Voltage (Data Out)	I_{out} = 20 μA	3.0	0.1	V
			6.0	0.1	
		I_{out} = 1.3 mA	4.5	0.4	
V_{OH}	Minimum High-Level Output Voltage (Data Out)	I_{out} = −20 μA	3.0	2.9	V
			6.0	5.9	
		I_{out} = −800 μA	4.5	4.1	
I_{in}	Maximum Input Leakage Current (Data In, Clock, $\overline{Enable}$)	$V_{in} = V_{DD}$ or V_{SS}	6.0	±2.0	μA
		$V_{in} = V_{DD}$ or V_{SS}, T_J = 25°C only	6.0	±0.1	
I_{OL}	Minimum Sinking Current (a, b, c, d, e, f, g, h)	V_{out} = 1.0 V	4.5	0.2	mA
I_{OH}	Peak Sourcing Current (See Fig. 9 for currents up to 35 mA) (a, b, c, d, e, f, g, h)	Rx = 2.0 kΩ, V_{out} = 3.0 V, Dimmer Bit = High	5.0	13 to 17.5	mA
		Rx = 2.0 kΩ, V_{out} = 3.0 V, Dimmer Bit = Low	5.0	6 to 9	
I_{OZ}	Maximum Output Leakage Current (Bank 1, Bank 2, Bank 3, Bank 4, Bank 5)	$V_{out} = V_{DD}$ (FET Leakage)	6.0	50	μA
		$V_{out} = V_{DD}$ (FET Leakage), T_J = 25°C only	6.0	1	
		$V_{out} = V_{SS}$ (Protection Diode Leakage)	6.0	1	
R_{on}	Maximum ON Resistance (Bank 1, Bank 2, Bank 3, Bank 4, Bank 5)	I_{out} = 0 to 200 mA	5.0	10	Ω
I_{DD}, I_{SS}	Maximum Quiescent Supply Current	Device in Low-Power Mode, $V_{in} = V_{SS}$ or V_{DD}, Rx in Place, Outputs Open	6.0	100	μA
		Same as Above, T_J = 25°C	6.0	20	
I_{ss}	Maximum RMS Operating Supply Current (The V_{SS} leg does not contain the Rx current component. See Pin Descriptions.)	Device NOT in Low-Power Mode, $V_{in} = V_{SS}$ or V_{DD}, Outputs Open	6.0	1.5	mA

★ See Thermal Considerations section.

AC ELECTRICAL CHARACTERISTICS ($T_J = -40°$ to 130°C ★, $C_L = 50$ pF, Input $t_r = t_f = 10$ ns)

Symbol	Parameter	V_{DD} V	Guaranteed Limit	Unit
f_{clk}	Serial Data Clock Frequency, Single Device or Cascaded Devices NOTE: Refer to Clock t_w below (Figure 1)	3.0 4.5 6.0	dc to 3.0 dc to 4.0 dc to 4.0	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Data Out (Figures 1 and 5)	3.0 4.5 6.0	140 80 80	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Data Out (Figures 1 and 5)	3.0 4.5 6.0	70 50 50	ns
f_R	Refresh Rate—Bank 1 through Bank 5 (Figures 2 and 6)	3.0 4.5 6.0	NA 700 to 1900 700 to 1900	Hz
C_{in}	Maximum Input Capacitance—Data In, Clock, $\overline{\text{Enable}}$	—	10	pF

★ See Thermal Considerations section.

TIMING REQUIREMENTS ($T_J = -40°$ to 130°C ★, Input $t_r = t_f = 10$ ns unless otherwise indicated)

Symbol	Parameter	V_{DD} V	Guaranteed Limit	Unit
t_{su}, t_h	Minimum Setup and Hold Times, Data In versus Clock (Figure 3)	3.0 4.5 6.0	50 40 40	ns
t_{su}, t_h, t_{rec}	Minimum Setup, Hold,* and Recovery Times, $\overline{\text{Enable}}$ versus Clock (Figure 4)	3.0 4.5 6.0	150 100 100	ns
$t_{w(L)}$	Minimum Active-Low Pulse Width, $\overline{\text{Enable}}$ (Figure 4)	3.0 4.5 6.0	4.5 3.4 3.4	μs
$t_{w(H)}$	Minimum Inactive-High Pulse Width, $\overline{\text{Enable}}$ (Figure 4)	3.0 4.5 6.0	300 150 150	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	3.0 4.5 6.0	167 125 125	ns
t_r, t_f	Maximum Input Rise and Fall Times—Data In, Clock, $\overline{\text{Enable}}$ (Figure 1)	3.0 4.5 6.0	1 1 1	ms

★ See Thermal Considerations section.

* For a high-speed 8-Clock access, t_h for $\overline{\text{Enable}}$ is determined as follows.
$V_{DD} = 3$ to 4.5 V, $f_{clk} > 1.78$ MHz: $t_h = 4350 - (7500/f_{clk})$
$V_{DD} = 4.5$ to 6 V, $f_{clk} > 2.34$ MHz: $t_h = 3300 - (7500/f_{clk})$
where t_h is in ns and f_{clk} is in MHz.

NOTES:
1. This restriction does NOT apply for f_{clk} rates less than those listed above. For "slow" f_{clk} rates, use the t_h limits in the above table.
2. This restriction does NOT apply for an access involving more than 8 Clocks. For >8 Clocks, use the t_h limits in the above table.

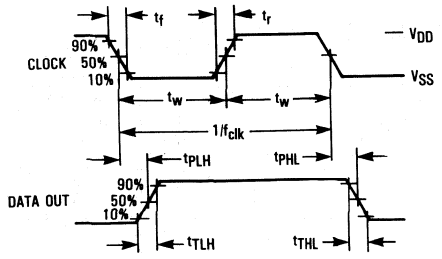


Figure 1

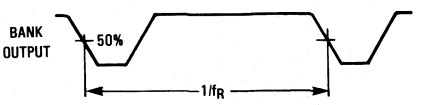


Figure 2

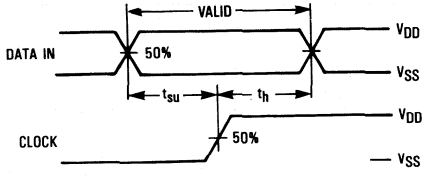


Figure 3

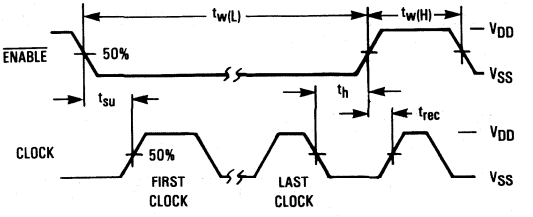
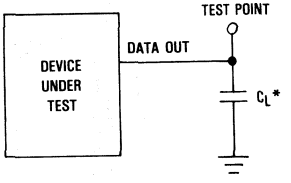
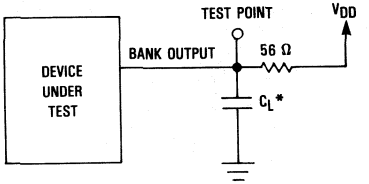


Figure 4



*Includes all probe and jig capacitance.

Figure 5. Test Circuit



*Includes all probe and jig capacitance.

Figure 6. Test Circuit

PIN DESCRIPTIONS

DIGITAL INTERFACE

Data In (Pin 12)

Serial Data Input. The bit stream begins with the MSB and is shifted in on the low-to-high transition of Clock. When the device is not cascaded, the bit pattern is either 1 byte (8 bits) long to change the configuration register or 3 bytes (24 bits) long to update the display register. For two chips cascaded, the pattern is either 4 or 6 bytes, respectively. The display does not flicker during shifting which allows slow serial data rates, if desired.

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the two registers. Random access of either register is provided. That is, the registers may be accessed in any sequence. Data is retained in the registers over a supply range of 3 to 6 V. The format is shown in Figures 7 and 8. Information on the segment decoder is given in Table 1.

Data In typically switches near 50% of V_{DD} and has a Schmitt-triggered input buffer. These features combine to maximize noise immunity for use in harsh environments and bus applications. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail-to-rail. When interfacing to NMOS or TTL devices, either a level shifter (MC14504B, MC74HCT04A) or pullup resistor of 1 kΩ to 10 kΩ must be used. Parameters to be considered when sizing the resistor are the worst-case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Clock (Pin 11)

Serial Data Clock Input. Low-to-high transitions on Clock shift bits available at Data In, while high-to-low transitions shift bits from Data Out. The chip's 24-1/2-stage shift register is static, allowing clock rates down to dc in a continuous or

intermittent mode. The Clock input does not need to be synchronous with the on-chip clock oscillator which drives the multiplexing circuit.

Eight clock cycles are required to access the configuration register, while 24 are needed for the display register when the MC14489 is not cascaded. See Figures 7 and 10.

As shown in Figure 11, two devices may be cascaded. In this case, 32 clock cycles access the configuration register and 48 access the display register, as depicted in Figure 8.

Cascading of 3, 4, and 5 devices is shown in Figures 12, 13, and 14, respectively.

Clock typically switches near 50% of V_{DD} and has a Schmitt-triggered input buffer. Slow Clock rise and fall times are tolerated. See the last paragraph of **Data In** for more information.

$\overline{\text{Enable}}$ (Pin 10)

Active-Low Enable Input. This pin allows the MC14489 to be used on a serial bus, sharing Data In and Clock with other peripherals. When $\overline{\text{Enable}}$ is in an inactive high state, Data Out is forced to a known (low) state, shifting is inhibited, and the port is held in the initialized state. To transfer data to the device, $\overline{\text{Enable}}$ (which initially must be inactive high) is taken low, a serial transfer is made via Data In and Clock, and $\overline{\text{Enable}}$ is taken high. The low-to-high transition on $\overline{\text{Enable}}$ transfers data to either the configuration or display register, depending on the data stream length.

CAUTION

Transitions on $\overline{\text{Enable}}$ must not be attempted while Clock is high.

This input is also Schmitt-triggered and switches near 50% of V_{DD}, thereby minimizing the chance of loading erroneous data in the registers. See the last paragraph of **Data In** for more information.

Data Out (Pin 18)

Serial Data Output. Data is transferred out of the shift register through Data Out on the high-to-low transition of Clock. This output is a no connect, unless used in one of the manners discussed below.

When cascading MC14489s, Data Out feeds Data In of the next device per Figures 11, 12, 13, and 14.

Data Out could be fed back to an MCU/MPU to perform a wrap-around test of serial data. This could be part of a system check conducted at power up to test the integrity of the system's processor, pc board traces, solder joints, etc.

The pin could be monitored at an in-line Q.A. test during board manufacturing.

Finally, Data Out facilitates troubleshooting a system.

DISPLAY INTERFACE

Rx (Pin 8)

External Current-Setting Resistor. A resistor tied between this pin and ground (V_{SS}) determines the peak segment drive current delivered at pins a through h. Pin 8's resistor ties into a current mirror with an approximate current gain of 10 when bit D23 = high (brighten). With D23 = low, the peak current is reduced about 50%. Values for Rx range from 700 Ω to infinity. When Rx = ∞ (open circuit), the display is extinguished. For proper current control, resistors having ± 1% tolerance should be used. See Figure 9.

CAUTION

Small Rx values may cause the chip to overheat if precautions are not observed. See **THERMAL CONSIDERATIONS**.

a through h (Pins 1, 2, 4–7, 19, 20)

Anode-Driver Current Sources. These outputs are closely-matched current sources which directly tie to the anodes of external discrete LEDs (lamps) or display segment LEDs.

When used with lamps, outputs a, b, c, and d are used to independently control up to 20 lamps. Output h is used to control up to 5 lamps dependently. (See Figure 17.) For lamps, the *No Decode* mode is selected via the configuration register, forcing e, f, and g inactive (low).

When used with segmented displays, outputs a through g drive segments a through g, respectively. Output h is used to drive the decimals. If unused, h must be left open. Refer to Figure 10.

Bank 1 through Bank 5 (Pins 9, 13, 15, 16, 17)

Diode-Bank FET Switches. These outputs are low-resistance switches to ground (V_{SS}) capable of handling currents of up to 320 mA. These pins directly tie to the common cathodes of segmented displays or the cathodes of lamps (wired with cathodes common).

The display is refreshed at a nominal 1 kHz rate to achieve optimum brightness from the LEDs. A 20% duty cycle is utilized.

Special design techniques are used on-chip to accommodate the high currents with low EMI (electromagnetic interference) and minimal spiking on the power lines.

POWER SUPPLY

V_{SS} (Pin 14)

Most-negative supply potential. This pin is usually ground.

Resistor Rx is externally tied to ground (V_{SS}). Therefore, the chip's V_{SS} pin does not contain the Rx current component.

V_{DD} (Pin 3)

Most-positive supply potential.

To guarantee data integrity in the registers and to ensure the serial interface is functional, this voltage may range from 3 to 6 volts with respect to V_{SS}. For example, within this voltage range, the chip could be placed in and out of the low-power mode.

To adequately drive the LEDs, this voltage must be 4.5 to 6 volts with respect to V_{SS}.

The V_{DD} pin contains the Rx current component plus the chip's current drain. In the low-power mode, the current mirror and clock oscillator are turned off, thus significantly reducing the V_{DD} current, I_{DD}.

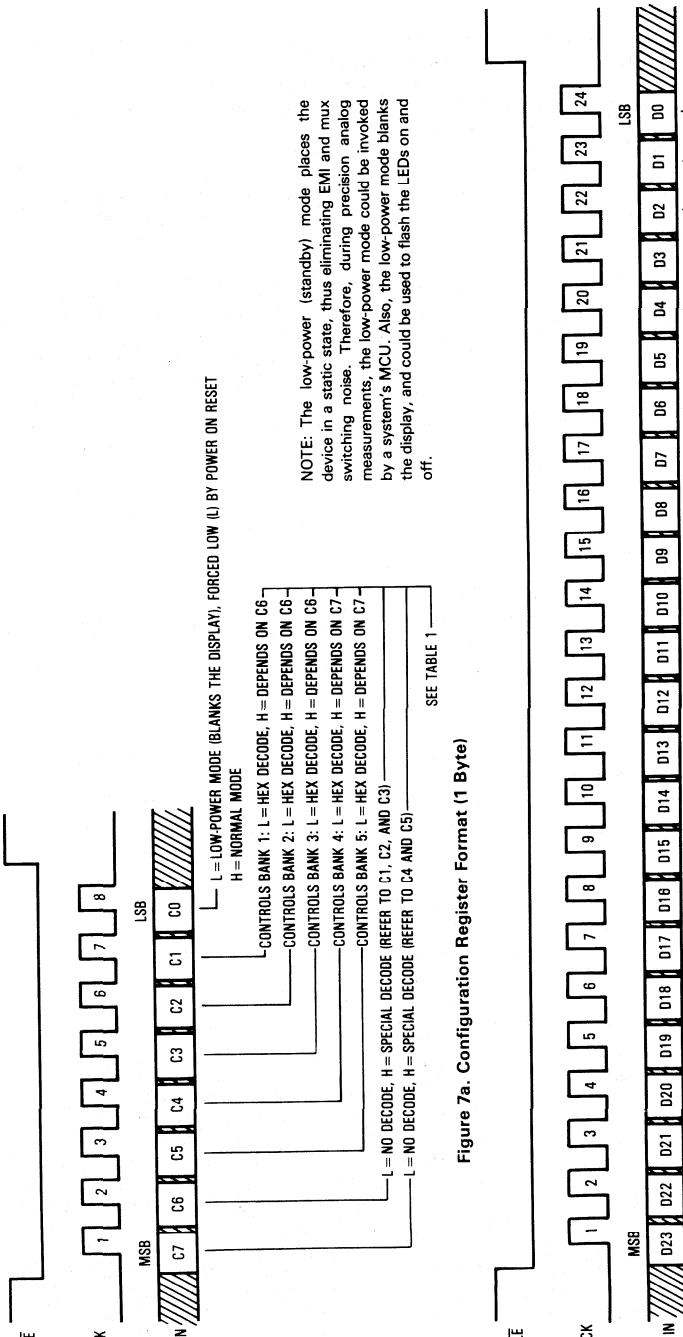


Figure 7a. Configuration Register Format (1 Byte)

Figure 7b. Display Register Format (3 Bytes)

NOTE: L = Low Voltage Level (Logic 0), H = High Voltage Level (Logic 1)

Figure 7. Timing Diagrams for Non-Cascaded Devices

Table 1. Triple-Mode Segment Decoder Function Table

Bank Nibble Value			7-Segment Display Characters		Lamp Conditions: No Decode (1) (Invoked via Bits C1 to C7)			
Hexadecimal	Binary MSB LSB		Hex Decode (Invoked via Bits C1 to C5)	Special Decode (Invoked via Bits C1 to C7)	d	c	b	a
$0	L L L L		0					
$1	L L L H		1	c				on
$2	L L H L		2	H			on	
$3	L L H H		3	h			on	on
$4	L H L L		4	J		on		
$5	L H L H		5 (2)	L		on		on
$6	L H H L		6	n		on	on	
$7	L H H H		7	o		on	on	on
$8	H L L L		8 (3)	P	on			
$9	H L L H		9 (4)	r	on			on
$A	H L H L		A	U	on		on	
$B	H L H H		b	u	on		on	on
$C	H H L L		C	y	on	on		
$D	H H L H		d	-	on	on		on
$E	H H H L		E	=	on	on	on	
$F	H H H H		F	o	on	on	on	on

(1) In the *No Decode* mode, outputs e, f, and g are unused and are all forced inactive (low). Output h's decoding is unaffected, i.e., unchanged from the other modes. The *No Decode* mode is used for three purposes:
1. Individually controlling lamps.
2. Controlling a half digit with sign.
3. Controlling annunciators—examples: AM, PM, UHF, kV, mm Hg.

(2) Can be used as "cap S".

(3) Can be used as "cap B".

(4) Can be used as "small g".

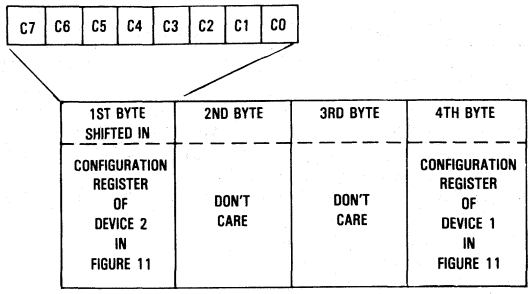


Figure 8a. Configuration Registers

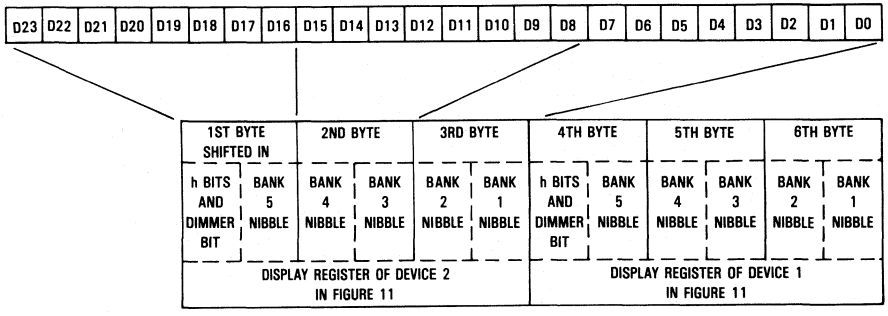


Figure 8b. Display Registers

NOTE: $\overline{\text{ENABLE}}$ (which initially must be inactive high) is kept active-low during the entire 4-byte configuration transfer or 6-byte display transfer. When $\overline{\text{ENABLE}}$ is brought back high, either a 4- or 6-byte transfer occurs in the cascaded devices, depending on the number of bytes in the transfer.

Figure 8. Bit Stream Formats for Two Devices Cascaded

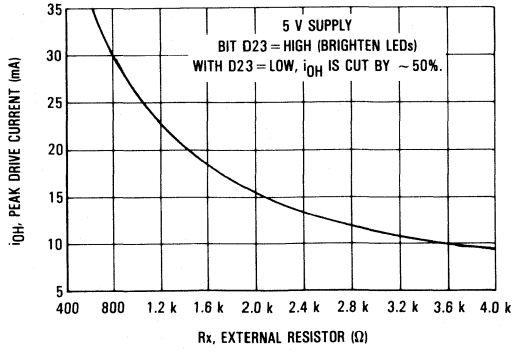


Figure 9. a through h Nominal Current versus Rx

APPLICATIONS INFORMATION

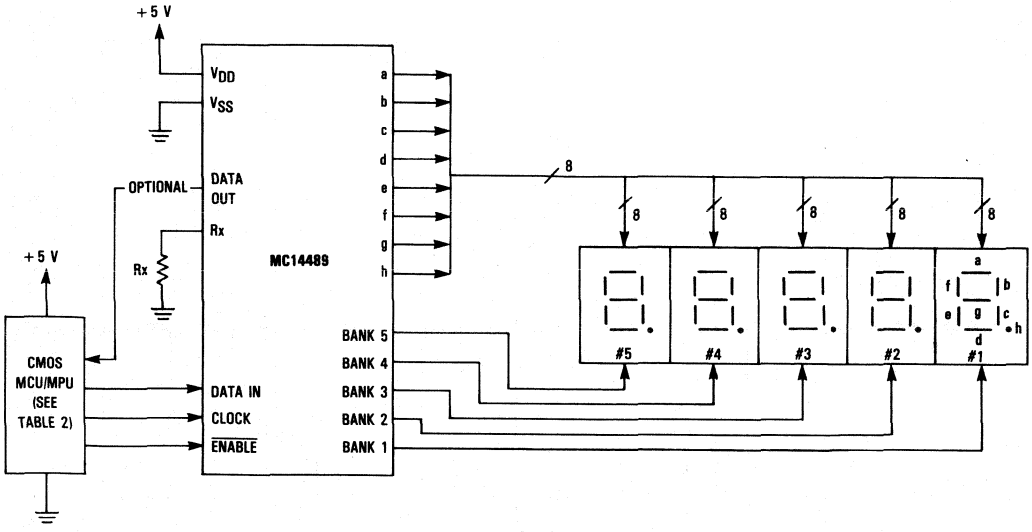


Figure 10. Non-Cascaded Application Example: 5 Character Common Cathode LED Display with Two Intensities as Controlled via Serial Port

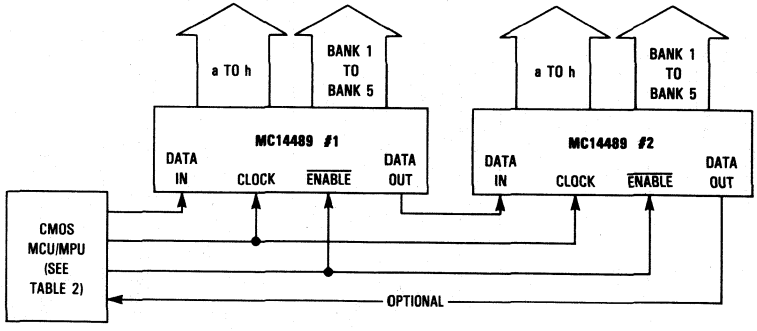


Figure 11. Cascading Two Devices

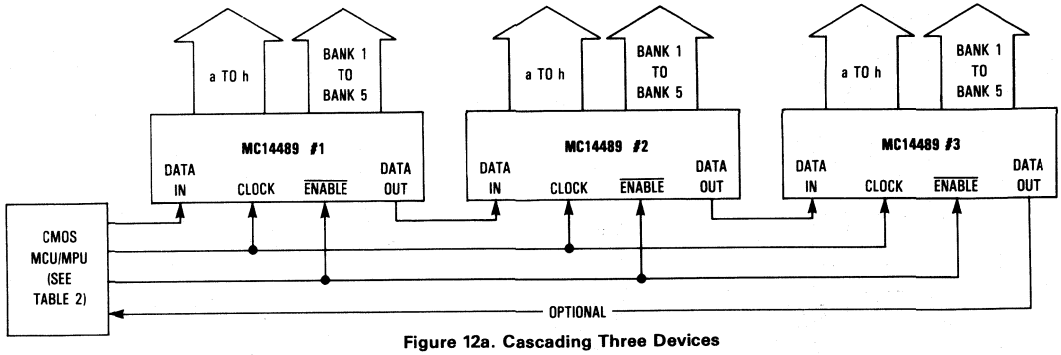


Figure 12a. Cascading Three Devices

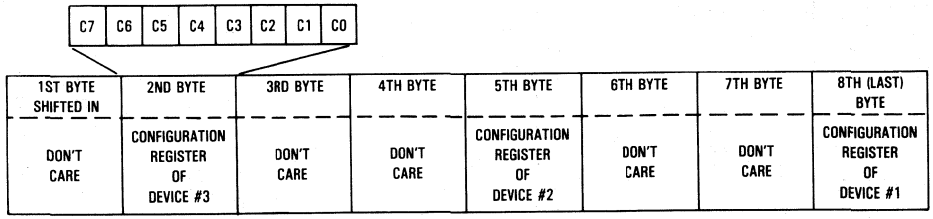


Figure 12b. Configuration Registers

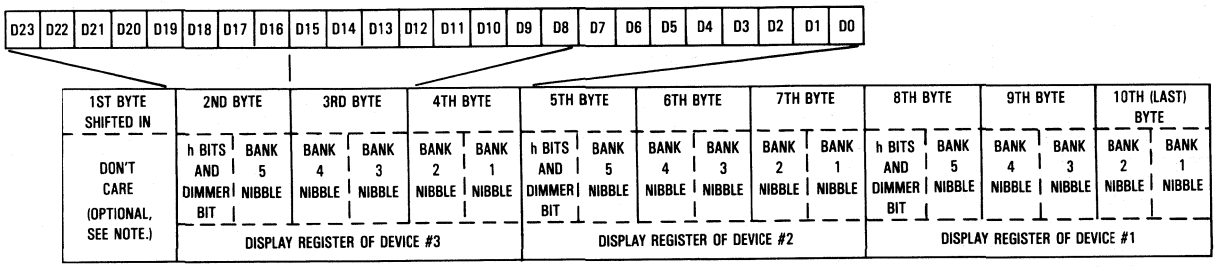


Figure 12c. Display Registers

NOTE: When the "don't care" bytes are included, $\overline{\text{ENABLE}}$ (which initially must be inactive high) is kept active-low during the entire 8-byte configuration transfer or 10-byte display transfer. When $\overline{\text{ENABLE}}$ is brought back high, either an 8- or 10-byte transfer occurs in the cascaded devices. Alternatively, when updating the display registers, the one "don't care" byte can be eliminated as follows: (1) take $\overline{\text{ENABLE}}$ active low, (2) transfer 6 bytes, (3) pulse $\overline{\text{ENABLE}}$ inactive high, see $t_{W(H)}$ spec, (4) transfer last 3 bytes, and (5) take $\overline{\text{ENABLE}}$ inactive high.

Figure 12. Bit Stream Formats for Three Devices Cascaded

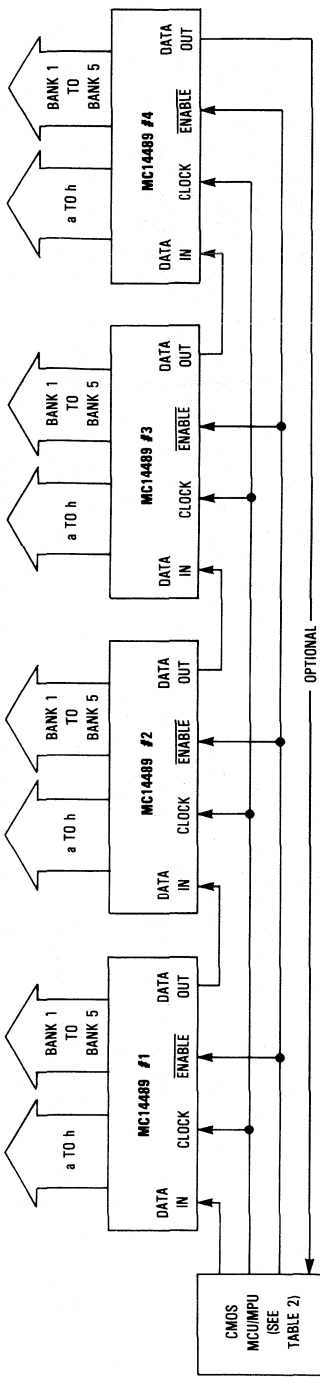


Figure 13a. Cascading Four Devices

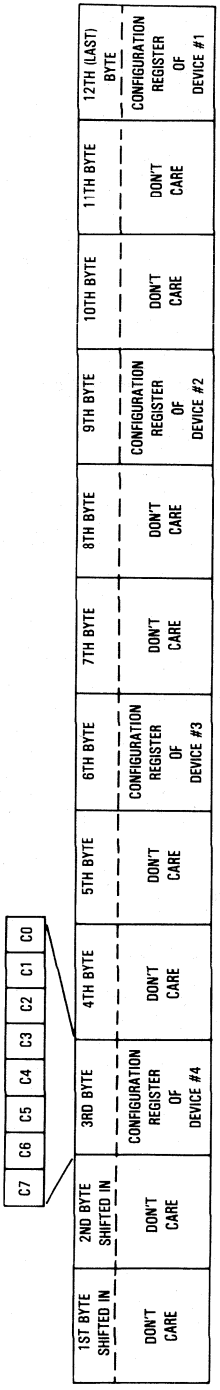


Figure 13b. Configuration Registers

Figure 13c. Display Registers

NOTE: When the "don't care" bytes are included, $\overline{\text{ENABLE}}$ (which initially must be inactive high) is kept active-low during the entire 12-byte configuration transfer or 14-byte display transfer. When $\overline{\text{ENABLE}}$ is brought back high, either a 12- or 14-byte transfer occurs in the cascaded devices. Alternatively, when updating the display registers, the two "don't care" bytes can be eliminated as follows: (1) take $\overline{\text{ENABLE}}$ active low, (2) transfer 6 bytes, (3) pulse $\overline{\text{ENABLE}}$ inactive high, see $t_{w(H)}$ spec, (4) transfer last 6 bytes, and (5) take $\overline{\text{ENABLE}}$ inactive high.

Figure 13. Bit Stream Formats for Four Devices Cascaded

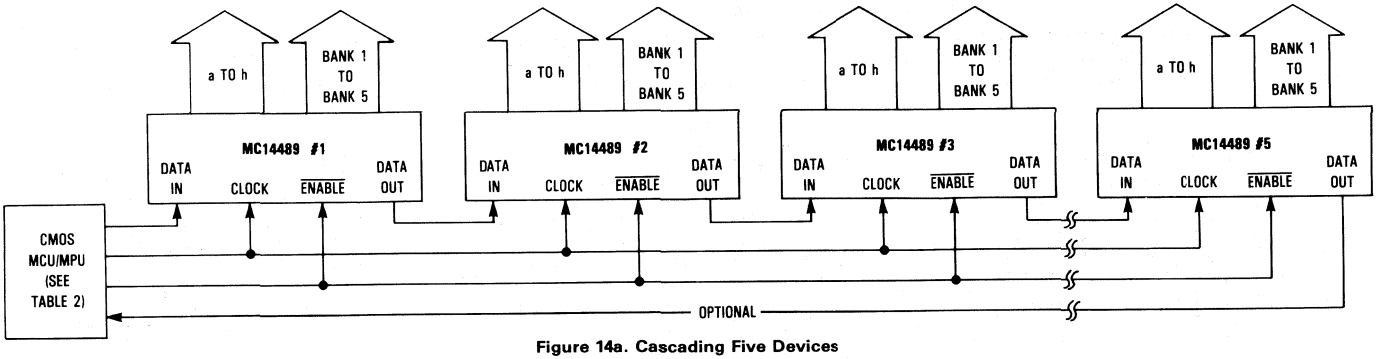


Figure 14a. Cascading Five Devices

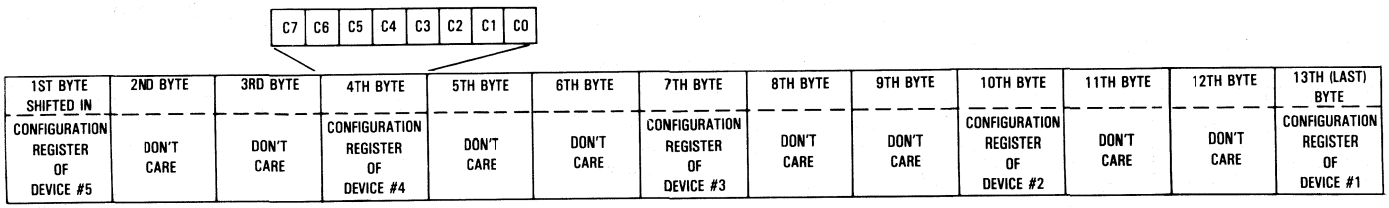


Figure 14b. Configuration Registers

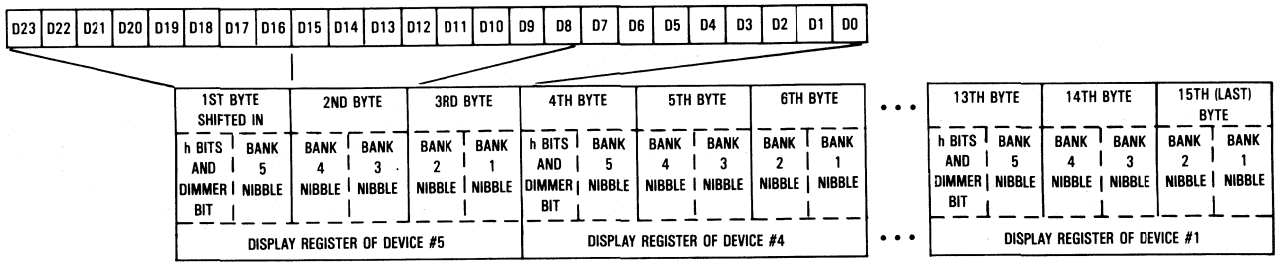
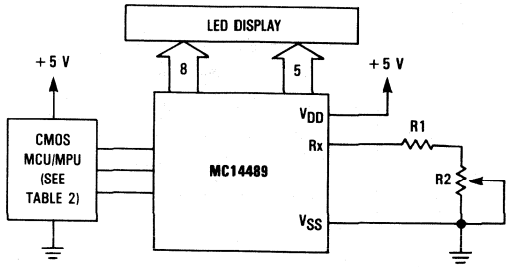


Figure 14c. Display Registers

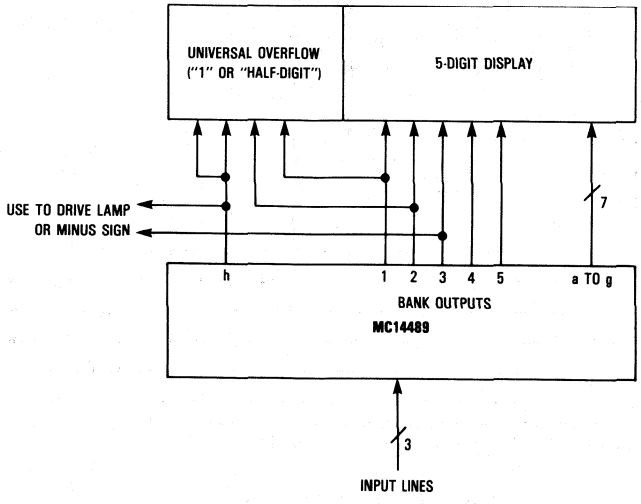
NOTE: $\overline{\text{ENABLE}}$ (which initially must be inactive high) is kept active-low during the entire 13-byte configuration transfer or 15-byte display transfer. When $\overline{\text{ENABLE}}$ is brought back high, either a 13- or 15-byte transfer occurs in the cascaded devices, depending on the number of bytes in the transfer.

Figure 14. Bit Stream Formats for Five Devices Cascaded



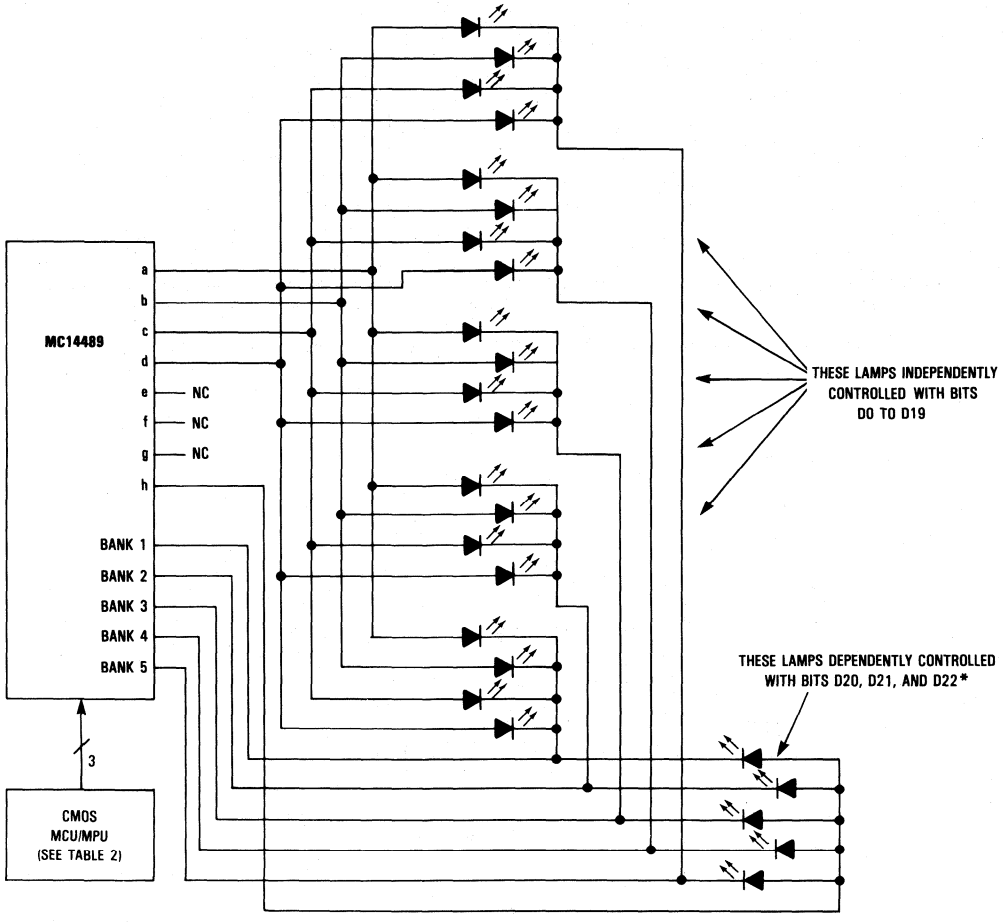
NOTES: R1 limits the maximum current to avoid damaging the display and/or the MC14489 due to overheating. See the Thermal Considerations section. An 1/8 watt resistor may be used for R1. R2 is a 1 kΩ or 5 kΩ potentiometer ($\geq$1/8 watt).

Figure 15. Common-Cathode LED Display with Dial-Adjusted Brightness



NOTE: A Universal Overflow pins out all anodes and cathodes.

Figure 16. Driving 5 1/2 Digits



*If required, this group of lamps can be independently controlled. To accomplish independent control, only connect lamps to BANK 1 and BANK 2 for output h (2 lamps). Then, use bits D20, D21, and D22 for control of these 2 lamps.

Figure 17. 25 Lamp Application

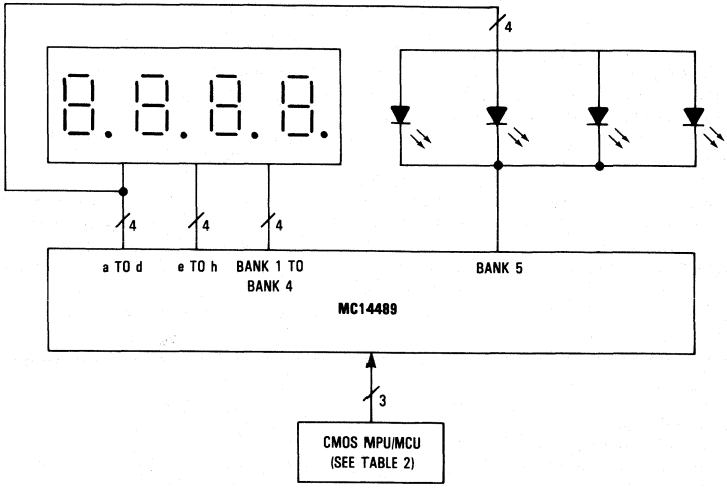


Figure 18. 4-Digit Display Plus Decimals with Four Annunciators or 4 1/2-Digit Display Plus Sign

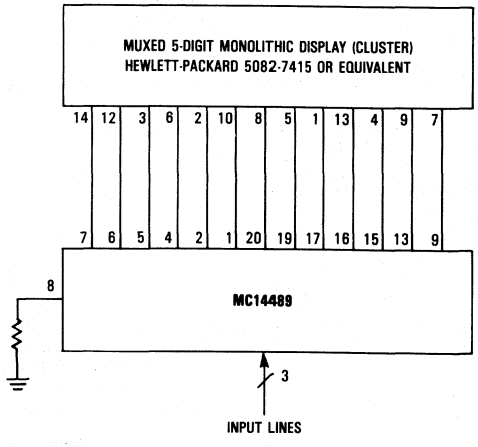


Figure 19. Compact Display System with Three Components

THERMAL CONSIDERATIONS

The MC14489 is designed to operate with a *chip-junction* temperature (T_J) ranging from −40 to 130°C, as indicated in the electrical characteristics tables. The *ambient* operating temperature range (T_A) is dependent on $R_{\theta JA}$, the internal chip current, how many anode drivers are used, the number of bank drivers used, the drive current, and how the package is cooled. The maximum ratings table gives the thermal resistance, junction-to-ambient, of the MC14489 mounted on a pc board using natural convection to be 90°C per watt for the plastic DIP. The SOG thermal resistance is 100°C per watt.

The following general equation (1) is used to determine the power dissipated by the MC14489.

$$P_T = P_D + P_I \quad (1)$$

where

P_T = Total power dissipation of the MC14489
P_D = Power dissipated in the driver circuitry (mW)
P_I = Power dissipated by the internal chip circuitry (mW)

The equations for the two terms of the general equation are:

$$P_D = (i_{OH})(N)(V_{DD} - V_{LED})(B/5) \quad (2)$$

$$P_I = (1.5\text{ mA})(V_{DD}) + I_{Rx}(V_{DD} - I_{Rx}R_x) \quad (3)$$

where

i_{OH} = Peak anode driver current (mA)
$I_{Rx} \approx i_{OH}/10$, with i_{OH} = the peak anode driver current (mA) when the dimmer bit is high
N = Number of anode drivers used
B = Number of bank drivers used
R_x = External resistor value (kΩ)
V_{DD} = Maximum supply voltage, referenced to V_{SS} (volts)
V_{LED} = Minimum anticipated voltage drop across the LED
1.5 mA = Operating supply current of the MC14489

The following two examples show how to calculate the maximum allowable ambient temperature.

Worst-Case Analysis Example 1:

5-digit display with decimals (5 banks and 8 anode drivers)
DIP without heat sink on PC board
$i_{OH} = 20$ mA max
$V_{LED} = 1.8$ V min
$V_{DD} = 5.25$ V max

$P_D = (20)(8)(5.25 - 1.8)(5/5) = 552$ mW Ref. (2)

$P_I = (1.5)(5.25) + 2[5.25 - 2(2)] = 10$ mW Ref. (3)

Therefore, $P_T = 552 + 10 \approx 562$ mW Ref. (1)

and $\Delta T_{chip} = R_{\theta JA}P_T = (90°C/W)(0.562) = 51°C$

Finally, the maximum allowable $T_A = T_J\text{max} - \Delta T_{chip} = 130 - 51 = 79°C$

That is, if $T_A = 79°C$, the maximum junction temperature is 130°C. The chip's average temperature for this example is lower than 130°C because all segments are usually not illuminated simultaneously for an indefinite period.

Worst-Case Analysis Example 2:

16 lamps (4 banks and 4 anode drivers)
SOG without heat sink on PC board
$i_{OH} = 30$ mA max
$V_{LED} = 1.8$ V min
$V_{DD} = 5.5$ V max

$P_D = (30)(4)(5.5 - 1.8)(4/5) = 355$ mW Ref. (2)

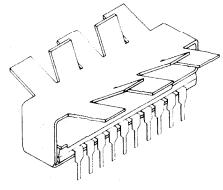
$P_I = (1.5)(5.5) + 3[5.5 - 3(1.0)] = 16$ mW Ref. (3)

Therefore, $P_T = 355 + 16 \approx 371$ mW Ref. (1)

and $\Delta T_{chip} = R_{\theta JA}P_T = (100°C/W)(0.371) = 37°C$

Finally, the maximum allowable $T_A = T_J\text{max} - \Delta T_{chip} = 130 - 37 = 93°C$

To extend the allowable ambient temperature range or to reduce T_J, which extends chip life, a heat sink such as shown in Figure 20 can be used in high-current applications. Alternatively, heat-spreader techniques can be used on the PC board, such as running a wide trace under the MC14489 and using thermal paste. Wide, radial traces from the MC14489 leads also act as heat spreaders.



AAVID #5804 or equivalent
(Tel. 603/524-4443, TWX 510/298-1127)
Motorola cannot recommend one supplier over another and in no way suggests that this is the only heat sink supplier.

Figure 20. Heat Sink

Table 2. Compatible Motorola MCUs/MPUs

This is not a complete listing of Motorola's MCUs/MPUs. Contact your Motorola representative if you need additional information.

Instruction Set	Memory (Bytes)		SPI ① SCI ②	A/D ③	Device Number
	ROM	EEPROM			
M68HC11	—	—	Yes	Yes	MC68HC11A0
	—	512	Yes	Yes	MC68HC11A1
	—	2048	Yes	Yes	MC68HC811A2
	8192	512	Yes	Yes	MC68HC11A8
	12 K	512	Yes	Yes	MC68HC11E9
M6805	2096	—	—	—	MC68HC05C2
	2096	—	Yes	—	MC68HC05C3
	4160	—	Yes	—	MC68HC05C4
	4160 ④	—	Yes	—	MC68HSC05C4
	8K ④	—	Yes	—	MC68HSC05C8
	4160 ⑤	—	Yes	—	MC68HCL05C4
	8K ⑤	—	Yes	—	MC68HCL05C8
	7700	—	Yes	—	MC68HC05C8
	—	4160	—	—	MC68HC805C4
M68000	—	—	—	—	MC68HC000

① SPI = Serial Peripheral Interface.

② SCI = Serial Communications Interface.

③ A/D = Analog-to-Digital Converter.

④ High speed.

⑤ Low power.

Table 3. LED Lamp and Common-Cathode Display Manufacturers

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of LED suppliers.

Supplier	Contact Information
General Instruments (GI), Optoelectronics Division	Phone: (415) 493-0400 TWX/TLX: 470208 FAX: (415) 493-7055
Hewlett-Packard (HP), Components Group	Contact your local H-P Components Sales Office
Industrial Electronic Engineers (IEE), Component Products Div.	Phone: (818) 787-0311 TLX: 4720556 FAX: (818) 902-3723
William J. Purdy Co., AND Division	Phone: (415) 347-9916 MCI/TLX: 677-1439 FAX: (415) 340-1670

MC14495-1

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

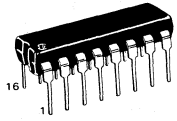
HEXADECIMAL-TO-SEVEN SEGMENT LATCH/DECODER LED DRIVER

HEXADECIMAL-TO-SEVEN SEGMENT LATCH/ DECODER LED DRIVER

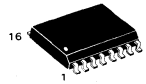
The MC14495-1 is constructed with CMOS enhancement-mode devices and NPN bipolar output drivers in a monolithic structure. The circuit provides the functions of a 4-bit storage latch. The decoder is implemented utilizing a mask-programmable ROM. With a 5-volt power supply, it can be used without resistor interface to drive seven segment LEDs. The series output resistors of, typically, 290 ohms are internal to the device.

Applicatons include MPU systems display driver, instrument display driver, computer/calculator display driver, clockpit display driver, and various clock, watch, and timer uses.

- Low Logic-Circuit Power Dissipation
- High Current-Sourcing Outputs with Internal Limiting Resistors
- Latch Storage of Code
- Supply Voltage Range = 4.5 to 18 V
- CMOS Input Switching Levels
- Standard ROM Provides Hex-to-Seven Segment Decoding
- Other ROM Options Available Upon Request (Contact your Motorola Sales Office)
- Chip Complexity: 187 FETs plus 9 NPNs or 49 Equivalent Gates



P SUFFIX
PLASTIC DIP
CASE 648

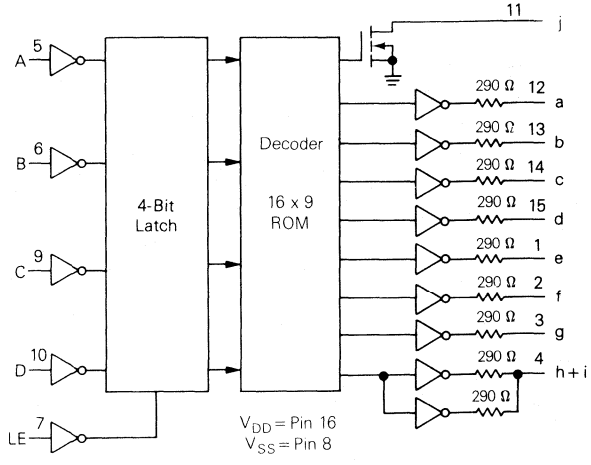


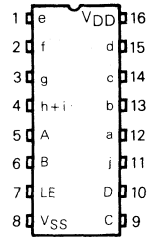
DW SUFFIX
SOG
CASE 751G

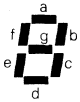
ORDERING INFORMATION

MC14495P1	Plastic DIP
MC14495DW1	SOG Package

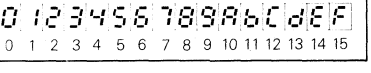
BLOCK DIAGRAM







ALPHANUMERIC DISPLAY



TRUTH TABLE (LE = Low)

INPUTS				OUTPUTS								
D	C	B	A	a	b	c	d	e	f	g	h+i	j	DISPLAY
0	0	0	0	1	1	1	1	1	1	0	0	Open	0
0	0	0	1	0	1	1	0	0	0	0	0	Open	1
0	0	1	0	1	1	0	1	1	0	1	0	Open	2
0	0	1	1	1	1	1	1	0	0	1	0	Open	3
0	1	0	0	0	1	1	0	0	1	1	0	Open	4
0	1	0	1	1	0	1	1	0	1	1	0	Open	5
0	1	1	0	1	0	1	1	1	1	1	0	Open	6
0	1	1	1	1	1	1	0	0	0	0	0	Open	7
1	0	0	0	1	1	1	1	1	1	1	0	Open	8
1	0	0	1	1	1	1	1	0	1	1	0	Open	9
1	0	1	0	1	1	1	0	1	1	1	1	Open	A
1	0	1	1	0	0	1	1	1	1	1	1	Open	b
1	1	0	0	1	0	0	1	1	1	0	1	Open	C
1	1	0	1	0	1	1	1	1	0	1	1	Open	d
1	1	1	0	1	0	0	1	1	1	1	1	Open	E
1	1	1	1	1	0	0	0	1	1	1	1	0	F

MAXIMUM RATINGS (Voltages referenced to V_{SS}).

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	V
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	V
DC Current Drain per Input Pin	I	10	mA
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Maximum Continuous Output Power (Source) per Output @ 25°C Pins 1, 2, 3, 12, 13, 14, 15 Pin 4	P_{OHmax}‡	 50 100	mW

‡ $P_{OHmax} = I_{OH}(V_{DD}-V_{OH})$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

ELECTRICAL CHARACTERISTICS (Voltages referenced to V_{SS})

Characteristic	Symbol	V_{DD} V	−40°C Min	−40°C Max	25°C Min	25°C Typ#	25°C Max	85°C Min	85°C Max	Unit
Input Voltage "0" Level	V_{IL}									V
(V_O = 3.8 or 0.5 V)		5	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 8.8 or 1.0 V)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.8 or 1.5 V)		15	–	4.0	–	6.00	4.0	–	4.0	
(V_O = 0.5 or 3.8 V) "1" Level	V_{IH}	5	3.5	–	3.5	2.75	–	3.5	–	V
(V_O = 1.0 or 8.8 V)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.8 V)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Voltage: a − g, h + i	V_{OL}	5	–	0.1	–	0	0.05	–	0.05	V
$V_{in} = V_{DD}$ or 0, $I_{out} = 0\ \mu A$		10	–	0.1	–	0	0.05	–	0.05	
		15	–	0.1	–	0	0.05	–	0.05	
Output Drive Voltage: a − g, h + i	V_{OH}	5								V
(I_{OH} = 0 mA)			4.0	–	4.0	4.8	–	4.0	–	
(I_{OH} = 5 mA)			2.45	–	2.4	3.0	–	2.05	–	
(I_{OH} = 10 mA)			1.3	–	0.8	1.7	–	–	–	
(I_{OH} = 0 mA)		10	9.0	–	9.0	9.8	–	9.0	–	V
(I_{OH} = 5 mA)			7.4	–	7.2	8.0	–	6.9	–	
(I_{OH} = 10 mA)			6.4	–	5.8	6.7	–	5.0	–	
(I_{OH} = 15 mA)			5.3	–	4.4	5.3	–	3.05	–	
(I_{OH} = 0 mA)		15	14.0	–	14.0	14.8	–	14.0	–	V
(I_{OH} = 5 mA)			12.2	–	12.0	13.0	–	11.7	–	
(I_{OH} = 10 mA)			10.9	–	10.4	11.7	–	9.6	–	
(I_{OH} = 15 mA)			9.7	–	8.8	10.3	–	7.45	–	
(I_{OH} = 20 mA)			8.5	–	7.2	8.8	–	5.25	–	
(I_{OH} = 25 mA)			7.4	–	5.6	7.1	–	3.0	–	
Output Sink Current: j	I_{OL}									mA
(V_{OL} = 0.4 V)		5	–	–	0.3	1.00	–	–	–	
(V_{OL} = 0.5 V)		10	–	–	–	–	–	–	–	
(V_{OL} = 1.5 V)		15	–	–	0.5	1.25	–	–	–	
Input Current (L Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μA
Input Current (P Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μA
Input Capacitance	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current	I_{DD}	5	–	0.3	–	0.08	0.25	–	0.2	mA
V_{in} = 0 or V_{DD}, $I_{out} = 0\ \mu A$		10	–	1.5	–	0.40	1.25	–	1.0	
(Per Package)		15	–	3.0	–	0.85	2.50	–	2.0	
Total Supply Current**†	I_T	5	$I_T = (1.9\ \mu A/kHz)f + I_{DD}$							μA
(Dynamic plus Quiescent,		10	$I_T = (3.8\ \mu A/kHz)f + I_{DD}$							
Per Package)		15	$I_T = (5.7\ \mu A/kHz)f + I_{DD}$							
(C_L = 50 pF on all outputs, all buffers switching)										

†To calculate total supply current at loads other than 50 pF: $I_T(C_L = I_T(50\text{ pF}) + 3.5 \times 10^{-3}(C_L - 50)\ V_{DD}f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in V, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

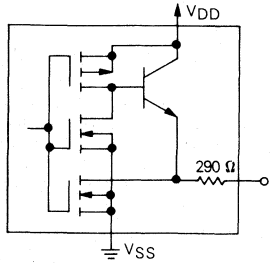
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

SWITCHING CHARACTERISTICS ($C_L = 50$ pF, $T_A = 25°C$)

Characteristic	Symbol	V_{DD} V	Min	Typ#	Max	Unit
Output Rise Time, a–g, h+i Outputs (Figure 1)	t_{TLH}					ns
		5	–	210	450	
		10	–	145	300	
		15	–	90	200	
Output Fall Time, a–g, h+i Outputs (Figure 1)	t_{THL}					μs
		5	–	1.5	3.5	
		10	–	1.3	2.75	
		15	–	1.1	2.25	
Output Fall Time, j Output (Figures 3 and 4)	t_{THL}					ns
		5	–	105	250	
		10	–	40	100	
		15	–	30	75	
Propagation Delay Time, A, B, C, D to a–g, h+i Outputs (Figure 2)	t_{PLH}					ns
		5	–	935	2400	
		10	–	340	900	
		15	–	230	500	
	t_{PHL}	5	–	7.0	18.0	μs
		10	–	3.5	9.0	
		15	–	2.0	5.0	
Propagation Delay Time, A, B, C, D to j Output (Figures 3 and 4)	t_{PLZ}					μs
		5	–	11.0	25.0	
		10	–	8.0	20.0	
		15	–	4.0	10.0	
	t_{PZL}	5	–	800	1500	ns
		10	–	400	1000	
		15	–	200	500	
Propagation Delay Time, LE to a–g, h+i Outputs (Figure 5)	t_{PLH}					ns
		5	–	1300	3000	
		10	–	500	1500	
		15	–	350	1000	
	t_{PHL}	5	–	16.0	30.0	μs
		10	–	6.0	15.0	
		15	–	5.0	10.0	
Propagation Delay Time, LE to j Output (Figures 4 and 6)	t_{PLZ}					μs
		5	–	14.0	30	
		10	–	8.0	20	
		15	–	6.0	15	
	t_{PZL}	5	–	10.0	25	μs
		10	–	5.0	15	
		15	–	4.0	10	
Setup Time, A, B, C, D to LE (Figure 7)	t_{su}	5	100	35	–	ns
		10	65	25	–	
		15	65	25	–	
Hold Time, LE to A, B, C, D (Figure 7)	t_h	5	125	45	–	ns
		10	75	30	–	
		15	75	25	–	
Latch Enable Pulse Width, LE (Figure 7)	t_w	5	525	210	–	ns
		10	200	80	–	
		15	140	55	–	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

OUTPUT CIRCUIT
(Except Pin 11)



INPUT/OUTPUT FUNCTIONS

SEGMENT DRIVER (a, b, c, d, e, f, g, h + i; PINS 12, 13, 14, 15, 1, 2, 3, 4)

The segment drivers are emitter-follower NPN transistors. To limit the output current, a resistor, typically 290 ohms, is integrated internally at each output. Therefore, external resistors are not necessary when driving an LED at the supply voltage of $V_{DD} = 5.0$ volts.

OUTPUT (j; PIN 11)

This open-drain output is activated (goes low) whenever inputs A, B, C, and D are all set to a logic one. Otherwise the output is in the high-impedance state. See the truth table.

INPUT DATA (A, B, C, D; PINS 5, 6, 9, 10)

The inputs A, B, C, and D are fed to a 4-bit latch which is controlled by the Latch Enable input.

LATCH ENABLE (LE; PIN 7)

The data on inputs A, B, C and D will pass through the latch and will be decoded immediately when LE is low. In this mode of operation the circuit is performing the function of a conventional decoder/driver. The data may be loaded into the latch when LE = low and will be latched with the rising edge of LE. The data will remain stored as long as LE is high.

SWITCHING WAVEFORMS

Figure 1

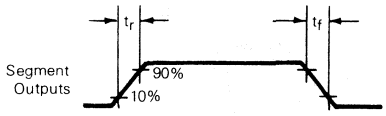


Figure 2

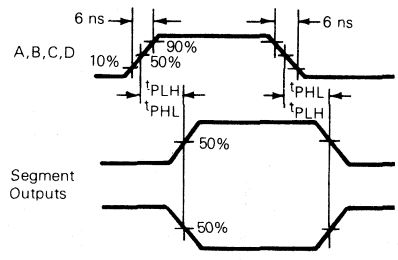


Figure 3

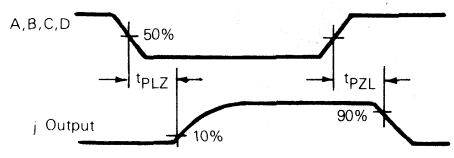


Figure 4

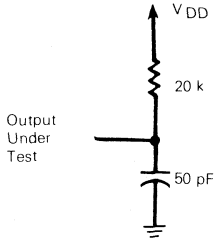
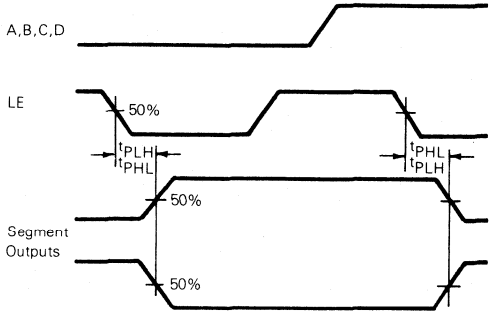


Figure 5



SWITCHING WAVEFORMS

Figure 6

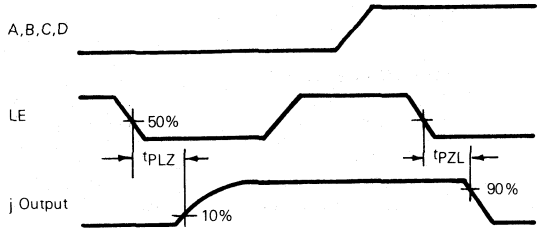
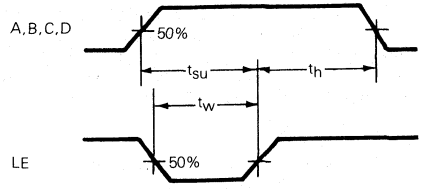
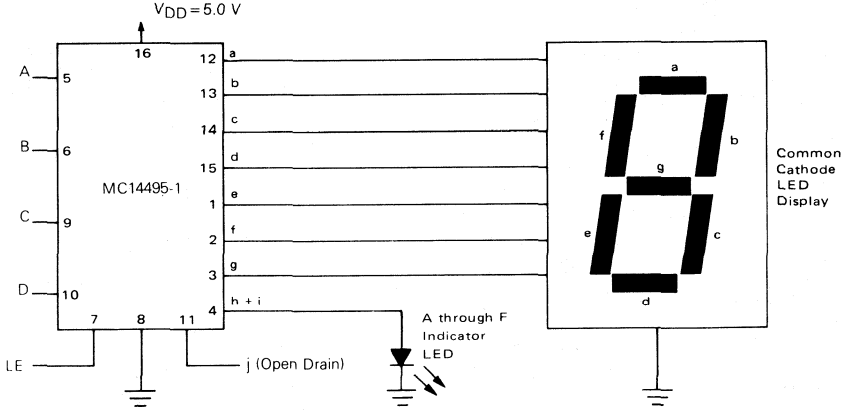


Figure 7



TYPICAL CIRCUIT @ V_{DD} = 5.0 V

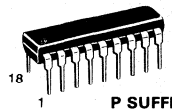


MC14499

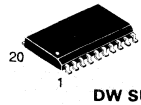
7-Segment LED Display Decoder/ Driver with Serial Interface
CMOS

The MC14499 is a 7-segment alphanumeric LED decoder/driver with a serial interface port to provide communication with CMOS microprocessors and microcomputers. This device features NPN output drivers which allow interfacing to common cathode LED displays through external series resistors.

- High-Current Segment Drivers on Chip
- CMOS MPU Compatible Input Levels
- Wide Operating Voltage Range: 4.5 to 6.5 V
- Operating Temperature Range: 0 to 70°C
- Drives Four Characters with Decimal Points
- Also See MC14489



P SUFFIX
PLASTIC DIP
CASE 707

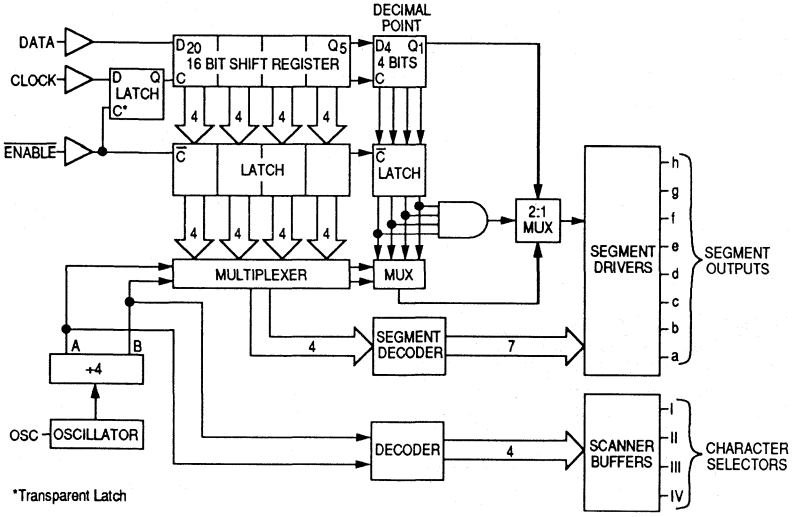


DW SUFFIX
SOG
CASE 751D

ORDERING INFORMATION

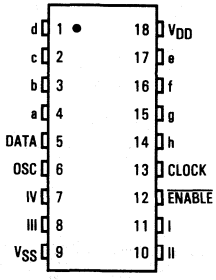
MC14499P Plastic DIP
MC14499DW SOG Package

BLOCK DIAGRAM

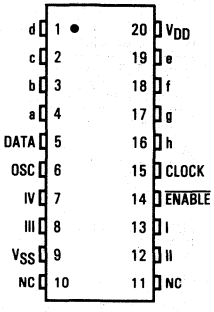


PIN ASSIGNMENTS

PLASTIC DIP



SOG PACKAGE



NC = NO CONNECTION

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +7.0	V
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} +0.5	V
Storage Temperature Range	T_{stg}	−65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics table or Circuit Operation section.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

ELECTRICAL CHARACTERISTICS (V_{DD} = 4.5 to 6.5 V)

Characteristic		Symbol	0°		25°		70°		Unit
			Min	Max	Min	Max	Min	Max	
Serial Port Input Voltage	'0' Level	V_{IL}	–	0.3 × V_{DD}	–	0.3 × V_{DD}	–	0.3 × V_{DD}	V
	'1' Level	V_{IH}	0.7 × V_{DD}	–	0.7 × V_{DD}	–	0.7 × V_{DD}	–	
Serial Port Input Current (V_{in} = 0 to V_{DD})		I_{in}	–	±0.1	–	±0.1	–	±1.0	μA
Oscillator Input Voltage	'0' Level	V_{IL}	–	0.25 × V_{DD}	–	0.25 × V_{DD}	–	0.2 × V_{DD}	V
	'1' Level	V_{IH}	0.75 × V_{DD}	–	0.75 × V_{DD}	–	0.8 × V_{DD}	–	
Oscillator Input Current	V_{OSC} = 0	I_{IL}	–	100	30	80	10	–	μA
	V_{OSC} = V_{DD}	I_{IH}	–	−100	−30	−80	−10	–	
Segment Driver Voltage Below V_{DD}									V
	I_{out} = 50 mA	ΔV_{OH}	–	1.1	–	1.0	–	1.1	
	I_{out} = 10 mA		–	0.8	–	0.75	–	0.8	
Segment Driver Off Leakage	V_{out} = 0	I_{OZ}	–	100	–	50	–	100	μA
Digit Drivers									mA
Source (On)	V_{out} = 0.8 V	I_{OH}	6	–	5.5	–	4	–	
Sink (Off)	V_{out} = 0.5 V	I_{OL}	−0.2	–	−0.2	–	−0.1	–	
Supply Current V_{in} = 0, I_{out} = 0, C_{OSC} = 0.015 μF		I_{DD}	–	1	–	1	–	1	mA
Maximum Power Dissipation		P_D	–	500	–	500	–	500	mW

SWITCHING CHARACTERISTICS (V_{DD} = 5 V ±10%, T_A = 0 to 70°C)

Characteristic	Fig	Symbol	Min	Max	Unit
Clock High Time	2	t_{CH}	2		μs
Clock Low Time	2	t_{CL}	2		μs
Clock Rise Time	2	t_{CR}		2	μs
Clock Fall Time	2	t_{CF}		2	μs
Enable Lead Time	2	$t_{E\ LEAD}$	200		ns
Enable Lag Time	2	$t_{E\ LAG}$	200		ns
Data Set-Up Time	2	$t_{D\ SUP}$	200		ns
Data Hold Time	2	$t_{D\ HOLD}$	1		μs
Scanner Frequency*	4	$1/t_{SCAN}$	50	300	Hz
OSC/Digit Lead Time	4	t_{OD}		10	μs
OSC/Segment Lead Time	4	t_{OS}		10	μs
Digit Overlap	4	t_{OV}		5	μs

*Scanner Capacitance = 0.022 μF.

CIRCUIT OPERATION

The circuit accepts a 20-bit input, 16 bits for the four digit display plus 4 bits for the decimal point—these latter four bits are optional.

The input sequence is the decimal point code followed by the four digits, as shown in Figure 1.

In order to enter data the enable input, $\overline{\text{ENABLE}}$, must be active low. The sample and shift are accomplished on the falling clock edge, see Figure 2. Data are loaded from the shift register to the latches when $\overline{\text{ENABLE}}$ goes high. While the shift register is being loaded the previous data are stored in the latches.

If the decimal point is used, the system requires 20 clock pulses to load data; otherwise only 16 are required.

CASCADING

The circuit may be cascaded in the following manner.

If a 1111 word is loaded into the decimal point latch, the output of the shift register is switched to the decimal point driver, see Figure 3. Therefore, to cascade n four digit display drivers a set-up is used which loads the 1111 cascading word:

1. $\overline{\text{ENABLE}}$ = active low.
2. Load 20-bits, the first four bits being 1, with 20 clock pulses.
3. $\overline{\text{ENABLE}}$ = high, to load the latch.
4. Repeat steps 1 to 3 (n-1) times.
5. (n × 20)-bits can be loaded into n circuits, with 1111 as decimal point word to continue the cascading.

SCANNER

The scanner frequency is determined by an on-chip oscillator, which requires an external frequency-determining capacitor. The capacitor voltage varies between two trigger levels at the oscillator frequency.

An external oscillator signal can be used, within the recommended operating range of 200 to 800 Hz. For test purposes this frequency may be increased up to 10 kHz.

A divide by four counter provides four non-overlapping scanner waveforms corresponding to the four digits—see Figure 4.

SEGMENT DECODER

The code used in this matrix decoders is shown in Figure 5.

OUTPUT DRIVERS

There are two different drivers:

- The segment and decimal point drivers; these are NPN emitter followers with no current limiting devices.
- The digit output buffers; these are short-circuit protected CMOS devices.

A typical application circuit is shown in Figure 6.

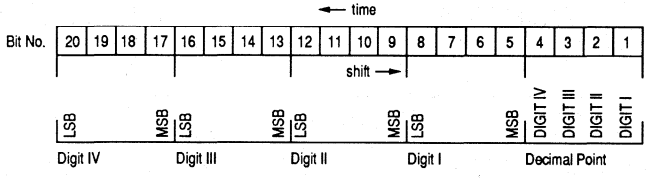


Figure 1. Input Sequence

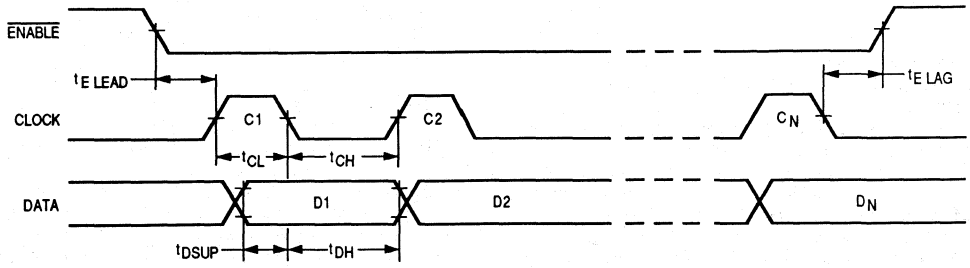


Figure 2a. Serial Input, Positive Clock

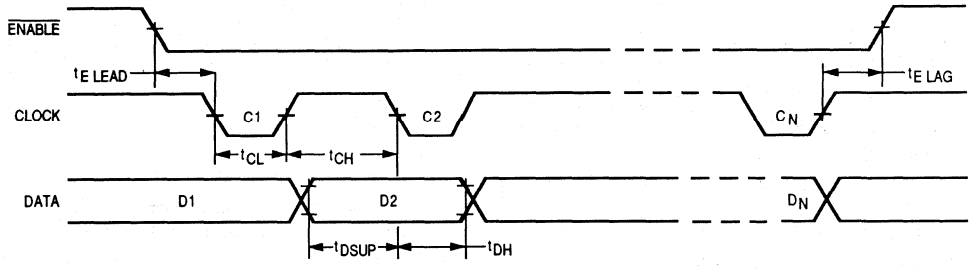


Figure 2b. Serial Input, Negative Clock

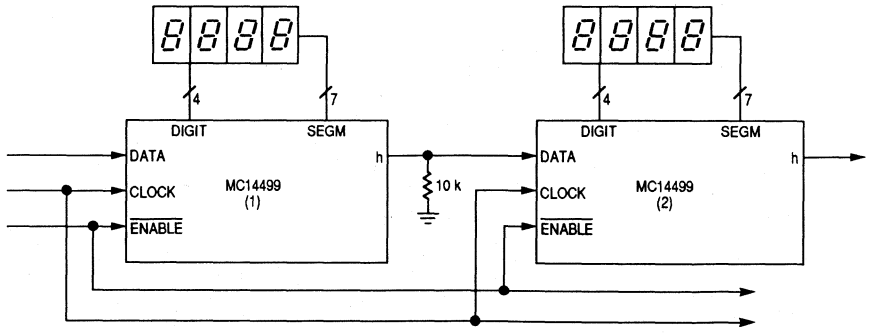


Figure 3. Cascading MC14499s

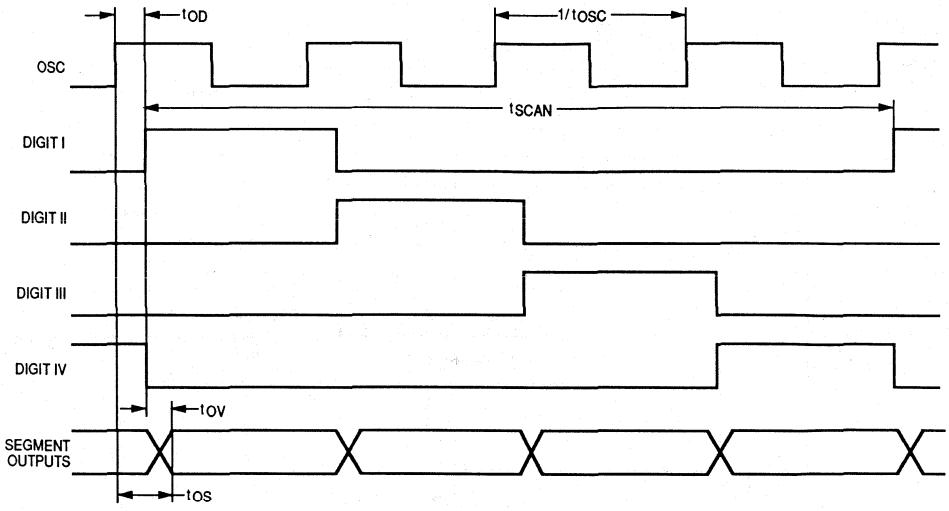


Figure 4. Scanner Waveforms

0000	0		1000	8
0001	1		1001	9
0010	2		1010	A
0011	3		1011	I
0100	4		1100	H
0101	5		1101	U
0110	6		1110	dash -
0111	7		1111	blank

Figure 5. Segment Code

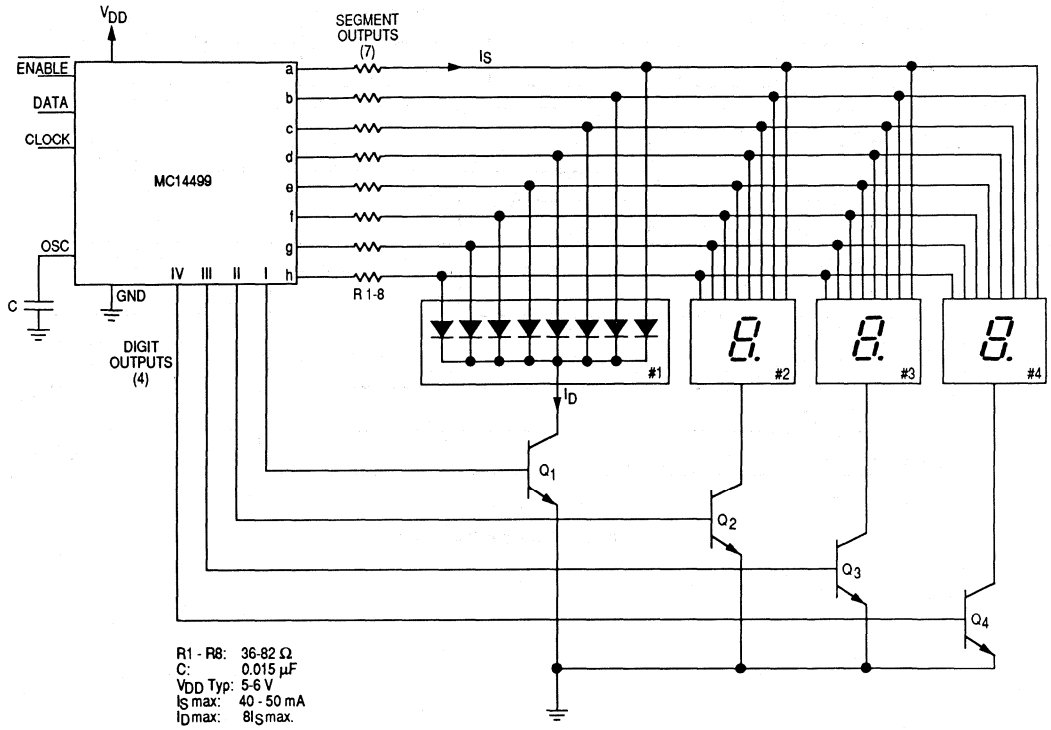


Figure 6. Application Example

MC145000
MC145001

SERIAL INPUT MULTIPLEXED LCD DRIVERS (MASTER AND SLAVE)

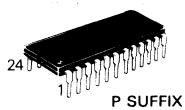
The MC145000 (Master) LCD Driver and the MC145001 (Slave) LCD Driver are CMOS devices designed to drive liquid crystal displays in a multiplexed-by-four configuration. The Master unit generates both frontplane and backplane waveforms, and is capable of independent operation. The Slave unit generates only frontplane waveforms, and is synchronized with the backplanes from the Master unit. Several Slave units may be cascaded from the Master unit to increase the number of LCD segments driven in the system. The maximum number of frontplanes is dependent upon the capacitive loading on the backplane drivers and the drive frequency. The devices use data from a microprocessor or other serial data and clock source to drive one LCD segment per bit.

- Direct Interface to CMOS Microprocessors
- Serial Data Port, Externally Clocked
- Multiplexing-By-Four
- Net dc Drive Component Less Than 50 mV
- Master Drives 48 LCD Segments
- Slave Provides Frontplane Drive for 44 LCD Segments
- Drives Large Segments—Up to one Square Centimeter
- Supply Voltage Range = 3 V to 6 V
- Latch Storage of Input Data
- Low Power Dissipation
- Logic Input Voltage Can Exceed V_{DD}
- Accomodates External Temperature Compensation
- Chip Complexities: MC145000—1723 FETs or 431 Equivalent Gates
  MC145001—1495 FETs or 374 Equivalent Gates

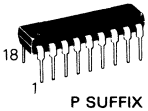
CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

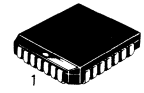
SERIAL INPUT MULTIPLEXED LCD DRIVERS (MASTER AND SLAVE)



P SUFFIX
PLASTIC DIP
CASE 709



P SUFFIX
PLASTIC DIP
CASE 707



FN SUFFIX
PLCC
CASE 776

ORDERING INFORMATION

MC14500xP	Plastic DIP
MC14500xFN	PLCC

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the ranges $V_{SS} \leq V_{out} \leq V_{DD}$ and $V_{SS} \leq V_{in} \leq 15$ V

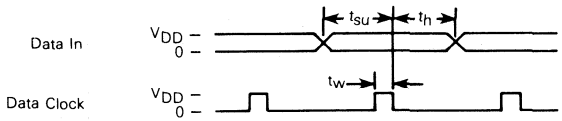
Unused inputs must always be tied to an appropriate logic voltage level.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ#	Max	Unit
Data Clock Frequency	f_{cl}	3.0 6.0	– –	12.5 24	7.5 12.5	MHz
Rise and Fall Times — Data clock	t_r, t_f	3.0 6.0	– –	– –	125 10	μs
Setup Time Data In to Data Clock	t_{su}	3.0 6.0	48 16	– –	– –	ns
Hold Time Data In to Data Clock	t_h	3.0 6.0	−5 0	– –	– –	ns
Pulse Width Data Clock	t_w	3.0 6.0	65 40	– –	– –	ns

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

SWITCHING WAVEFORMS



DEVICE OPERATION

Figure 1 shows a block diagram of the Master unit. The unit is composed of two independent circuits: the data input circuit with its associated data clock, and the LCD drive circuit with its associated system clock.

Forty-eight bits of data are serially clocked into the shift register on the falling edges of the external data clock. Data in the shift register is latched into the 48-bit latch at the beginning of each frame period. (As shown in Figure 3, the frame period, t_{frame}, is the time during which all the LCD segments are set to the desired "ON" or "OFF" states.)

The binary data present in the latch determines the appropriate waveform signal to be generated by the frontplane drive circuits, whereas the backplane waveforms are invariant. The frontplane and backplane waveforms, FPn and BPn, are generated using the system clock (which is the oscillator divided by 256) and voltages from the V/3 generator circuit (which divides V_{DD} into one-third increments). As shown in Figure 3, the frontplane and backplane waveforms and the "ON" and "OFF" segment waveforms have periods equal to t_{frame} and frequencies equal to the system clock divided by four.

Twelve frontplane and four backplane drivers are available from the Master unit. The latching of the data at the beginning of each frame period and the carefully balanced voltage-generation circuitry minimize the generation of a net dc component across any LCD segment.

The Slave unit (Figure 2) consists of the same circuitry as the Master unit, with two exceptions: it has no backplane drive circuitry, and its shift register and latch hold 44 bits. Eleven frontplane and no backplane drivers are available from the Slave unit.

LCD DRIVER SYSTEM CONFIGURATIONS

Figure 4 shows a basic LCD Driver system configuration, with one Master and several Slave units. The maximum number of slave units in a system is dictated by the maximum backplane drive capability of the device and by the system data update rate. Data is serially shifted first into the Master unit and then into the following Slave units on the falling edge of the common data clock. The oscillator is common to the Master unit and each of the Slave units. At the beginning of each frame period, t_{frame}, the Master unit generates a frame-sync pulse (Figure 3) which is received by the Slave units. The pulse is to ensure that all Slave unit frontplane drive circuits are synchronized to the Master unit's backplane drive circuits.

A single multiplexed-by-four, 7-segment (plus decimal point) LCD and possible frontplane and backplane connections are shown in Figure 5. When several such displays are used in a system, the four backplanes generated by the Master unit are common to all the LCD digits in the system. The twelve frontplanes of the Master unit are capable of controlling forty-eight LCD segments (6 LCD digits), and the eleven frontplanes of each Slave unit are capable of controlling forty-four LCD segments (5½ LCD digits).

FIGURE 1 — BLOCK DIAGRAM OF THE MC145000 (MASTER) LCD DRIVER

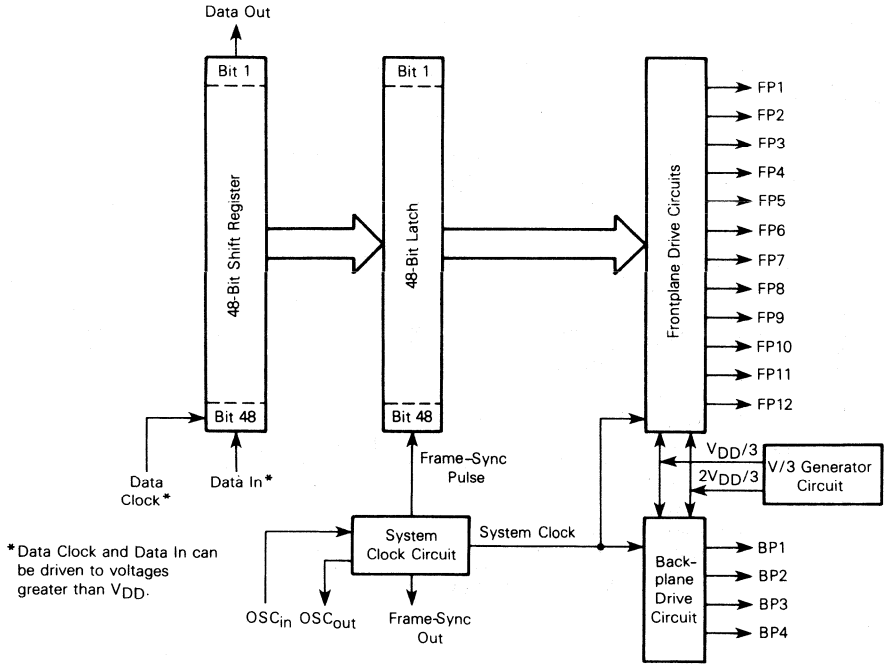
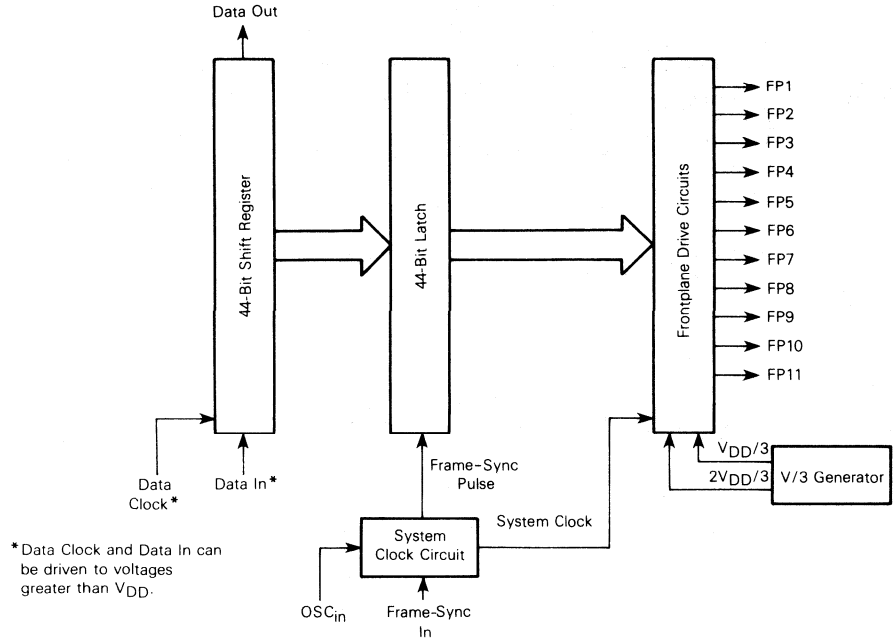


FIGURE 2 — BLOCK DIAGRAM OF THE MC145001 (SLAVE) LCD DRIVER



OSC_{in} (Master and Slave)

The input pin to the system clock circuit. The oscillator frequency is either obtained from an external oscillator or generated in the Master unit by connecting an external resistor between the OSC_{in} pin and the OSC_{out} pin. Figure 6 shows the relationship between resistor value and frequency.

OSC_{out} (Master)

The output pin of the system clock circuit. This pin is connected to the OSC_{in} input of each Slave unit.

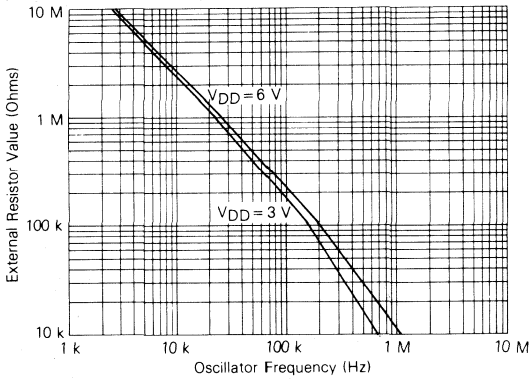
V_{DD} (Master and Slave)

The positive supply voltage.

V_{SS} (Master and Slave)

The negative supply (or ground) voltage.

FIGURE 6 — TYPICAL OSCILLATOR FREQUENCY vs EXTERNAL RESISTOR VALUE



APPLICATIONS

The following examples are presented to give the user further insight into the operation and organization of the Master and Slave LCD Drivers.

An LCD segment is turned either on or off depending upon the RMS value of the voltage across it. This voltage is equal to the backplane voltage waveform minus the frontplane voltage waveform. As previously stated, the backplane waveforms are invariant (see Figure 3). Figure 10 shows one period of every possible frontplane waveform.

For a detailed explanation of the operation of liquid crystal materials and multiplexed displays, refer to a brochure entitled "Multiplexed Liquid Crystal Displays," by Gregory A. Zaker, General Electric Company, Liquid XTAL Displays Operation, 24500 Highpoint Road, Cleveland, Ohio 44122.

Example 1: Many applications (e.g., meters, gasoline pumps, pinball machines, and automobile dashboard displays) require that, for each display update, an entirely new set of data must be shifted into the Master and cascaded Slave units. The correspondence between the frontplane-backplane intersections at the LCD segments and the data bit locations in the 48-bit latch of the Master (or 44-bit latch of the Slave) is necessary information to the system designer. In Figure 1, it is shown that data is serially shifted first into the 48th-bit location of the shift register of the Master. Thus, after 48 data bits have been shifted in, the first bit to be entered has been shifted into bit-location one, the second bit into bit-location two, and so on. Table 1 shows the bit location in the latch that controls the corresponding frontplane-backplane intersection. For example, the information stored in the 26th-bit location of the latch controls the LCD segment at the intersection of FP7 and BP3. The voltage waveform across that segment is equal to (BP3 minus FP7). The same table, but with the column for FP12 deleted, describes the operation of the Slave unit.

In applications of this type, all the necessary data to completely update the display are serially shifted into the Master and succeeding Slave units within a frame period. Typically, a microprocessor is used to accomplish this.

Example 2: Many keyboard-entry applications, such as calculators, require that the most significant digit be entered and displayed first. Then as each succeeding digit is entered, the previously entered digits must shift to the left. It is, therefore, neither necessary nor desirable to enter a completely new set of data for each display change. Figure 7 shows a representation of a system consisting of one Master and three Slave units and displaying 20 LCD digits. If each digit has the frontplane-backplane configuration shown in Figure 5, the relationship between frontplanes, backplanes, and LCD segments in the display is shown in Table 2.

Digits (or alphanumeric characters) are entered, most-significant digit first, by using a keyboard and a decoder external to the MC145000. Data is entered into the Master and cascaded Slave units according to the following format:

1) Initially, all registers and latches must be cleared by entering 160 zero data bits. This turns off all 160 segments of the display.

2) Entering the most-significant digit from the keyboard causes the appropriate eight bits to be serially shifted into the Master unit. These eight bits control LCD segments a through h of digit 1, and cause the desired digit to be displayed in the least-significant digit location.

3) Entering the second-most-significant digit from the keyboard causes eight more bits to be serially shifted into the Master unit. These eight bits now control LCD segments a through h of digit 1, and the previously entered eight bits now control segments a through h of digit 2. Thus the two digits are displayed in the proper locations.

4) Entering the remaining 18 digits from the keyboard fills the 20-digit display. Entering an extra digit will cause the first digit entered to be shifted off the display.

Example 3: In addition to controlling 7-segment (plus decimal point) digital displays, the MC145000 and MC145001 may be used to control displays using 5×7 dot matrices. A Master and three Slave units can drive 180 LCD segments, and therefore are capable of controlling five 5×7 dot matrices (175 segments). Two control schemes are presented in Figures 8 and 9; one using a single Master unit, and one using two Master units.

TABLE 1 — THE BIT LOCATIONS, IN THE LATCH, THAT CONTROL THE LCD SEGMENTS LOCATED AT EACH FRONTPLANE-BACKPLANE INTERSECTION

		FRONTPLANES											
BACKPLANES		FP1	FP2	FP3	FP4	FP5	FP6	FP7	FP8	FP9	FP10	FP11	FP12
	BP1	4	8	12	16	20	24	28	32	36	40	44	48
	BP2	3	7	11	15	19	23	27	31	35	39	43	47
	BP3	2	6	10	14	18	22	26	30	34	38	42	46
	BP4	1	5	9	13	17	21	25	29	33	37	41	45

FIGURE 7 — A 20-DIGIT DISPLAY (EQUIVALENT TO A 4×40 ARRAY)

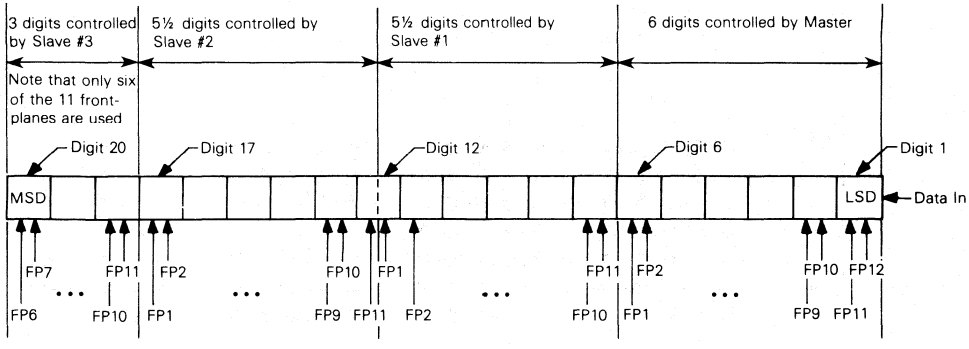


TABLE 2 — THE RELATIONSHIP BETWEEN FRONTPLANE-BACKPLANE INTERSECTIONS AND LCD SEGMENTS FOR THE SYSTEM CONFIGURATION OF FIGURE 7

	Master							Slave #1				Slave #2						Slave #3				
	FP12	FP11	FP10	FP9	• • •	FP2	FP1	FP11	FP10	• • •	FP1	FP11	FP10	FP9	• • •	FP2	FP1	FP11	FP10	• • •	FP7	FP6
BP1	a1	f1	a2	f2		a6	f6	a7	f7		a12	f12	a13	f13		a17	f17	a18	f18		a20	f20
BP2	b1	g1	b2	g2		b6	g6	b7	g7		b12	g12	b13	g13		b17	g17	b18	g18		b20	g20
BP3	c1	e1	c2	e2		c6	e6	c7	e7		c12	e12	c13	e13		c17	e17	c18	e18		c20	e20
BP4	h1	d1	h2	d2		h6	d6	h7	d7		h12	d12	h13	d13		h17	d17	h18	d18		h20	d20
	digit 1		digit 2		• • •	digit 6		digit 7		• • •	digit 12	digit 13			• • •	digit 17		digit 18		• • •	digit 20	

FIGURE 8 — EXAMPLE OF A 5×7 DOT MATRIX DISPLAY SYSTEM CONTROLLED BY ONE MASTER AND THREE SLAVE UNITS

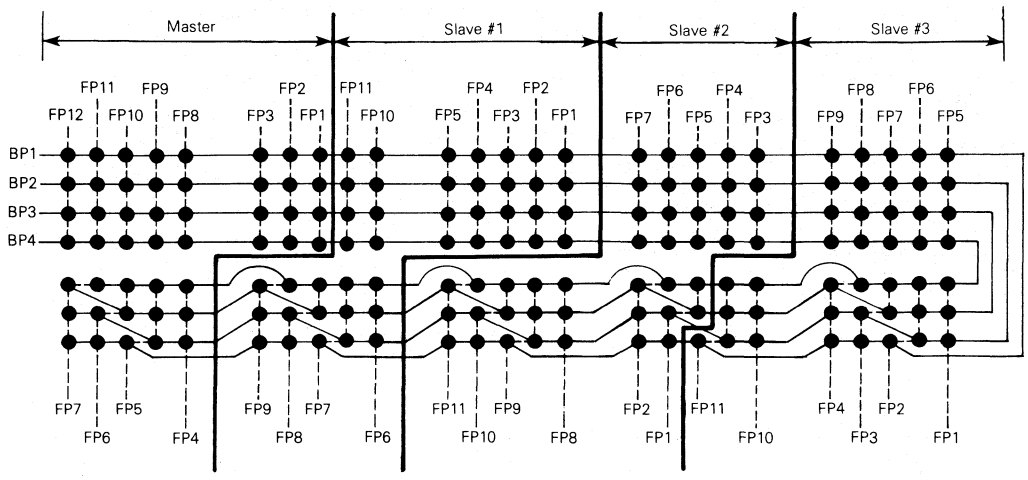


FIGURE 9 — EXAMPLE OF A 5×7 DOT MATRIX DISPLAY SYSTEM CONTROLLED BY TWO MASTER AND TWO SLAVE UNITS

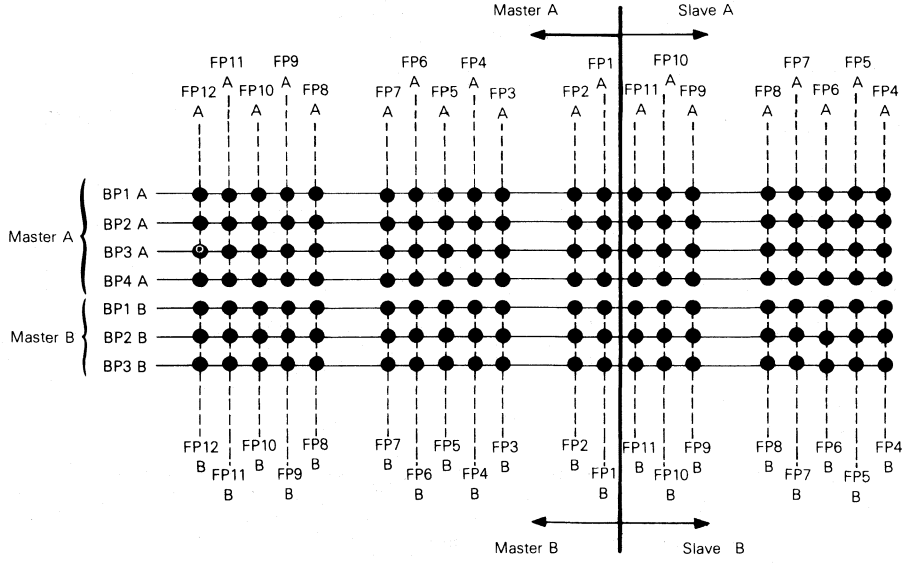
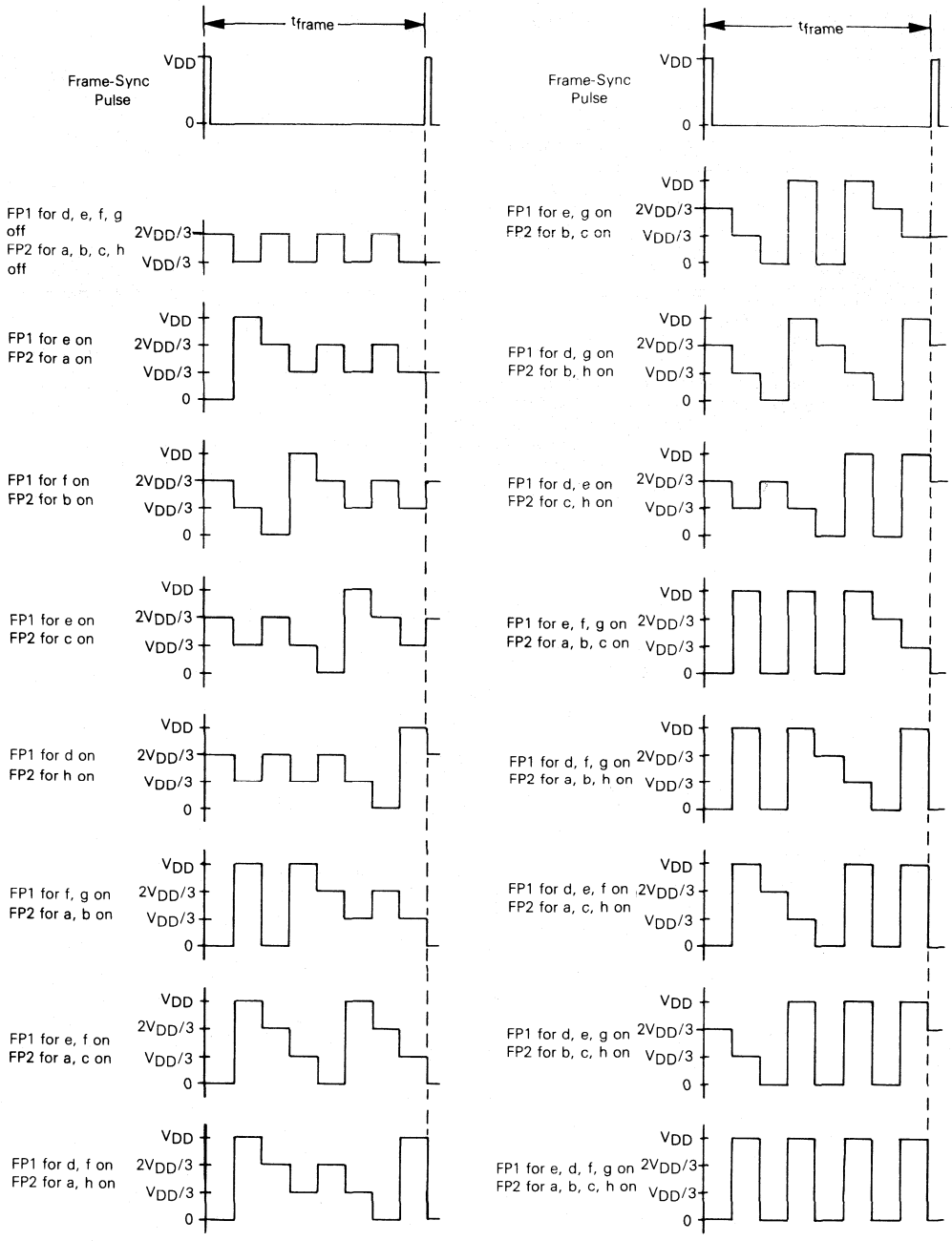


FIGURE 10 — POSSIBLE FRONTPLANE WAVEFORMS



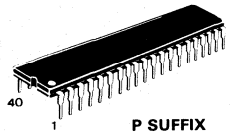
MC145453

LCD Driver with Serial Interface
LSI CMOS

The MC145453 Liquid-Crystal Display Driver consists of a 36-stage serial-in/parallel-out shift register with 33 latches and drivers. Each package drives up to 33 non-multiplexed LCD segments; e.g., a 4½-digit, 7-segment-plus-decimal display. This device may be paralleled to increase the number of segments driven.

The input format is a Start Bit (high), followed by 33 Display Bits, plus 2 Trailing Bits (don't cares). A high Start Bit, after propagating to the last shift register stage, triggers generation of an internal load signal which transfers the 33 Display Bits into latches. An internal reset clears only the shift register which readies the device for the next bit stream.

- On-Chip Oscillator Provides 50 Percent Duty Cycle Backplane Drive
- No External Load Signal Required
- Operating Voltage Range: 3 to 10 V
- Operating Temperature Range: −40° to 85°C
- TTL-Compatible Inputs May Be Driven With CMOS
- May Be Used With Segmented-Alphanumeric, Bar-Graph, or Dot-Matrix LCDs
- Advantages Over Multiplexed LCD Systems: Wider Viewing Angle
  Optimum Contrast at Low Voltage
  Better Legibility at Extreme Temperature
- *For Additional Applications Information, see AR266*

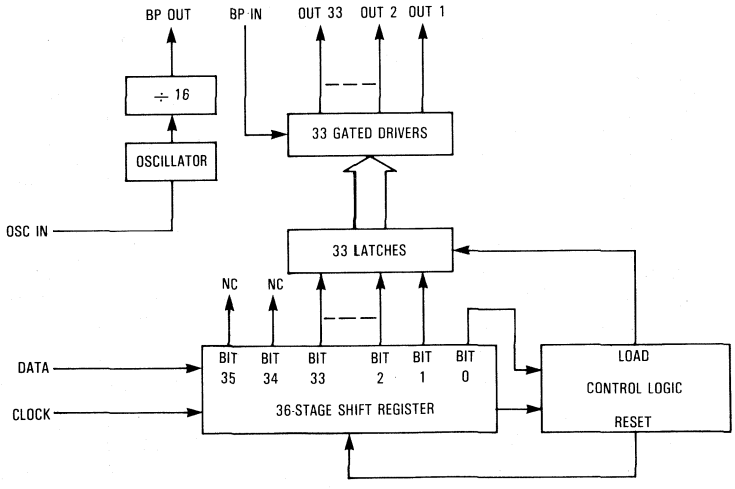


P SUFFIX
PLASTIC DIP
CASE 711

FN SUFFIX
PLCC
CASE 777

ORDERING INFORMATION
MC145453P Plastic DIP
MC145453FN PLCC

BLOCK DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

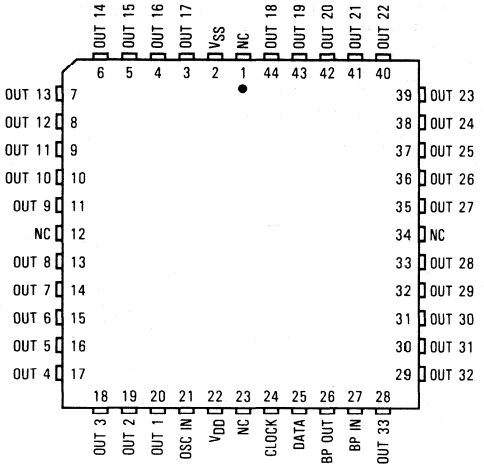
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +11.0	V
V_{in}	DC Input Voltage	−0.5 to V_{DD} +0.5	V
V_{out}	DC Output Voltage	−0.5 to V_{DD} +0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{DD} and V_{SS} Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating: −12 mW/°C from 65°C to 85°C.

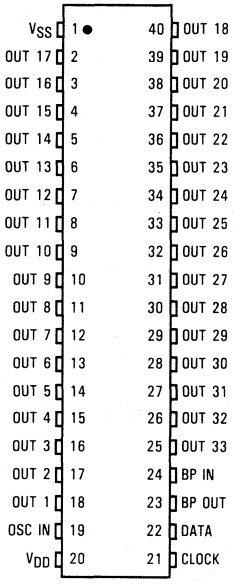
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD} except Osc In which must be tied to V_{SS}). Unused outputs must be left open.

PIN ASSIGNMENTS



NC = NO CONNECTION



APPLICATIONS INFORMATION

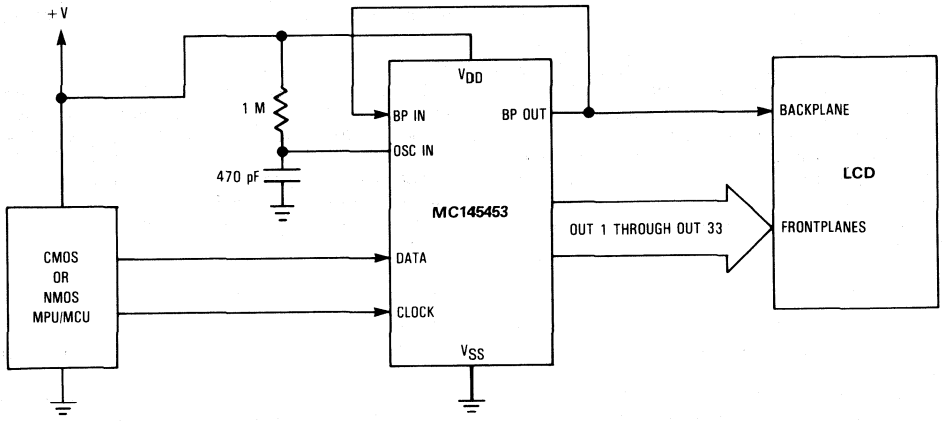


Figure 3. Using On-Chip Oscillator

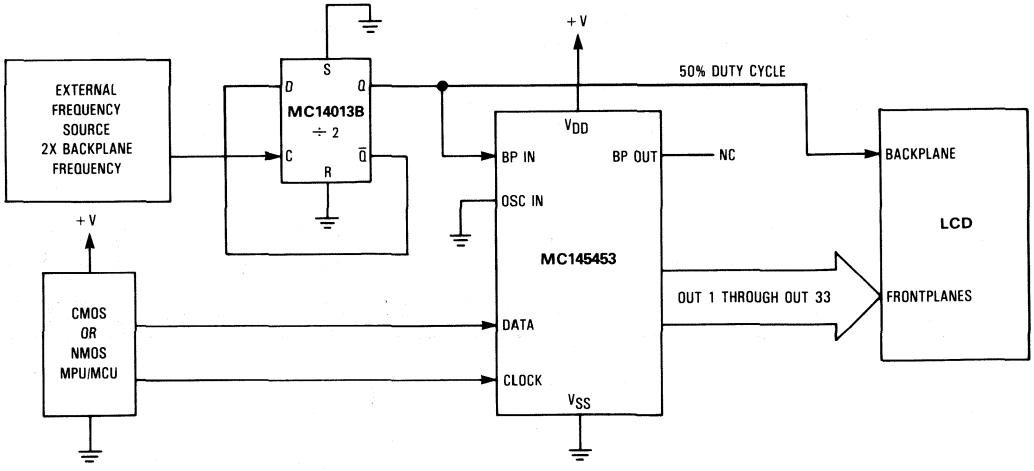


Figure 4. Converting External Backplane Frequency Source to 50% Duty Cycle

APPLICATIONS INFORMATION (CONT'D)

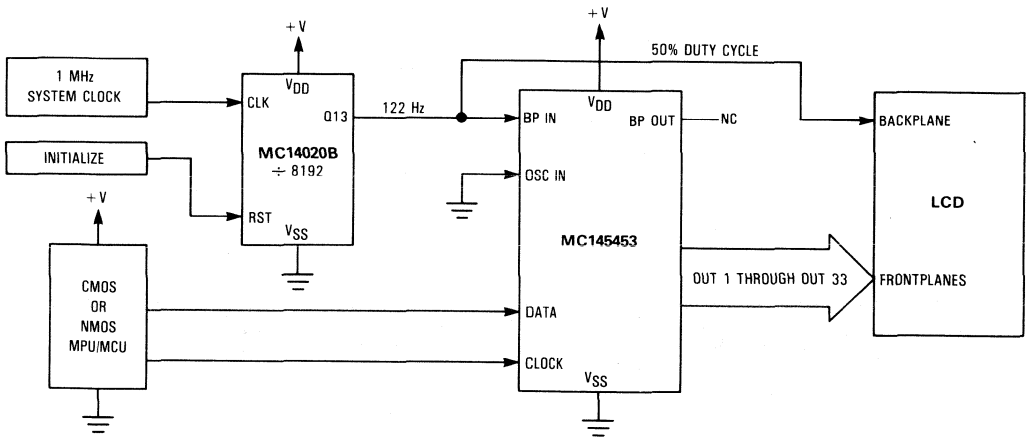


Figure 5. Using Low-Cost Divider to Sync Backplane Frequency

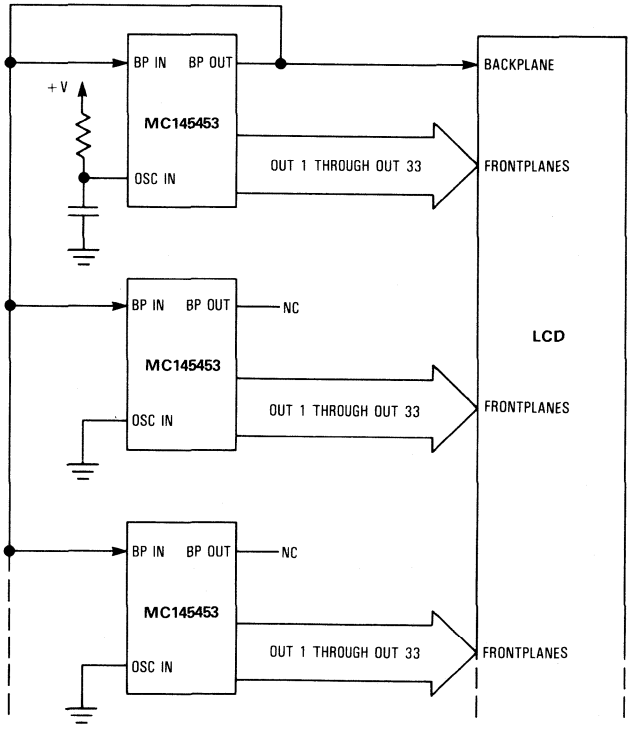


Figure 6. Paralleling Devices to Increase Number of Driven Segments

Operational Amplifiers/Comparators

		Page No.
MC14471	Low-Power Comparators plus Alarm Driver Circuitry	4-3
MC14573	Quad Programmable Op Amp	4-8
MC14574	Quad Programmable Comparator	4-8
MC14575	Programmable Dual Op Amp/Dual Comparator	4-8
MC14576A	Dual Video Amplifier	4-17
MC14577A	Dual Video Amplifier	4-17
MC14578	Micro-Power Comparator plus Voltage Follower	4-23

SELECTOR GUIDE

Function	Quantity Per Package	Single Supply Voltage Range	Dual Supply Voltage Range	Frequency Range	Device Number
Operational Amplifiers	4	3 to 15 V	±1.5 to ±7.5 V	DC to ~1 MHz	**MC14573**
Video Amplifiers	2	5 to 12 V*	±2.5 to ±6 V♦	up to 10 MHz	**MC14576A MC14577A**
Comparators	4	3 to 15 V	±1.5 to ±7.5 V	DC to ~1 MHz	**MC14574**
Micro-Power Comparator	1	3.5 to 14 V	±1.75 to ±7 V	—	**MC14578**
Low-Power Comparators	2	6 to 12 V	—	—	**MC14471**
Operational Amplifiers and Comparators	2 and 2	3 to 15 V	±1.5 to ±7.5 V	DC to ~1 MHz	**MC14575**

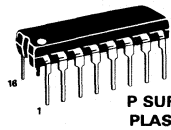
*5 to 10 V for surface-mount package.

♦±2.5 to ±5 V for surface-mount package.

MC14471

Advance Information

Low-Power Comparators plus Alarm-Driver Circuitry
CMOS

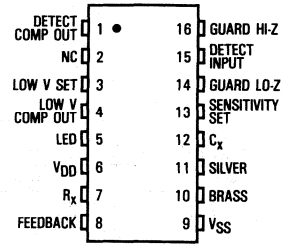


P SUFFIX
PLASTIC
CASE 648

ORDERING INFORMATION

MC14471P	PDIP

PIN ASSIGNMENT



The MC14471 contains both digital and analog components for use as an alarm driver. The device consists of three comparators: one for the detection of an alarm condition, one to detect a low battery, and one to track the voltage of the alarm-detect input, without loading that input down. An on-chip oscillator is provided, which requires two external passive components. The part also contains circuitry to drive an external piezoelectric horn and a visible LED.

This device is used in any equipment that requires a battery-operated audible and/or visual alarm. The MC14471 operates in one of four possible environmental conditions: (1) no alarm condition/no low battery, (2) alarm condition/no low battery, (3) no alarm condition/low battery, and (4) alarm condition/low battery. While in the no alarm/no low battery condition, the status of the detect inputs are checked every 1.67 seconds. If an alarm/good battery condition exists, the detect inputs are sampled every 40 ms and the alarm is sounded. In this mode, the horn is repeatedly on for 160 ms and off for 80 ms and the LED flashes every 0.96 second until the alarm status goes away. If a no alarm/low battery condition is present, the detect inputs again are checked every 1.67 seconds and the horn and LED outputs are activated every 40 seconds with an on time of 10 ms. Lastly, during the alarm/low battery condition, the detect inputs are sampled every 40 ms, the horn sounds, and the LED flashes once per 0.96 second.

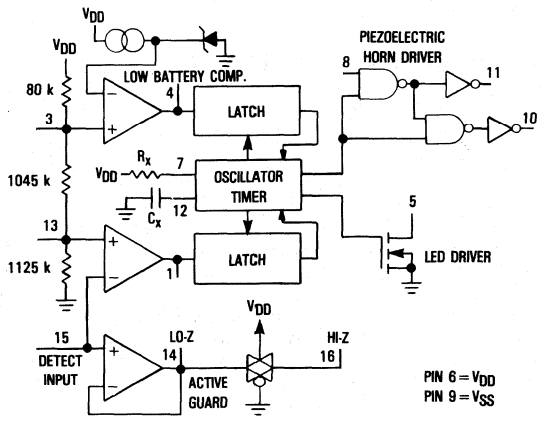
The trip point for the alarm input is typically 50% of V_{DD}, while the trip point of the low-battery input is established by an on-chip zener diode. These thresholds can be altered over a limited range with the use of external resistors connected to either V_{SS} or V_{DD}.

Applications for the MC14471 include liquid level detectors, soil moisture-content detectors, and virtually any situation in which an alarm is needed.

- Piezoelectric Horn Driver
- Guard Outputs on Both Sides of Alarm Detect Input
- Comparator Outputs for Alarm Detect and Low Battery
- Internal Reverse Battery Protection
- Electrostatic Discharge (ESD) and Latch-Up Protection Circuitry on All Pins
- Pin-for-Pin Compatible with the MC14467P1, without ±1.0 pA Leakage Testing or UL217 Compatibility
- Operating Voltage Range: 6 to 12 V
- Average Supply Current: 12 μA
- Operating Temperature Range: −10 to 60°C
- Chip Complexity: 239 FETs

This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +15	V
V_{in}	DC Input Voltage, All Inputs Except Pin 8	−0.25 to V_{DD} + 0.25	V
I_{in}	DC Input Current, per Pin, Except Pin 15 = 1 mA	±10	mA
I_{out}	DC Output Current, per Pin	±30	mA
T_{stg}	Storage Temperature	−55 to +125	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
t_{RB}	Reverse Battery Time	5.0	s

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$ except for pin 8, which can exceed V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	9.0	V
C_x	Timing Capacitor (Can Use Up to ±20% Tolerance)	0.1	μF
R_x	Timing Resistor (Can Use Up to ±20% Tolerance)	8.2	MΩ
I_{ld}	Battery Load (Resistor or LED)	10	mA
T_A	Operating Temperature	−10 to +60	°C

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, Voltages Referenced to V_{SS})

Symbol	Parameter	Test Condition	V_{DD} V	Min	Max	Unit
V_{DD}	Power Supply Voltage Range		–	6.0	12	V
I_{DD}	Average Operating Supply Current	$R_X = 8.20$ MΩ	9.0 12.0	– –	9.0 12.0	μA
V_{in}	Input Voltage Range, Pin 8		–	−10	$V_{DD}+10$	V
V_{th}	Supply Threshold Voltage, Low-Supply Alarm		–	7.2	7.8	V
V_{ref}	Smoke Comparator Reference Voltage		–	47	53	$\%V_{DD}$
V_{hys}	Hysteresis Voltage	Alarm Condition, Pin 13	9.0	75	150	mV
V_{CM}	Common Mode Voltage Range, Pin 15		–	0.6	$V_{DD}-2$	V
V_{OS}	Offset Voltage — Active Guard Detect Comparator	$V_{in} = V_{DD}/2$	9.0 9.0	– –	±100 ±50	mV
I_{in}	Input Current, Detect Input	$V_{in} = V_{SS}$ or V_{DD}	9.0	–	±40	nA
C_{in}	Input Capacitance		–	–	TBD	pF
V_{OH}	High-Level Output Voltage — Piezoelectric Horn Drivers Comparators	$I_{out} = -16$ mA $I_{out} = -30$ μA	7.2 9.0	6.3 8.5	– –	V
V_{OL}	Low-Level Output Voltage — Piezoelectric Horn Drivers Comparators	$I_{out} = 16$ mA $I_{out} = 30$ μA	7.2 9.0	– –	0.9 0.5	V
V_{OL}	Low-Level Output Voltage — LED Driver	$I_{out} = 10$ mA	7.2	–	3.0	V
Z_{out}	Output Impedance, Active Guard — Lo-Z, Pin 14 Hi-Z, Pin 16		9.0 9.0	– –	10 1000	kΩ

AC ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V_{DD} = 9.0$ V, $C_X = 0.10$ μF, $R_X = 8.20$ MΩ, See Figure 4)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
$1/f_{osc}$	Oscillator Period	Free-Running Sawtooth Measured at Pin 12	No Alarm Alarm	1.34 32	1.67 40	2.0 48	s ms
t_r	Oscillator Rise Time			8	10	12	ms
$t_{w(Horn)}$	Horn Pulse Width	During Alarm Condition	On Off	120 60	160 80	208 104	ms
$t_{w(LED)}$	LED Pulse Width		Between Pulses On	32 8	40 10	48 12	s ms
$t_{w(Horn)}$	Horn Pulse Width	During Low Battery	On Between Pulses	8 32	10 40	12 48	ms s

DEVICE OPERATION

TIMING

The internal oscillator of the MC14471 operates with a period of 1.67 seconds during no-alarm conditions. Each 1.67 seconds, internal power is applied to the entire IC and a check is made for an alarm state, except during LED pulse, Low Battery Alarm Chirp, or Horn Modulation (in alarm condition). Every 24 clock cycles a check is made for low battery by comparing V_{DD} to an internal zener voltage.

The oscillator capacitor should be of a low-leakage type because of the low-current oscillator employed. Lastly, the tolerance of the external timing components must be no greater than ±20%.

DETECT CIRCUITRY

If an alarm is detected, the oscillator period becomes 40 ms and the piezoelectric horn oscillator circuit is enabled. The horn output is modulated 160 ms on, 80 ms off. During the off time, the alarm condition is again checked and inhibits further horn output if an alarm condition is not sensed. During the alarm condition the low battery alarm is inhibited, but the LED pulses at a 1.0 Hz rate.

An active guard is provided on both pins adjacent to the detect input. The voltage at these pins is within 100 mV of the input signal. This keeps surface leakage currents to a minimum and provides a method of measuring the input voltage without loading the detect input pin. The active guard op amp is not power strobed and thus gives constant protection from surface leakage currents. The Detect Input has internal diode protection against static damage.

SENSITIVITY/LOW BATTERY THRESHOLDS

Both the sensitivity threshold and the low battery voltage levels are set internally by a common voltage divider connected between V_{DD} and V_{SS}. These voltages can be altered by external resistors connected from pins 3 or 13 to either V_{DD} or V_{SS}. Due to the common voltage divider network, there is a slight interaction between the thresholds.

TEST MODE

Because the internal op amps and comparators are power strobed, adjustments for sensitivity or low battery level may be difficult and time consuming. By forcing pin 12 to V_{SS},

the power strobing is bypassed and the outputs, Pins 1 and 4, constantly show alarm/no alarm and good battery/low battery, respectively. Pin 1 = V_{DD} for smoke and Pin 4 = V_{DD} for low battery. In this mode and during the 10 ms power strobe, chip current rises to approximately 50 μA.

LED PULSE

The 9-volt battery level is checked every 40 seconds during the LED pulse. The battery is loaded via a 10 mA pulse for 10 ms. If the LED is not used, it should be replaced with an equivalent resistor such that the battery loading remains at 10 mA.

HYSTERESIS

When an alarm is detected, the resistor/divider network that sets sensitivity is altered to increase sensitivity. This yields approximately 100 mV of hysteresis and reduces intermittent triggering.

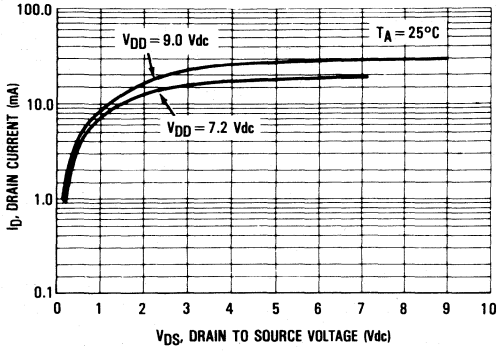


Figure 1. Typical LED Output I-V Characteristic

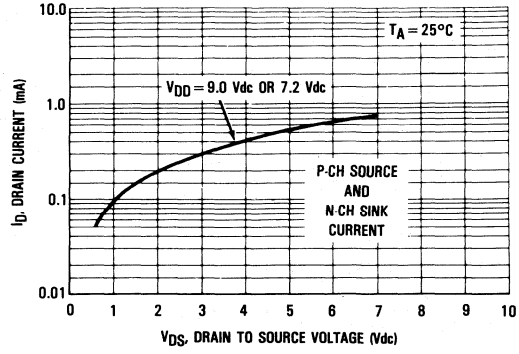
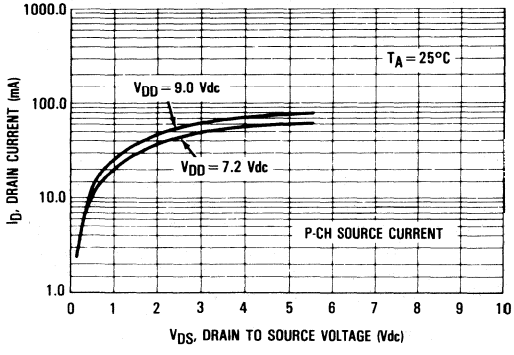


Figure 2. Typical Comparator Output I-V Characteristic



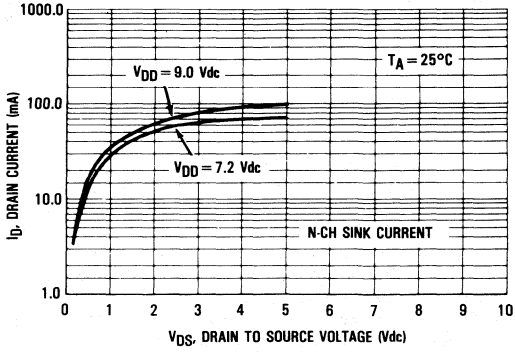
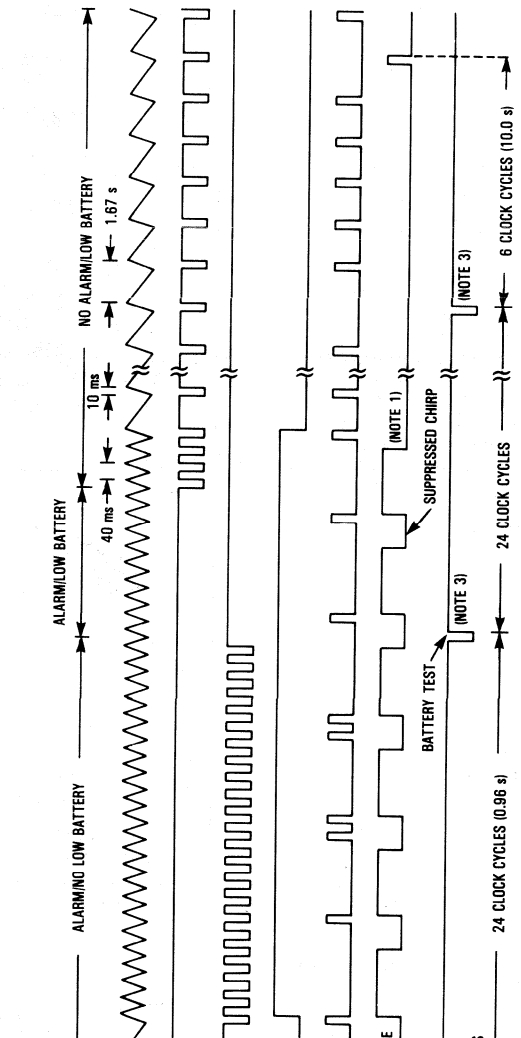


Figure 3. Typical P Horn Driver Output I-V Characteristic



NOTES:
1. Horn modulation is self-completing. When going from alarm to no alarm, the alarm condition will terminate only when horn is off.
2. Comparators are strobed on once per clock cycle (1.67 s for no alarm, 40 ms for alarm).
3. Low battery comparator information is latched only during LED pulse.
4. ~ 100 mVp-p swing.

Figure 4. Timing Diagram

OPERATIONAL AMPLIFIER ELECTRICAL CHARACTERISTICS

(I_{Set} = 200 μA, R_L = 10 MΩ, C_L = 15 pF, T_A = 25°C, unless otherwise indicated, Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} V	Min	Typ#	Max	Unit
Input Common Mode Voltage Range	V_{ICR}	5	0	–	3	V
		10	0	–	8	
		15	0	–	13	
Output Voltage Range	V_{OR}	5	0.1	–	4.8	V
R_L = 100 k to V_{SS}		10	0.1	–	9.8	
		15	0.1	–	14.8	
Input Offset Voltage	V_{IO}	5	–	±8	±30	mV
MC14573, MC14575		10	–	±10	±30	
		15	–	±12	±30	
Average Temperature Coefficient of V_{IO}	$\Delta V_{IO}/\Delta T$	–	–	20	–	μV/°C
Input Capacitance	C_{in}	–	–	5	10	pF
Input Bias Current	I_{IB}	–	–	1	50	pA
Input Bias Current T_A = −40°C to +85°C	I_{IB}	–	–	–	1	nA
Input Offset Current	I_{IO}	–	–	–	100	pA
Open Loop Voltage Gain V_O = 3 V p-p	A_{VOL}	5	1	2	–	V/mV
V_O = 6 V p-p		10	1	3	–	
V_O = 9 V p-p		15	1	4	–	
Power Supply Rejection Ratio	PSRR	5	45	54	–	dB
MC14573, MC14575		10	54	67	–	
		15	54	67	–	
Common Mode Rejection Ratio	CMRR	5	40	55	–	dB
MC14573, MC14575		10	50	67	–	
		15	50	70	–	
Output Source Current $V_{OH} = V_{DD} - 1.5$ V	I_{OH}	15	550	800	–	μA
Output Sink Current V_{OL} = 0.4 V	I_{OL}	5	2.2	4.2	–	mA
V_{OL} = 0.5 V		10	5.0	10.0	–	
V_{OL} = 1.5 V		15	15	30	–	
Slew Rate	S_R	–	5	7	–	V/μs
Unity Gain Bandwidth	G_{BW}	5	1.5	3	–	MHz
Phase Margin	ϕM	–	–	48	–	Degrees
Channel Separation	–	–	–	80	–	dB
Supply Current, Per Pair ($R_L = \infty$, V_{in+} = 1.0 V, V_{in-} = 0 V)	I_{DD}	15	–	2.6	3.4	mA

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

COMPARATOR ELECTRICAL CHARACTERISTICS

(I_{Set} = 20 μA, R_L = 10 MΩ, C_L = 50 pF, T_A = 25°C, unless otherwise indicated, Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} V	Min	Typ #	Max	Unit
Input Common Mode Voltage Range	V_{ICR}	3	0	–	1.5	V
		5	0	–	3.5	
		10	0	–	8.5	
		15	0	–	13.5	
Output Voltage Range "0" Level	V_{OL}	3	–	0	0.05	V
		5	–	0	0.05	
		10	–	0	0.05	
		15	–	0	0.05	
Output Voltage Range "1" Level	V_{OH}	3	2.95	3	–	V
		5	4.95	5	–	
		10	9.95	10	–	
		15	14.95	15	–	
Input Offset Voltage MC14574, MC14575	V_{IO}	3	–	±8	±30	mV
		5	–	±8	±30	
		10	–	±10	±30	
		15	–	±10	±30	
Average Temperature Coefficient of V_{IO}	$\Delta V_{IO}/\Delta T$	–	–	15	–	μV/°C
Input Capacitance	C_{in}	–	–	5	10	pF
Input Bias Current	I_{IB}	–	–	1	50	pA
Input Bias Current T_A = −40°C to +85°C	I_{IB}	–	–	–	1	nA
Input Offset Current	I_{IO}	–	–	–	100	pA
Open Loop Voltage Gain V_O = 1 Vp-p	A_{VOL}	3	1	20	–	V/mV
V_O = 3 Vp-p		5	1	10	–	
V_O = 6 Vp-p		10	1	6	–	
V_O = 9 Vp-p		15	1	6	–	
Power Supply Rejection Ratio MC14574, MC14575	PSRR	3	45	57	–	dB
		5	54	67	–	
		10	54	67	–	
		15	54	67	–	
Common Mode Rejection Ratio MC14574, MC14575	CMRR	3	45	55	–	dB
		5	50	65	–	
		10	54	67	–	
		15	54	67	–	
Output Source Current V_{OH} = 2.6 V	I_{OH}	3	−0.35	−0.65	–	mA
V_{OH} = 2.5 V		5	−2.5	−5.0	–	
V_{OH} = 4.6 V		5	−0.60	−1.1	–	
V_{OH} = 9.5 V		10	−1.3	−2.5	–	
V_{OH} = 13.5 V		15	−5.0	−9.5	–	
Output Sink Current V_{OL} = 0.4 V	I_{OL}	3	1.3	2.6	–	mA
V_{OL} = 0.4 V		5	1.9	3.8	–	
V_{OL} = 0.5 V		10	3.5	6.5	–	
V_{OL} = 1.5 V		15	14	25	–	
Output Rise and Fall Time, 100 mV Overdrive	t_{TLH}, t_{THL}	3	–	140	250	ns
		5	–	100	180	
		10	–	120	200	
		15	–	140	250	
Propagation Delay Time, 5 mV Overdrive	t_d	3	–	15	30	μs
		5	–	10	20	
		10	–	12	24	
		15	–	15	30	
Propagation Delay Time, 100 mV Overdrive	t_d	3	–	4	8	μs
		5	–	2	4	
		10	–	3	6	
		15	–	4	8	
Channel Separation	–	–	–	80	–	dB
Supply Current, Per Pair (R_L = ∞, I_{Set} = 20 μA, V_{in+} = 1.0 V, V_{in-} = 0 V)	I_{DD}	5	–	180	250	μA

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

COMPARATOR ELECTRICAL CHARACTERISTICS

(I_{Set} = 200 µA, R_L = 10 MΩ, C_L = 50 pF, T_A = 25°C, unless otherwise indicated, Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} V	Min	Typ#	Max	Unit
Input Common Mode Voltage Range		V_{ICR}	5 10 15	0 0 0	– – –	3 8 13	V
Output Voltage Range "0" Level		V_{OL}	5 10 15	– – –	0 0 0	0.05 0.05 0.05	V
Output Voltage Range "1" Level		V_{OH}	5 10 15	4.95 9.95 14.95	5 10 15	– – –	V
Input Offset Voltage MC14574, MC14575		V_{IO}	5 10 15	– – –	±10 ±13 ±15	±30 ±30 ±30	mV
Average Temperature Coefficient of V_{IO}	T_A = −40°C to +85°C	$\Delta V_{IO}/\Delta T$	–	–	20	–	µV/°C
Input Capacitance		C_{in}	–	–	5	10	pF
Input Bias Current		I_{IB}	–	–	1	50	pA
Input Bias Current	T_A = −40°C to +85°C	I_{IB}	–	–	–	1	nA
Input Offset Current		I_{IO}	–	–	–	100	pA
Open Loop Voltage Gain	V_O = 3 Vp-p V_O = 6 Vp-p V_O = 9 Vp-p	A_{VOL}	5 10 15	2 1 1	7 4 4	– – –	V/mV
Power Supply Rejection Ratio MC14574, MC14575		PSRR	5 10 15	45 54 54	67 67 67	– – –	dB
Common Mode Rejection Ratio MC14574, MC14575		CMRR	5 10 15	40 50 50	65 67 67	– – –	dB
Output Source Current	V_{OH} = 2.5 V V_{OH} = 4.6 V V_{OH} = 9.5 V V_{OH} = 13.5 V	I_{OH}	**5** **5** **10** **15**	−2.5 −0.60 −1.3 −5.0	−5.0 −1.1 −2.5 −9.5	– – – –	mA
Output Sink Current	V_{OL} = 0.4 V V_{OL} = 0.5 V V_{OL} = 1.5 V	I_{OL}	5 10 15	1.9 3.5 14	3.8 6.5 25	– – –	mA
Output Rise and Fall Time, 100 mV Overdrive		t_{TLH}, t_{THL}	5 10 15	– – –	75 50 45	150 100 90	ns
Propagation Delay Time, 5 mV Overdrive		t_d	5 10 15	– – –	2.5 3.5 5	5.0 7 10	µs
Propagation Delay Time, 100 mV Overdrive		t_d	5 10 15	– – –	0.6 0.75 0.75	1.2 1.5 1.5	µs
Channel Separation		–	–	–	80	–	dB
Supply Current, Per Pair	(R_L = ∞, V_{in+} = 1.0 V, V_{in-} = 0 V)	I_{DD}	15	–	1.8	2.5	mA

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

The programming current I_{Set} is fixed by an external resistor R_{Set} connected between V_{SS} and either one or both of the I_{Set} pins (8 and 9). When two external programming resistors are used, the set currents for each op amp pair or comparator are given by:

$$I_{Set}\ (\mu A) \approx \frac{V_{DD} - V_{SS} - 1.5}{R_{Set}\ (M\Omega)}$$

Pins 8 and 9 may be tied together for use with a single programming resistor. The set currents for each op amp pair or comparator pair are then given by:

$$I_{Set\ A,\ B} = I_{Set\ C,\ D}\ (\mu A) \approx \frac{V_{DD} - V_{SS} - 1.5}{2\ R_{Set}\ (M\Omega)}$$

The total device current is typically 13 times I_{Set} per pair if the outputs are in the low state, and 5 times I_{Set} per pair if the outputs are in the high state. For op amps with an output in the linear region the device current will be between the values of 5 times and 13 times I_{Set}.

If a pair of op amps is not used, the I_{Set} pin for that pair may be tied to V_{DD} for minimum power consumption. To minimize power consumption in an unused pair of comparators this is not effective. The comparators should use a high value set resistor and the inputs should be set to a voltage that will force the output to V_{DD} (i.e., $+in = V_{DD}$, $-in = V_{SS}$).

It should be noted that increasing I_{Set} for comparators will decrease propagation delay for that comparator.

For operational amplifiers, the maximum obtainable output voltage (V_{OH}) for a given load resistor connected to V_{SS} is given by:

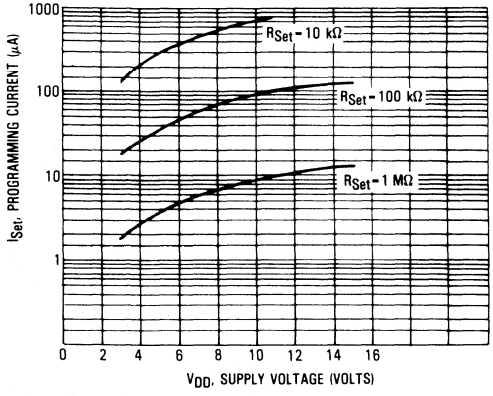
$$V_{OH} = 4 \times I_{Set} \times R_L - 0.05\ V,\ R_L \text{ in } \Omega,\ I_{Set} \text{ in A}$$

Note: V_{OH} Max = V_{DD}

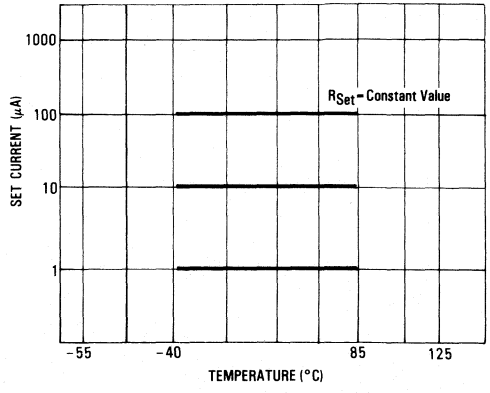
Typical op amp slew rates are given by:

$$S_R \approx 0.04\ I_{Set}\ (V/\mu s),\ I_{Set} \text{ in } \mu A$$

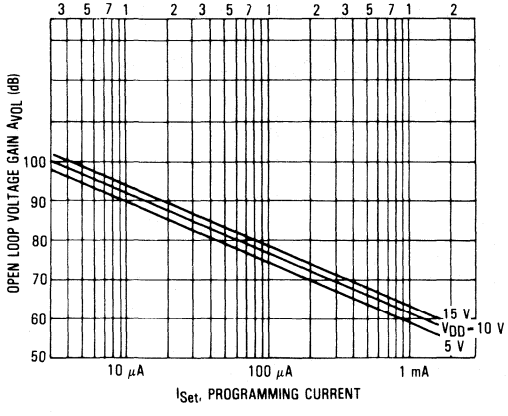
SET CURRENT versus V_{DD}



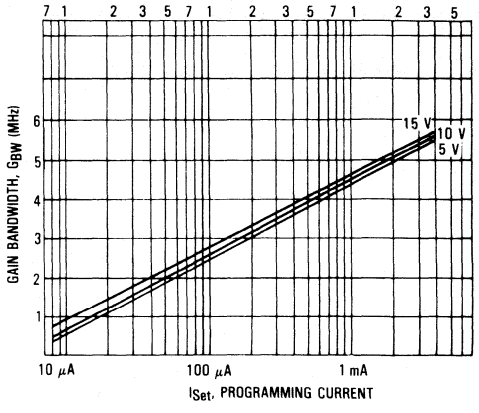
SET CURRENT versus TEMPERATURE



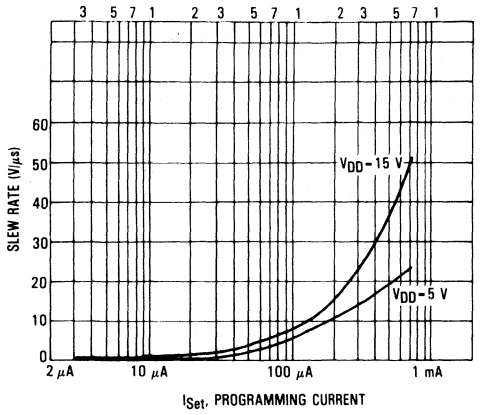
LOW FREQUENCY OPEN LOOP VOLTAGE GAIN versus I_{Set}



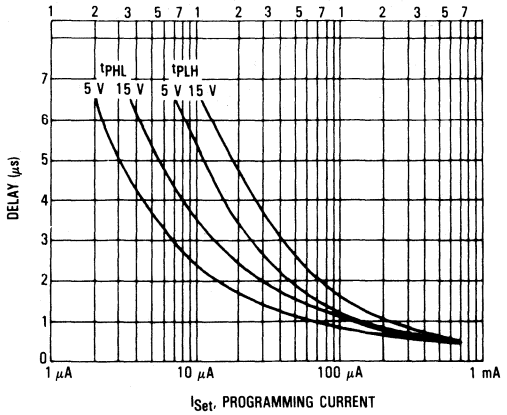
GAIN-BANDWIDTH PRODUCT versus I_{Set}



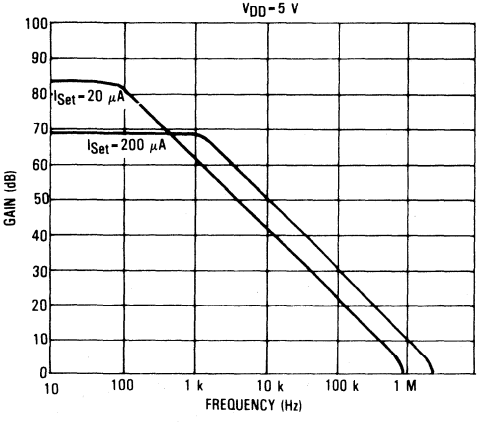
SLEW RATE versus I_{Set}



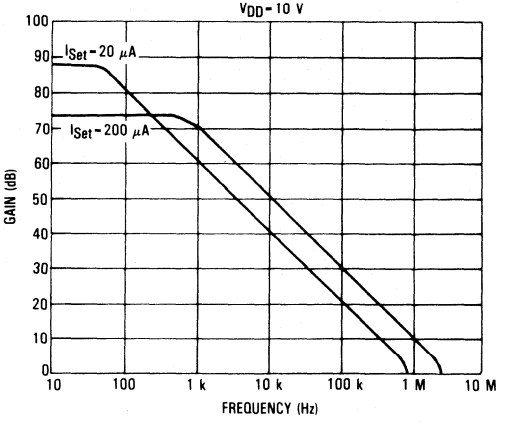
COMPARATOR PROPAGATION DELAY versus I_{Set}
(±50 mV OVERDRIVE)



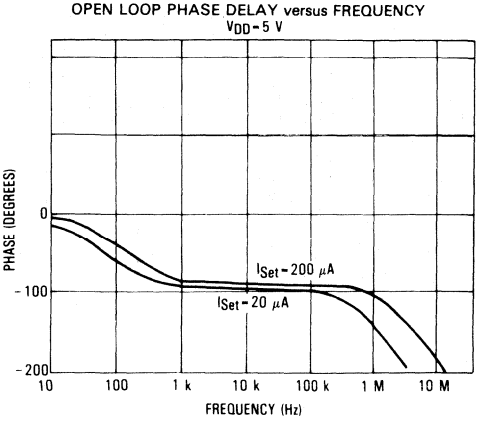
OPEN LOOP GAIN versus FREQUENCY
V_{DD} = 5 V



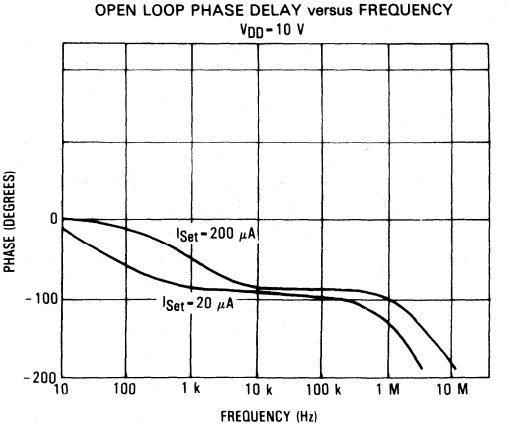
OPEN LOOP GAIN versus FREQUENCY
V_{DD} = 10 V



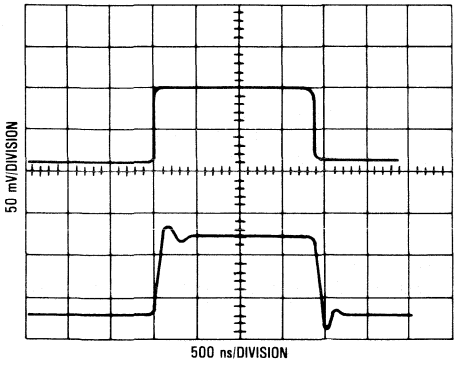
OPEN LOOP PHASE DELAY versus FREQUENCY
V_{DD} = 5 V



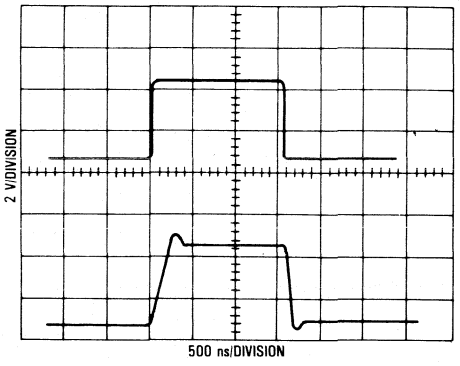
OPEN LOOP PHASE DELAY versus FREQUENCY
V_{DD} = 10 V



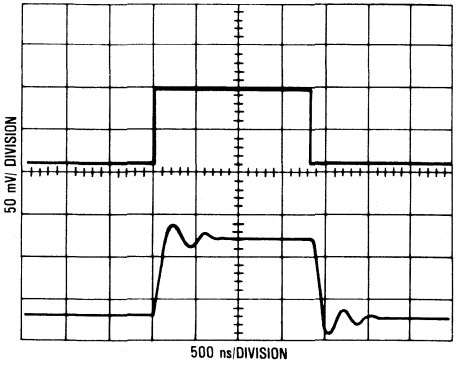
SMALL SIGNAL TRANSIENT RESPONSE
V_{DD} = 10 V NON-INVERTING UNITY GAIN
I_{Set} = 200 μA, V_{in} AVERAGE = 5 V



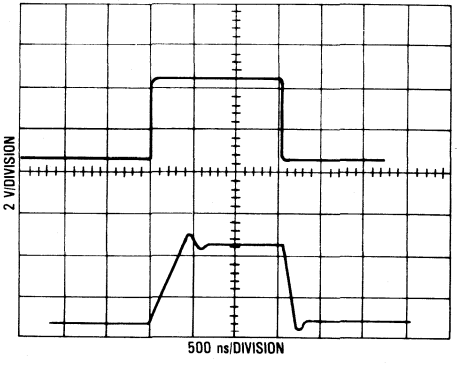
LARGE SIGNAL TRANSIENT RESPONSE
V_{DD} = 10 V NON-INVERTING UNITY GAIN
I_{Set} = 200 μA, V_{in} AVERAGE = 5 V



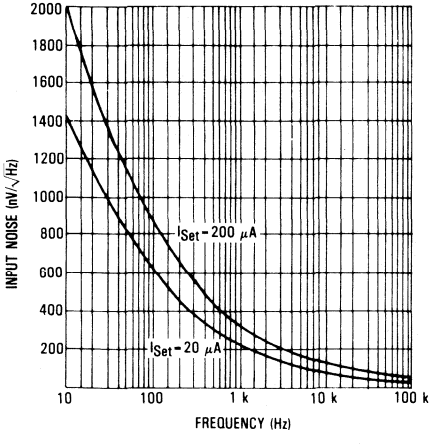
SMALL SIGNAL TRANSIENT RESPONSE
V_{DD} = 10 V NON-INVERTING UNITY GAIN
I_{Set} = 20 μA, V_{in} AVERAGE = 5 V



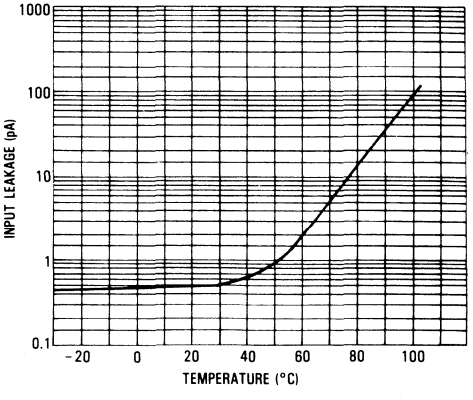
LARGE SIGNAL TRANSIENT RESPONSE
V_{DD} = 10 V NON-INVERTING UNITY GAIN
I_{Set} = 20 μA, V_{in} AVERAGE = 5 V



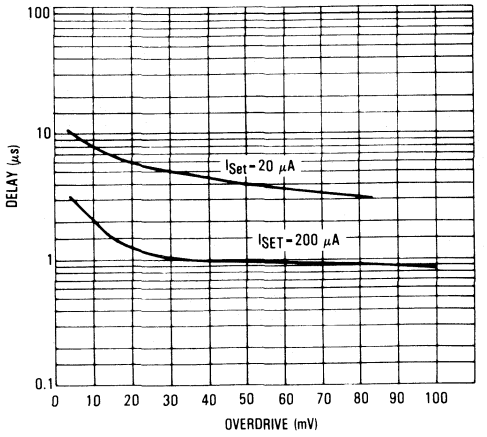
EQUIVALENT INPUT NOISE VOLTAGE (E_N) versus FREQUENCY



TYPICAL INPUT LEAKAGE versus TEMPERATURE
V_{DD} = 15 V V_{in} = 7.5 V

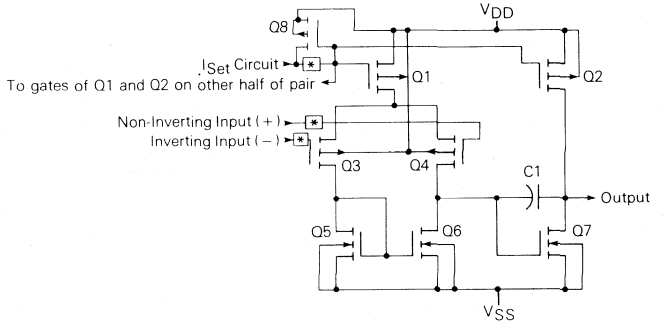


COMPARATOR PROPAGATION DELAY versus OVERDRIVE*
V_{DD} = 10 V, t_{PLH} and t_{PHL}

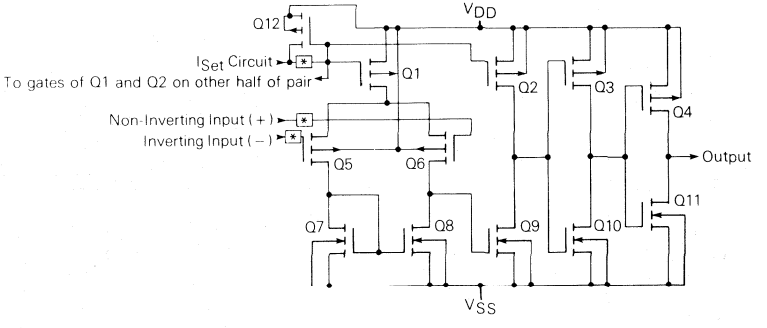


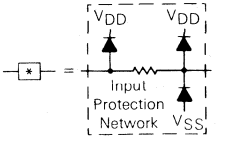
*A 10 mV overdrive is a signal on one input of a comparator that ranges from 10 mV less than the other input to 10 mV more than the other input.

OPERATIONAL AMPLIFIER SCHEMATIC
¼th CIRCUIT



COMPARATOR SCHEMATIC
¼th CIRCUIT





MC14576A
MC14577A

Advance Information

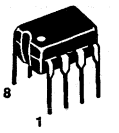
Dual Video Amplifiers
CMOS

Each of these devices contains two amplifiers realized in CMOS. Each amp also employs two lateral NPN bipolar transistors.

The MC14576A contains two internally-compensated operational amplifiers. On-chip gain-setting resistors result in a noninverting voltage gain of 6.0 dB ±1.0 dB at 4.43 MHz for each amp. Each noninverting input of the MC14576A appears as a mostly-capacitive load of about 10 pF.

The MC14577A also contains two internally-compensated operational amplifiers. However, the gain for each amp is adjustable with external components. (The value of the closed-loop voltage gain with a 150 Ω load should not exceed 10 dB at 5 MHz and 6 dB at 10 MHz.) All inputs of the MC14577A appear as mostly-capacitive loads of about 10 pF.

- Direct Drive of 150 Ω Loads
- Maximum Supply Current: 40 mA per Package
- Operating Voltage Range — P Suffix: 5.0 to 12 V Relative to V_{SS}
  F Suffix: 5.0 to 10 V Relative to V_{SS}
- May be used with Single or Dual Supplies
- Operating Temperature Range — P Suffix: –20 to 70°C
  F Suffix: –20 to 50°C
- Excellent Differential Gain: 3% Maximum @ 4.43 MHz
- Excellent Differential Phase: 3° Maximum @ 4.43 MHz
- Guaranteed Bandwidth: 10 MHz
- Minimal External Components Required



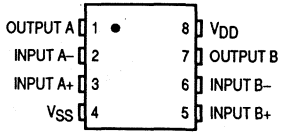
P SUFFIX
PLASTIC DIP
CASE 626

F SUFFIX
SOG PACKAGE
CASE TBD

ORDERING INFORMATION

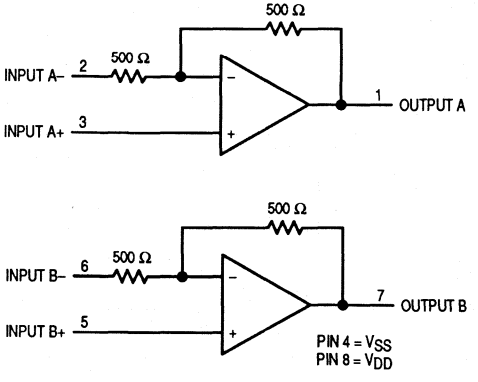
MC14576AP, MC14577AP	Plastic DIP
MC14576AF, MC14577AF	SOG Package

PIN ASSIGNMENT

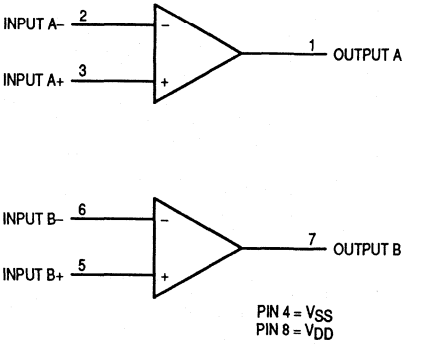


SYMBOLIC REPRESENTATIONS

MC14576A



MC14577A



NOTE: Resistors are shown above with nominal values.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage (Referenced to V_{SS})	–0.5 to +14	V
V_{in}	DC Input Voltage	V_{SS}–0.5 to V_{DD}+0.5	V
V_{out}	DC Output Voltage	V_{SS}–0.5 to V_{DD}+0.5	V
T_{stg}	Storage Temperature	–65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (T_A=25°C, Reference Figures 1 and 2, R_L=150 Ω Unless Otherwise Indicated)

Symbol	Parameter	Test Condition	V_{DD} V	V_{SS} V	Guaranteed Limit	Unit
V_{DD}	Power Supply Voltage Range (Referenced to V_{SS}) P Suffix		—	—	5.0 to 12	V
	F Suffix		—	—	5.0 to 10	
I_{DD}	Maximum Power Supply Current (Per Package)	V_{in} = 0 V, R_L = ∞ (open)	+5.0	–5.0	40	mA
N	Maximum Output Noise	V_{in} = 0 V, BW = 30 Hz to 25 MHz	+5.0	–5.0	250	μV RMS
A_V	Closed-Loop Voltage Gain	V_{in} = 2.0 V p-p, f = 4.43 MHz	+5.0	–5.0	5.0 to 7.0	dB
BW	Bandwidth	V_{in} = 2.0 V p-p, A_V within ±3.0 dB of the gain at 4.43 MHz	+5.0	–5.0	10	MHz
V_{out}	Minimum Output Voltage Swing	V_{in} = 4.0 V p-p, f = 10 MHz	+5.0	–5.0	3.5	V p-p
		V_{in} = 1.5 V p-p, f = 5.0 MHz	+2.5	–2.5	2.0	
—	Maximum Differential Gain	V_{in} = 300 mV p-p biased from –0.5 to +0.5 V, f = 4.43 MHz	+5.0	–5.0	3.0	%
—	Maximum Differential Phase	V_{in} = 300 mV p-p biased from –0.5 to +0.5 V, f = 4.43 MHz	+5.0	–5.0	3.0	Degrees
PSRR	Minimum Power Supply Rejection Ratio, V_{DD} or V_{SS} pins	V_{in} = 0 V, ΔV_{DD} or ΔV_{SS} = 400 mV p-p @ 100 kHz	+5.0	–5.0	43	dB
—	Minimum Channel Separation	V_{in} = 1.0 V p-p, f = 4.43 MHz	+5.0	–5.0	40	dB
C_{in}	Maximum Input Capacitance	V_{in} = 1.0 V p-p, f = 4.43 MHz	+5.0	–5.0	TBD	pF
R_{in}	Minimum Input Resistance, all Inputs except Input A– and Input B– of the MC14576A		+5.0	–5.0	10^{7}**	Ω

**Typical value only; not guaranteed.

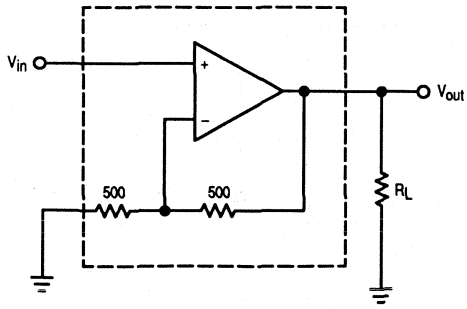


Figure 1. MC14576A Test Circuit

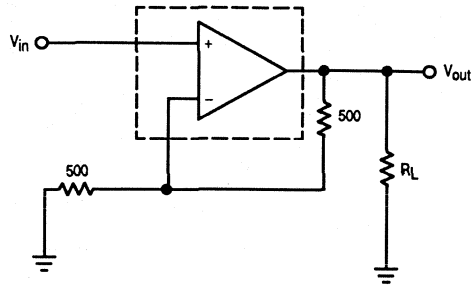


Figure 2. MC14577A Test Circuit

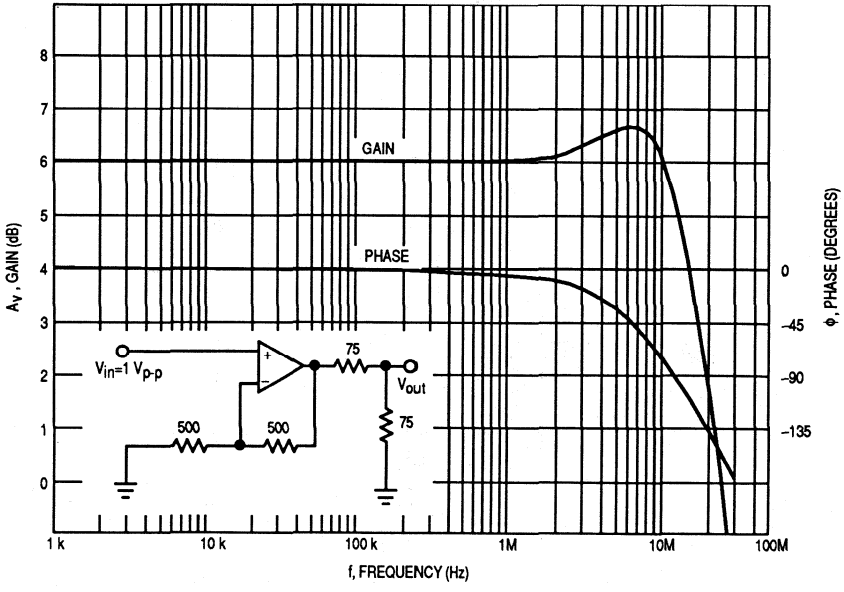


Figure 3. Typical Gain/Phase-Frequency Response (Not Guaranteed)

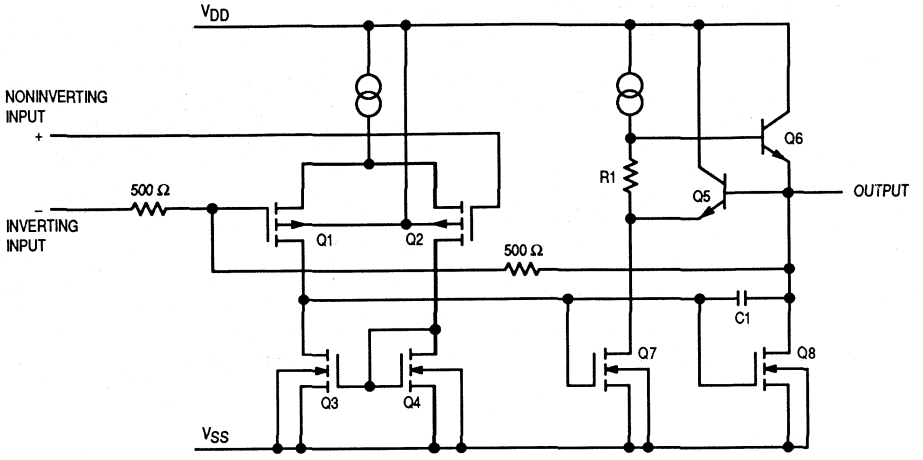


Figure 4. MC14576A Schematic

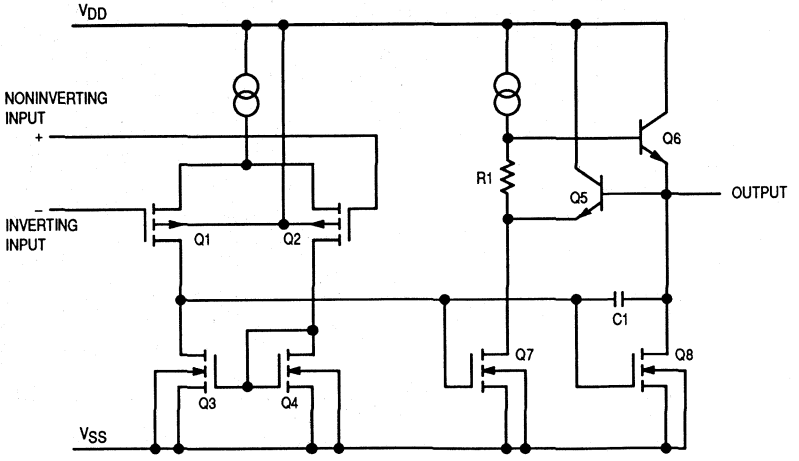


Figure 5. MC14577A Schematic

APPLICATIONS

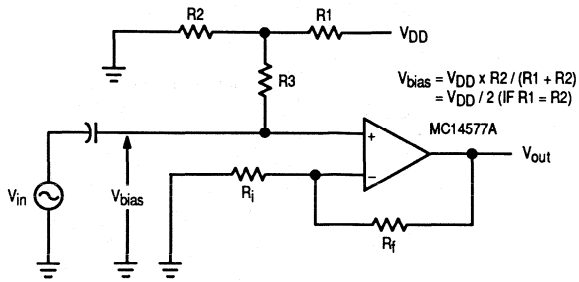


Figure 6. AC-Coupled Noninverting Amplifier with Single-Supply Operation

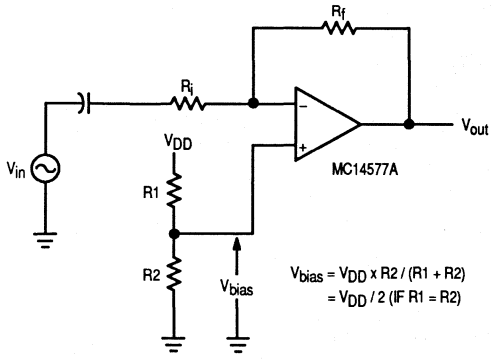


Figure 7. AC-Coupled Inverting Amplifier with Single-Supply Operation

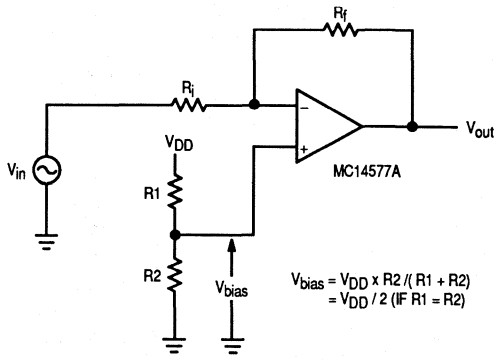


Figure 8. DC-Coupled Inverting Amplifier with Single-Supply Operation

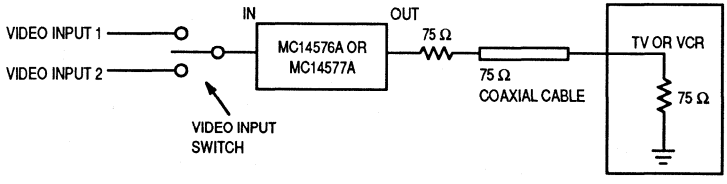


Figure 9. Typical Application of MC14576/77A

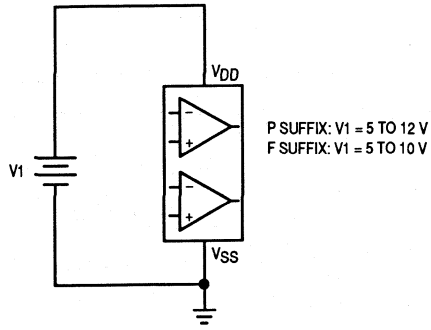


Figure 10. Single-Supply Operation

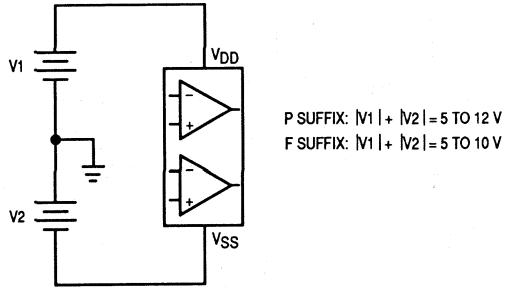


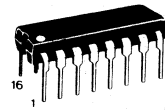
Figure 11. Dual- or Split-Supply Operation

MC14578

Advance Information

Micro-Power Comparator plus Voltage Follower

CMOS



P SUFFIX
PLASTIC DIP
CASE 648

D SUFFIX
SOG
CASE 751B

ORDERING INFORMATION

MC14578P	Plastic DIP
MC14578D	SOG Package

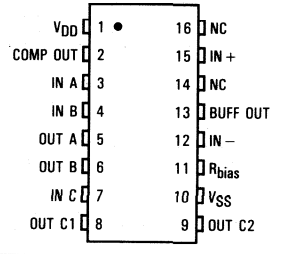
The MC14578 is an analog building block consisting of a very-high input impedance comparator. The voltage follower allows monitoring the noninverting input of the comparator without loading.

Four enhancement-mode MOSFETs are also included on chip. These FETs can be externally configured as open-drain or totem-pole outputs. The drains have on-chip static-protecting diodes. Therefore, the output voltage must be maintained between V_{SS} and V_{DD}.

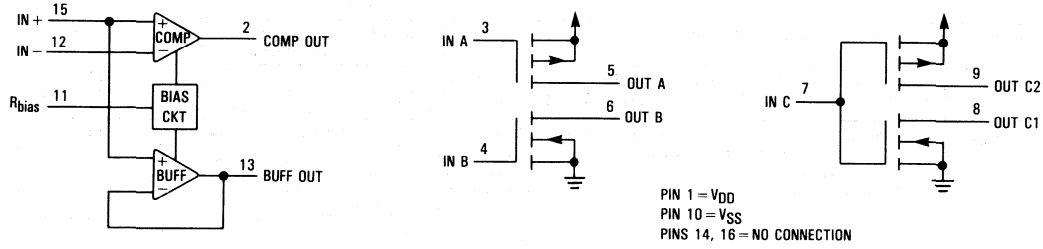
The chip requires one external component. A 3.9 MΩ ± 10% resistor must be connected from the R_{bias} pin to V_{DD}.

- Applications:
  - Pulse Shapers
  - Threshold Detectors
  - Low-Battery Detectors
  - Line-Powered Smoke Detectors
  - Liquid/Moisture Sensors
- DIP Complies with the UL217 and UL268 Specifications
- Operating Voltage Range: 3.5 to 14 V
- Operating Temperature Range: −30° to 70°C
- Input Current (IN+ Pin): ±1 pA @ 25°C (DIP Only)
- Quiescent Current: 10 μA @ 25°C
- Electrostatic Discharge (ESD) Protection Circuitry on All Pins
- Chip Complexity: 26 FETs

PIN ASSIGNMENT



LOGIC DETAIL



PIN 1 = V_{DD}
PIN 10 = V_{SS}
PINS 14, 16 = NO CONNECTION

This document contains information on a new product. Specifications and information herein are subject to change without notice.

PLL Frequency Synthesizers

PLL Frequency Synthesizers (PLL FS)

		Page No.
MC145106	PLL FS (Single-Modulus)	5-3
MC145145-2	4-Bit Data Bus Input PLL FS (Single-Modulus)	5-10
MC145146-2	4-Bit Data Bus Input PLL FS (Dual-Modulus)	5-22
MC145149	Dual PLL FS (Dual-Modulus)	5-34
MC145151-2	Parallel Input PLL FS (Single-Modulus)	5-45
MC145152-2	Parallel Input PLL FS (Dual-Modulus)	5-45
MC145155-2	Serial Input PLL FS (Single-Modulus)	5-45
MC145156-2	Serial Input PLL FS (Dual-Modulus)	5-45
MC145157-2	Serial Input PLL FS (Single-Modulus)	5-45
MC145158-2	Serial Input PLL FS (Dual-Modulus)	5-45
MC145159-1	Serial Input PLL FS with Analog Phase Detector (Dual-Modulus)	5-75
MC145160	Dual PLL FS for 46/49 MHz Cordless Telephones	5-85
MC145166	Dual PLL FS for 46/49 MHz Cordless Telephones	5-85
MC145167	Dual PLL FS for 46/49 MHz Cordless Telephones	5-85
MC145168	Dual PLL FS for 46/49 MHz Cordless Telephones	5-92
MC145169	Dual PLL FS for 46/49 MHz Cordless Telephones	5-92
MC145170	Serial Input PLL FS (VHF)	5-101

SELECTOR GUIDE

Divider Programming Format	External Prescaler Modulus	Single-Ended 3-State Phase Detector Output	Double-Ended Phase Detector Output	Number of Divider Stages +R	+A	+N	f_{max} MHz	Device Number
Serial	Single	√	√	14*	—	14	20	MC145155-2
		√	√	14	—	14	20	MC145157-2
	Dual	√√♦	—	14	7	10	15	MC145149
		√	√	12*	7	10	20	MC145156-2
		√	√	14	7	10	20	MC145158-2
	Dual	Frequency Detector	Analog Detector	14	7	10	15	MC145159-1
	None	√√♦	—	11*	—	14	60	MC145167
		√√♦	—	11*	—	14	60	MC145169
		√	√	15	—	16	160#	MC145170
Parallel	Single	√	—	11*	—	9	4	MC145106
		√	√	14*	—	14	20	MC145151-2
	Dual	—	√	12*	6	10	20	MC145152-2
	None	√√♦	—	12*	—	14	60	MC145160
		√√♦	—	11*	—	14	60	MC145166
		√√♦	—	11*	—	14	60	MC145168
4-Bit Bus	Single	√	√	12	—	14	20	MC145145-2
	Dual	√	√	12	7	10	20	MC145146-2

*Limited number of selectable values.

♦Accommodates two loops per package.
#180 MHz version available. See data sheet.

MC145106

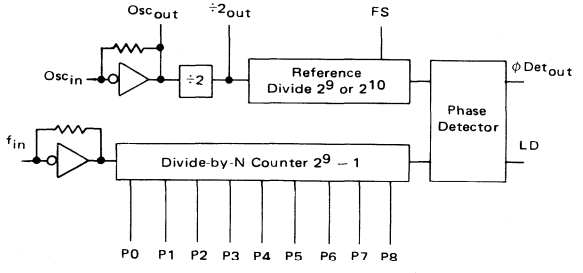
PLL FREQUENCY SYNTHESIZER

The MC145106 is a phase locked loop (PLL) frequency synthesizer constructed in CMOS on a single monolithic structure. This synthesizer finds applications in such areas as CB and FM transceivers. The device contains an oscillator/amplifier, a 2^{10} or 2^{11} divider chain for the oscillator signal, a programmable divider chain for the input signal and a phase detector. The MC145106 has circuitry for a 10.24 MHz oscillator or may operate with an external signal. The circuit provides a 5.12 MHz output signal, which can be used for frequency tripling. A 2^9 programmable divider divides the input signal frequency for channel selection. The inputs to the programmable divider are standard ground-to-supply binary signals. Pull-down resistors on these inputs normally set these inputs to ground enabling these programmable inputs to be controlled from a mechanical switch or electronic circuitry.

The phase detector may control a VCO and yields a high level signal when input frequency is low, and a low level signal when input frequency is high. An out of lock signal is provided from the on-chip lock detector with a "0" level for the out of lock condition.

- Single Power Supply
- Wide Supply Range: 4.5 to 12 V
- Provision for 10.24 MHz Crystal Oscillator
- 5.12 MHz Output
- Programmable Division Binary Input Selects up to 2^9
- On-Chip Pull Down Resistors on Programmable Divider Inputs
- Selectable Reference Divider, 2^{10} or 2^{11} (including ÷ 2)
- Three-State Phase Detector
- See Application Notes AN535 and AR254
- Chip Complexity: 880 FETs or 220 Equivalent Gates

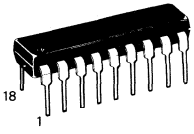
BLOCK DIAGRAM



CMOS MSI

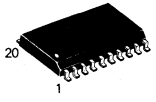
(LOW-POWER COMPLEMENTARY MOS)

PLL
FREQUENCY SYNTHESIZER



P SUFFIX
PLASTIC DIP
CASE 707

FN SUFFIX
PLCC
CASE 775

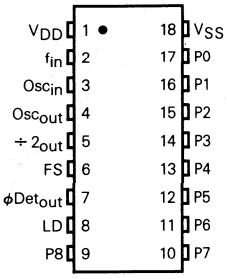


DW SUFFIX
SOG
CASE 751D

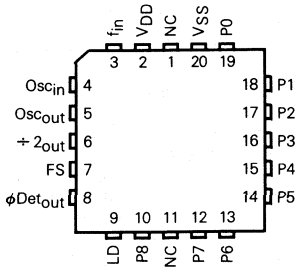
ORDERING INFORMATION

MC145106P	Plastic DIP
MC145106FN	PLCC
MC145106DW	SOG

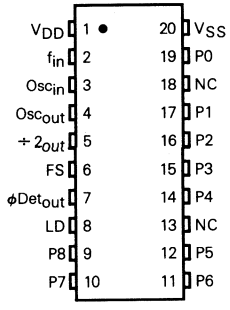
PIN ASSIGNMENTS



PLASTIC DIP



PLCC PACKAGE



SOG PACKAGE

NC = no connection

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +12	V
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} +0.5	V
DC Input Current, per Pin	I	±10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

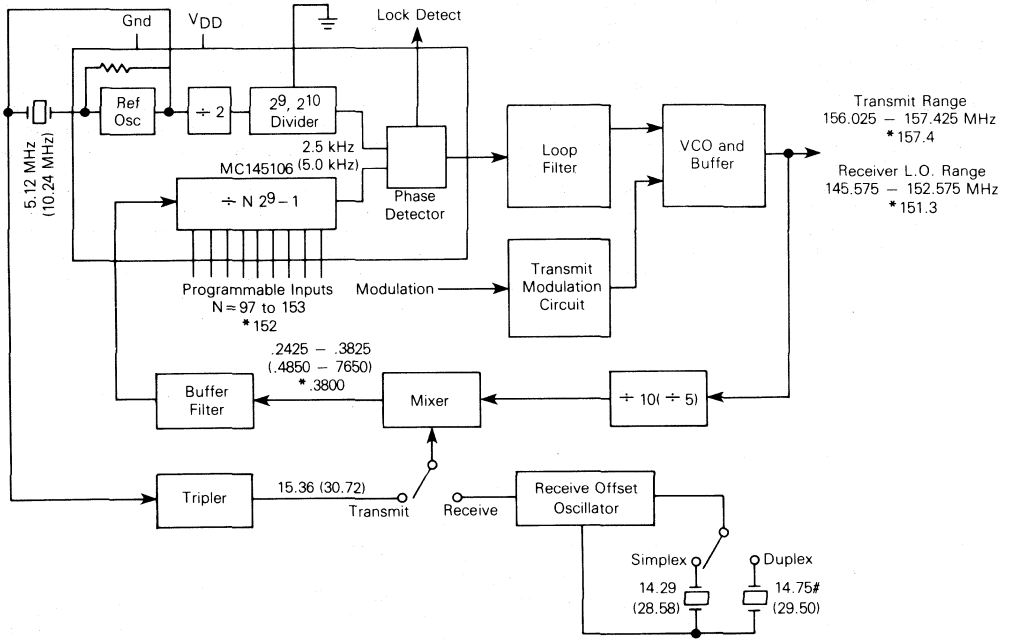
ELECTRICAL CHARACTERISTICS

(T_A = 25°C Unless Otherwise Stated, Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	All Types Min	All Types Typ #	All Types Max	Unit
Power Supply Voltage Range	V_{DD}	–	4.5	–	12	V
Supply Current	I_{DD}	5.0	–	6	10	mA
		10	–	20	35	
		12	–	28	50	
Input Voltage "0" Level	V_{IL}	5.0	–	–	1.5	V
		10	–	–	3.0	
		12	–	–	3.6	
"1" Level	V_{IH}	5.0	3.5	–	–	
		10	7.0	–	–	
		12.	8.4	–	–	
Input Current "0" Level	I_{in}	5.0	−5.0	−20	−50	μA
(FS, Pull-up Resistor Source Current)		10	−15	−60	−150	
		12	−20	−80	−200	
(P0 to P8)		5.0	–	–	−0.3	
		10	–	–	−0.3	
		12	–	–	−0.3	
(FS) "1" Level		5.0	–	–	0.3	
		10	–	–	0.3	
		12	–	–	0.3	
(P0 to P8, Pull-down Resistor Sink Current)		5.0	7.5	30	75	
		10	22.5	90	225	
		12	30	120	300	
(Osc_{in}, f_{in}) "0" Level		5.0	−2.0	−6.0	−15	
		10	−6.0	−25	−62	
		12	−9.0	−37	−92	
(Osc_{in}, f_{in}) "1" Level		5.0	2.0	6.0	15	
		10	6.0	25	62	
		12	9.0	37	92	
Output Drive Current	I_{OH}					mA
(V_O = 4.5 V) Source		5.0	−0.7	−1.4	–	
(V_O = 9.5 V)		10	−1.1	−2.2	–	
(V_O = 11.5 V)		12	−1.5	−3.0	–	
(V_O = 0.5 V) Sink	I_{OL}	5.0	0.9	1.8	–	
(V_O = 0.5 V)		10	1.4	2.8	–	
(V_O = 0.5 V)		12	2.0	4.0	–	
Input Amplitude	–					Vp-p
(f_{in} @ 4.0 MHz)		–	1.0	0.2	–	Sine
(Osc_{in} @10.24 MHz)		–	1.5	0.3		
Input Resistance	R_{in}					MΩ
(Osc_{in}, f_{in})		5.0	–	1.0	–	
		10	–	0.5	–	
		12	–	–	–	
Input Capacitance	C_{in}					pF
(Osc_{in}, f_{in})		–	–	6.0		
Three State Leakage Current	I_{OZ}	5.0	–	–	1.0	μA
(ψ Det_{out})		10	–	–	1.0	
		12	–	–	1.0	
Input Frequency	f_{in}	4.5	0	–	4.0	MHz
(−40°C to +85°C)		12	0	–	4.0	
Oscillator Frequency	Osc_{in}	4.5	0.1	–	10.24	MHz
(−40°C to +85°C)		12	0.1	–	10.24	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

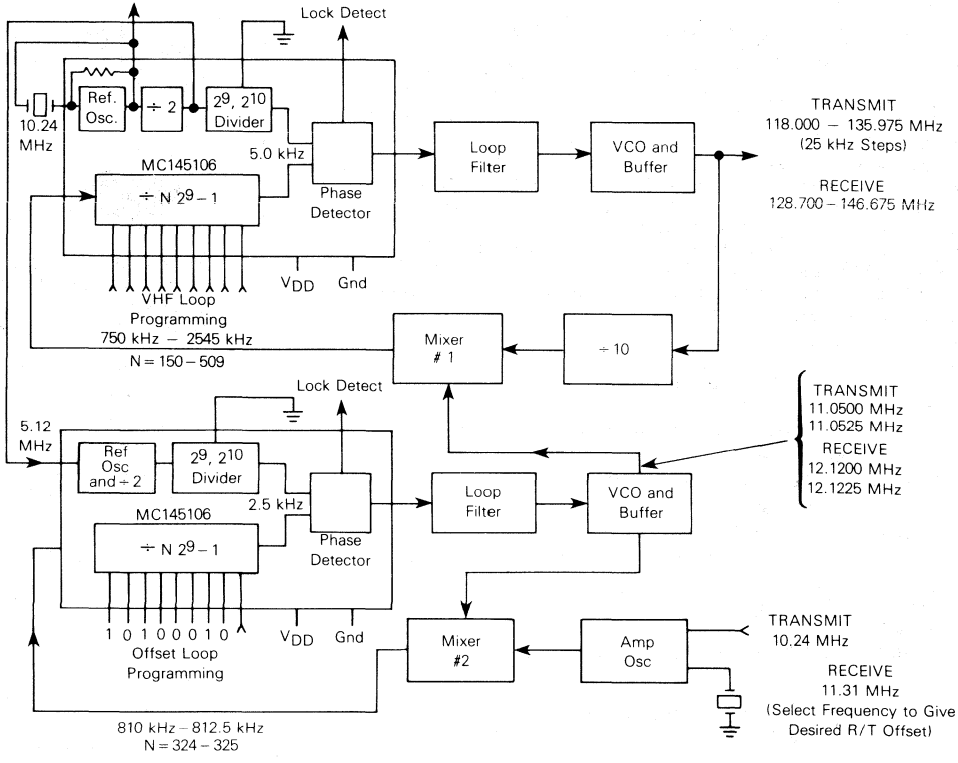
FIGURE 4 – VHF MARINE TRANSCEIVER SYNTHESIZER



NOTES:
- Receiver IF = 10.7 MHz
- Low Side Injection
- Duplex Offset = 4.6 MHz
- Step Size = 25 kHz
- Frequencies in MHz unless noted
- Values in Parentheses are for a 5.0 kHz Reference Frequency
- Example Frequencies for Channel 28 Shown by *

#Can be eliminated by adding 184 to ÷ N for Duplex Channels.

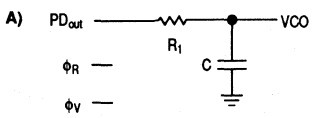
FIGURE 5 — VHF AIRCRAFT 720 CHANNEL TWO CRYSTAL FREQUENCY SYNTHESIZER



DESIGN CONSIDERATIONS

PHASE-LOCKED LOOP—LOW PASS FILTER DESIGN

A)

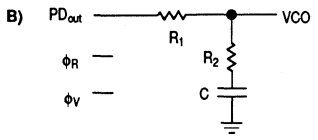


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1sC+1}$$

B)

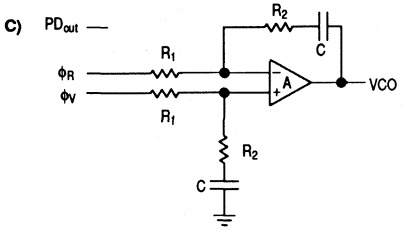


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1+R_2)}}$$

$$\zeta = 0.5\,\omega_n \left(R_2C + \frac{N}{K_\phi K_{VCO}} \right)$$

$$F(s) = \frac{R_2sC+1}{(R_1+R_2)\,sC+1}$$

C)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2sC+1}{R_1sC}$$

NOTE: Sometimes R_1 is split into two series resistors each $R_1 \div 2$. A capacitor C_C is then placed from the midpoint to ground to further filter ϕ_V and ϕ_R. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

DEFINITIONS:

N=Total Division Ratio in feedback loop

K_ϕ (Phase Detector Gain)=$V_{DD}/4\pi$ for PD_{out}

K_ϕ (Phase Detector Gain)=$V_{DD}/2\pi$ for ϕ_V and ϕ_R

K_{VCO} (VCO Gain)= $\dfrac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$

for a typical design w_n (Natural Frequency) $\approx \frac{2\pi fr}{10}$ (at phase detector input).

Damping Factor: $\zeta \cong 1$

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley-Interscience, 1979.

Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley-Interscience, 1980.

Blanchard, Alain, *Phase-Locked Loops: Application to Coherent Receiver Design.* New York, Wiley-Interscience, 1976.

Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley-Interscience, 1981.

Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice-Hall, 1983.

Berlin, Howard M., *Design of Phase-Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.

Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.

AN535, Phase-Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.

AR254, Phase-Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.

BR504/D, Electronic Tuning Address Systems, Motorola Semiconductor Products, Inc., 1986.

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers. The most desirable is discussed first.

USE OF A HYBRID CRYSTAL OSCILLATOR

Commercially available temperature-compensated crystal oscillators (TCXOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or dc coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct-coupled square wave having a rail-to-rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog*, the *Gold Book*, or similar publications.

DESIGN AN OFF-CHIP REFERENCE

The user may design an off-chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), dc coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct-coupled square wave having rail-to-rail voltage swing.

USE OF THE ON-CHIP OSCILLATOR CIRCUITRY

The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 7.

For V_{DD}=5.0 V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8.0 MHz, 20 pF for frequencies in the area of 8.0 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. The shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in}+C_{out}} + C_a + C_o + \frac{C1 \bullet C2}{C1+C2}$$

where

C_{in}=5.0 pF (see Figure 8)
C_{out}=6.0 pF (see Figure 8)
C_a=1.0 pF (see Figure 8)
C_O=the crystal's holder capacitance (see Figure 9)
C1 and C2=external capacitors (see Figure 7)

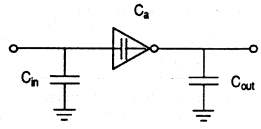
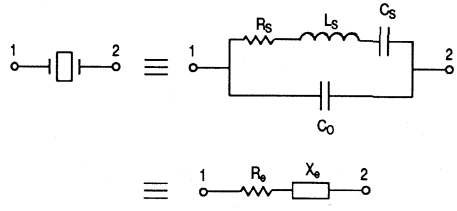
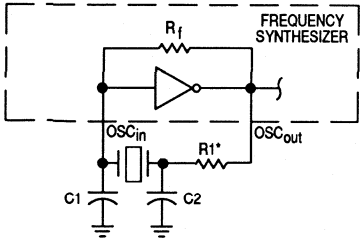


Figure 8. Parasitic Capacitances of the Amplifier



Note: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 9. Equivalent Crystal Networks



*May be deleted in certain cases. See text.

Figure 7. Pierce Crystal Oscillator Circuit

The oscillator can be "trimmed" on-frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. In some cases, stray capacitance should be added to the value for C_{in} and C_{out}.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 9. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damaging or excessive shift in frequency. R1 in Figure 7 limits the drive level. The use of R1 may not be necessary in some cases; i.e., R1=0 ohms.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize load-

DESIGN CONSIDERATIONS

ing.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. See Table 1.

RECOMMENDED READING

Technical Note TN-24, Statek Corp.

Technical Note TN-7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit – Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2 Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro-Technology*, June, 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May, 1966.

Table 1. Partial List of Crystal Manufacturers

Name	Address	Phone
United States Crystal Corp.	3605 McCart St., Ft. Worth, TX 76110	(817) 921-3013
Crystek Crystal	2371 Crystal Dr., Ft. Myers, FL 33907	(813) 936-2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639-7810

Note: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

APPLICATIONS

The features of the MC145145-2 permit bus operation with a dedicated wire needed only for the strobe input. In a microprocessor-controlled system this strobe input is accessed when the phase lock loop is addressed. The remaining data and address inputs will directly interface to the microprocessor's data and address buses.

The +R programmability is used to advantage in Figure 10. Here, the nominal +R value is 3667; but by programming small changes in this value, fine tuning is accomplished. Better tuning resolution is achievable with this method than by changing the +N, due to the use of the large fixed prescaling value of +256 provided by the MC12071.

The two loop synthesizer, in Figure 11, takes advantage of these features to control the phase locked loop with a minimum of dedicated lines while preserving optimal loop performance. Both 25 Hz and 100 Hz steps are provided while the relatively large reference frequencies of 10 kHz or 10.1 kHz are maintained.

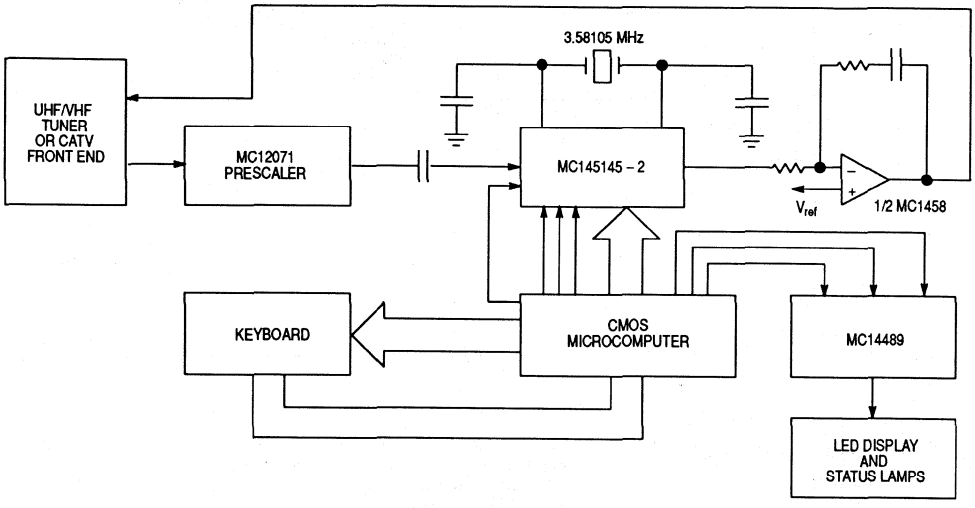
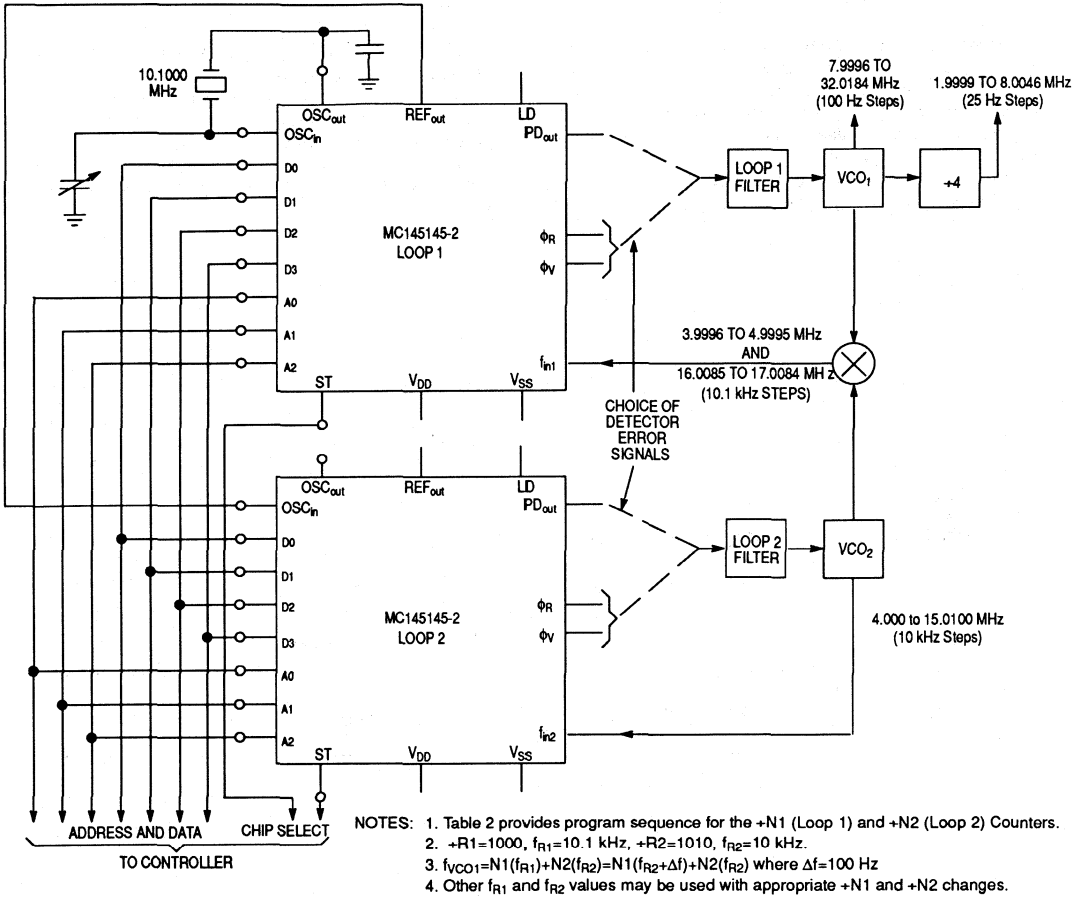


Figure 10. TV/CATV Tuning System



NOTES: 1. Table 2 provides program sequence for the +N1 (Loop 1) and +N2 (Loop 2) Counters.
2. +R1=1000, f_{R1}=10.1 kHz, +R2=1010, f_{R2}=10 kHz.
3. $f_{VCO1}=N1(f_{R1})+N2(f_{R2})=N1(f_{R2}+\Delta f)+N2(f_{R2})$ where Δf=100 Hz
4. Other f_{R1} and f_{R2} values may be used with appropriate +N1 and +N2 changes.

Figure 11. Two Loop Synthesizer Provides 25 and 100 Hz Frequency Steps While Maintaining High Detector Comparison Frequencies of 10 and 10.1 kHz

Table 2. Programming Sequence for Two-Loop Synthesizer of Figure 11

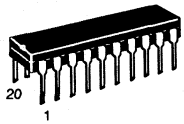
+N1	f_{in1} (MHz)	+N2	f_{VCO2} (MHz)	f_{VCO1} (MHz)
"A" 396 ↓ 397 ↓ 495	"B" 3.9996 ↓ 4.0097 ↓ 4.9995	400 ↓ 399 ↓ 301	4.0000 ↓ 3.9900 ↓ 3.0100	7.9996 ↓ 7.9997 ↓ 8.0095
"A"	"B"	401 ↓ 400 ↓ 303	4.0100 ↓ 4.0000 ↓ 3.0200	8.0096 ↓ 8.0097 ↓ 8.0195
"A"	"B"	"C" 402 ↓ 401 ↓ 303	"D" 4.0200 ↓ 4.0100 ↓ 3.0300	8.0196 ↓ 8.0197 ↓ 8.0295
"A"	"B"	↓ 1500	↓ 15.0000	Increasing In 100 Hz Steps ↓ 19.9995
"A"	"B"	1600 ↓ 1599 ↓ 1501	16.0000 ↓ 15.9900 ↓ 15.0100	19.9996 ↓ 19.9997 ↓ 20.0095
"E" 1585 ↓ 1586 ↓ 1684	"F" 16.0085 ↓ 16.0186 ↓ 17.0084			20.0085 ↓ 20.0086 ↓ 20.0184
"E"	"F"	"C"	"D"	20.0185 ↓ 20.0186 ↓ 20.0284
				Increasing In 100 Hz Steps ↓ 32.0084
"E"	"F"			32.0085 ↓ 32.0086 ↓ 32.0184

Advance Information

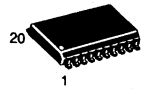
4-Bit Data Bus Input PLL Frequency Synthesizer

Interfaces with Dual-Modulus Prescalers

MC145146-2



P SUFFIX
PLASTIC DIP
CASE 738



DW SUFFIX
SOG
CASE 751D

The MC145146-2 is programmed by a 4-bit input, with strobe and address lines. The device features consist of a reference oscillator, 12-bit programmable reference divider, digital phase detector, 10-bit programmable divide-by-N counter, 7-bit divide-by-A counter and the necessary latch circuitry for accepting the 4-bit input data. When combined with a loop filter and VCO, the MC145146-2 can provide all of the remaining functions for a PLL frequency synthesizer operating up to the device frequency limit. For higher VCO frequency operation, a down mixer or a dual-modulus prescaler can be used between the VCO and the MC145146-2.

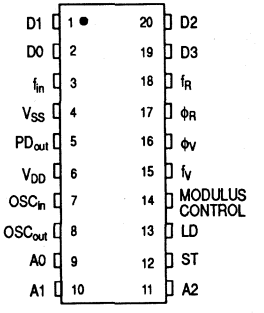
The MC145146-2 is an improved performance drop-in replacement for the MC145146-1. Power consumption has decreased and ESD and latch-up performance have improved.

- General Purpose Applications
  - CATV — TV Tuning
  - AM/FM Radios — Scanning Receivers
  - Two Way Radios — Amateur Radio
- Low Power Consumption Through the Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- Programmable Reference Divider for Values Between 3 and 4095
- On- or Off-Chip Reference Oscillator Operation
- Dual-Modulus 4-Bit Data Bus Programming
- +N Range = 3 to 1023, +A Range=0 to 127
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options:
  - Single Ended (Three State)
  - Double Ended
- Chip Complexity: 5,692 FETs or 1,423 Equivalent Gates

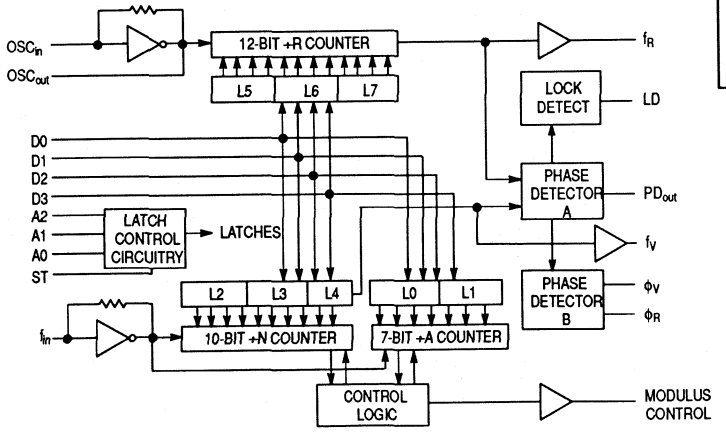
ORDERING INFORMATION

MC145146P2	Plastic DIP
MC145146DW2	SOG Package

PIN ASSIGNMENT



BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +10	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD}+0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
I_{DD}, I_{SS}	Supply Current, V_{DD} or V_{SS} Pins	±30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

† Power Dissipation Temperature Derating:
Plastic DIP: −12 mW/°C from 65°C to 85°C
SOG Package: −7.0 mW/°C from 65°C to 85°C

These devices contain protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to these high-impedance circuits. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}), except for inputs with pullup devices. Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Symbol	Parameter	Test Condition	V_{DD} V	−40°C		25°C		85°C		Unit
				Min	Max	Min	Max	Min	Max	
V_{DD}	Power Supply Voltage Range		—	3.0	9.0	3.0	9.0	3.0	9.0	V
I_{ss}	Dynamic Supply Current	f_{in}=OSC_{in}=10 MHz, 1 Vp-p ac-coupled sine wave R=128, A=32, N=128	3.0	—	3.5	—	3.0	—	3.0	mA
			5.0	—	10	—	7.5	—	7.5	
			9.0	—	30	—	24	—	24	
I_{SS}	Quiescent Supply Current	V_{in}=V_{DD} or V_{SS} I_{out}=0 µA	3.0	—	800	—	800	—	1600	µA
			5.0	—	1200	—	1200	—	2400	
			9.0	—	1600	—	1600	—	3200	
V_{in}	Input Voltage — f_{in}, OSC_{in}	Input ac-coupled sine wave	—	500	—	500	—	500	—	mVp-p
V_{IL}	Low-Level Input Voltage — f_{in}, OSC_{in}	V_{out}≥2.1 V Input dc-coupled square wave	3.0	—	0	—	0	—	0	V
		V_{out}≥3.5 V	5.0	—	0	—	0	—	0	
		V_{out}≥6.3 V	9.0	—	0	—	0	—	0	
V_{IH}	High-Level Input Voltage — f_{in}, OSC_{in}	V_{out}≤0.9 V Input dc-coupled square wave	3.0	3.0	—	3.0	—	3.0	—	V
		V_{out}≤1.5 V	5.0	5.0	—	5.0	—	5.0	—	
		V_{out}≤2.7 V	9.0	9.0	—	9.0	—	9.0	—	
V_{IL}	Low-Level Input Voltage — except f_{in}, OSC_{in}		3.0	—	0.9	—	0.9	—	0.9	V
			5.0	—	1.5	—	1.5	—	1.5	
			9.0	—	2.7	—	2.7	—	2.7	
V_{IH}	High-Level Input Voltage — except f_{in}, OSC_{in}		3.0	2.1	—	2.1	—	2.1	—	V
			5.0	3.5	—	3.5	—	3.5	—	
			9.0	6.3	—	6.3	—	6.3	—	
I_{in}	Input Current (f_{in}, OSC_{in})	V_{in}=V_{DD} or V_{SS}	9.0	±2.0	±50	±2.0	±25	±2.0	±22	µA
I_{IL}	Input Leakage Current (all inputs except f_{in}, OSC_{in})	V_{in}=V_{SS}	9.0	—	−0.3	—	−0.1	—	−1.0	µA
I_{IH}	Input Leakage Current (all inputs except f_{in}, OSC_{in})	V_{in}=V_{DD}	9.0	—	0.3	—	0.1	—	1.0	µA
C_{in}	Input Capacitance		—	—	10	—	10	—	10	pF

(continued)

ELECTRICAL CHARACTERISTICS—continued (Voltages Referenced to V_{SS})

Symbol	Parameter	Test Condition	V_{DD} V	−40°C		25°C		85°C		Unit
				Min	Max	Min	Max	Min	Max	
V_{OL}	Low-Level Output Voltage — OSC_{out}	$I_{out}\approx 0$ µA $V_{in}=V_{DD}$	3.0 5.0 9.0	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	V
V_{OH}	High-Level Output Voltage — OSC_{out}	$I_{out}\approx 0$ µA $V_{in}=V_{SS}$	3.0 5.0 9.0	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	V
V_{OL}	Low-Level Output Voltage — Other Outputs	$I_{out}\approx 0$ µA	3.0 5.0 9.0	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	V
V_{OH}	High-Level Output Voltage — Other Outputs	$I_{out}\approx 0$ µA	3.0 5.0 9.0	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	V
I_{OL}	Low-Level Sinking Current — Modulus Control	$V_{out}=0.3$ V $V_{out}=0.4$ V $V_{out}=0.5$ V	3.0 5.0 9.0	1.3 1.9 3.8	— — —	1.1 1.7 3.3	— — —	0.66 1.08 2.1	— — —	mA
I_{OH}	High-Level Sourcing Current — Modulus Control	$V_{out}=2.7$ V $V_{out}=4.6$ V $V_{out}=8.5$ V	3.0 5.0 9.0	−0.6 −0.9 −1.5	— — —	−0.5 −0.75 −1.25	— — —	−0.3 −0.5 −0.8	— — —	mA
I_{OL}	Low-Level Sinking Current — Lock Detect	$V_{out}=0.3$ V $V_{out}=0.4$ V $V_{out}=0.5$ V	3.0 5.0 9.0	0.25 0.64 1.3	— — —	0.2 0.51 1.0	— — —	0.15 0.36 0.7	— — —	mA
I_{OH}	High-Level Sourcing Current — Lock Detect	$V_{out}=2.7$ V $V_{out}=4.6$ V $V_{out}=8.5$ V	3.0 5.0 9.0	−0.25 −0.64 −1.3	— — —	−0.2 −0.51 −1.0	— — —	−0.15 −0.36 −0.7	— — —	mA
I_{OL}	Low-Level Sinking Current — Other Outputs	$V_{out}=0.3$ V $V_{out}=0.4$ V $V_{out}=0.5$ V	3.0 5.0 9.0	0.44 0.64 1.3	— — —	0.35 0.51 1.0	— — —	0.22 0.36 0.7	— — —	mA
I_{OH}	High-Level Sourcing Current — Other Outputs	$V_{out}=2.7$ V $V_{out}=4.6$ V $V_{out}=8.5$ V	3.0 5.0 9.0	−0.44 −0.64 −1.3	— — —	−0.35 −0.51 −1.0	— — —	−0.22 −0.36 −0.7	— — —	mA
I_{OZ}	Output Leakage Current — PD_{out}	$V_{out}=V_{DD}$ or V_{SS} Output in Off State	9.0	—	±0.3	—	±0.1	—	±1.0	µA
C_{out}	Output Capacitance — PD_{out}	PD_{out} — 3-State	—	—	10	—	10	—	10	pF

AC ELECTRICAL CHARACTERISTICS (C_L=50 pF, Input t_r=t_f=10 ns)

Symbol	Parameter	V_{DD} V	Guaranteed Limit 25°C	Guaranteed Limit −40°C to 85°C	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, f_{in} to Modulus Control (Figures 1 and 6)	3.0 5.0 9.0	110 60 35	120 70 40	ns
t_w	Output Pulse Width, ϕ_R, ϕ_V, and LD with f_R in Phase with f_V (Figures 2 and 6)	3.0 5.0 9.0	25 to 200 20 to 100 10 to 70	25 to 260 20 to 125 10 to 80	ns
t_{TLH}	Maximum Output Transition Time, Modulus Control (Figures 3 and 6)	3.0 5.0 9.0	115 60 40	115 75 60	ns
t_{THL}	Maximum Output Transition Time, Modulus Control (Figures 3 and 6)	3.0 5.0 9.0	60 34 30	70 45 38	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Lock Detect (Figures 3 and 6)	3.0 5.0 9.0	180 90 70	200 120 90	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Other Outputs (Figures 3 and 6)	3.0 5.0 9.0	160 80 60	175 100 65	ns
t_{su}	Minimim Set-Up Time, Data to ST (Figure 4)	3.0 5.0 9.0	10 10 10	TBD TBD TBD	ns
t_{su}	Minimum Set-Up Time, Address to ST (Figure 4)	3.0 5.0 9.0	25 20 15	TBD TBD TBD	ns
t_h	Minimum Hold Time, Address to ST (Figure 4)	3.0 5.0 9.0	10 10 10	TBD TBD TBD	ns
t_h	Minimum Hold Time, Data to ST (Figure 4)	3.0 5.0 9.0	25 20 15	TBD TBD TBD	ns
t_w	Minimum Input Pulse Width, ST (Figure 5)	3.0 5.0 9.0	40 30 20	TBD TBD TBD	ns

SWITCHING WAVEFORMS

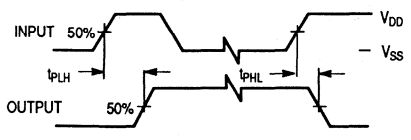


Figure 1.

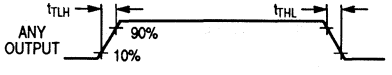


Figure 3.

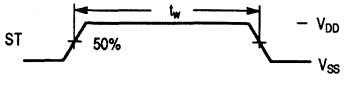


Figure 5.

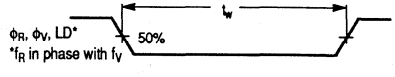


Figure 2.

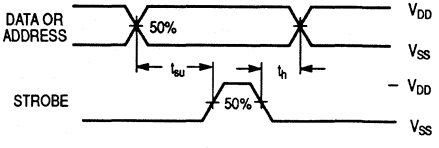
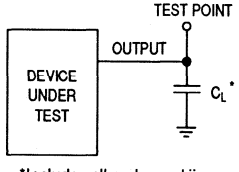


Figure 4.

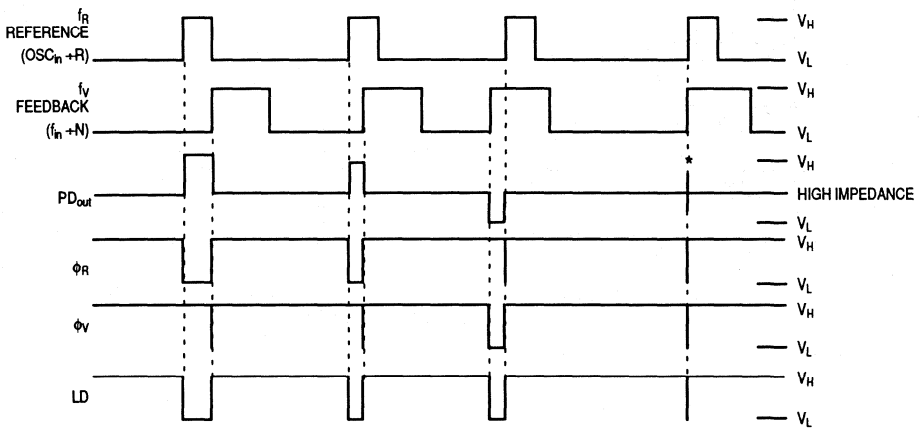


*Includes all probe and jig capacitance.

Figure 6.

FREQUENCY CHARACTERISTICS (Voltages Referenced to V_{SS}, C_L=50 pF, Input t_r=t_f=10 ns unless otherwise specified)

Symbol	Parameter	Test Condition	V_{DD} V	−40°C		25°C		85°C		Unit
				Min	Max	Min	Max	Min	Max	
f_i	Input Frequency (f_{in}, OSC_{in})	R≥8, A≥0, N≥8 V_{in}=500 mVp-p ac-coupled sine wave	3.0 5.0 9.0	— — —	6.0 15 15	— — —	6.0 15 15	— — —	6.0 15 15	MHz
		R≥8, A≥0, N≥8 V_{in}=1.0 Vp-p ac-coupled sine wave	3.0 5.0 9.0	— — —	12 22 25	— — —	12 20 22	— — —	7.0 20 22	MHz
		R≥8, A≥0, N≥8 V_{in}=V_{DD} to V_{SS} dc-coupled square wave	3.0 5.0 9.0	— — —	13 25 25	— — —	12 22 25	— — —	8.0 22 25	MHz



V_H=High voltage level
V_L=Low voltage level
*At this point, when both f_R and f_V are in phase, the output is forced to near mid supply.
Note: The PD_{out} generates error pulses during out-of-lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low pass filter capacitor.

Figure 7. Phase/Frequency Detectors and Lock Detector Output Waveforms

PIN DESCRIPTIONS

DATA INPUTS (Pins 2, 1, 20, 19) — Information at these inputs is transferred to the internal latches when the ST input is in the high state. Pin 19 (D3) is most significant bit.

f_{in} (Pin 3) — Input to +N portion of synthesizer. f_{in} is typically derived from loop VCO and is ac coupled into Pin 3. For larger amplitude signals (standard CMOS-logic levels) dc coupling may be used.

V_{SS} (Pin 4) — Circuit Ground.

PD_{out} (Pin 5) — Three-state output of phase detector for use as loop error signal.

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence:
High-Impedance State

V_{DD} (Pin 6) — The positive supply voltage may range from 3.0 to 9.0 volts with respect to V_{SS}.

OSC_{in}, OSC_{out} (Pin 7 and 8) — These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as input for an externally-generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS-logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

ADDRESS INPUTS (Pins 9, 10, 11) — A0, A1 and A2 are used to define which latch receives the information on the data input lines. The addresses refer to the following latches:

A2	A1	A0	Selected	Function	D0	D1	D2	D
0	0	0	Latch 0	+A Bits	0	1	2	3
0	0	1	Latch 1	+A Bits	4	5	6	—
0	1	0	Latch 2	+N Bits	0	1	2	3
0	1	1	Latch 3	+N Bits	4	5	6	7
1	0	0	Latch 4	+N Bits	8	9	—	—
1	0	1	Latch 5	Reference Bits	0	1	2	3
1	1	0	Latch 6	Reference Bits	4	5	6	7
1	1	1	Latch 7	Reference Bits	8	9	10	11

ST (Pin 12) — The rising edge of strobe transfers data into the addressed latch. The falling edge of strobe latches data into the latch. This pin should normally be held low to avoid loading latches with invalid data.

LD (Pin 13) — Lock detector signal. High level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

MODULUS CONTROL (Pin 14) — Signal generated by the on-chip control logic circuitry for controlling an external dual-modulus prescaler. The modulus control level is low at the beginning of a count cycle and remains low until the + A counter has counted down from its programmed value. At this time, modulus control goes high and remains high until the +N counter has counted the rest of the way down from its programmed value (N-A additional counts since both +N and +A are counting down during the first portion of the cycle). Modulus control is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (N_T)=N•P+A where P and P+1 represent the dual-modulus prescaler divide values respectively for high and low modulus control levels; N the number programmed into the +N counter and A the number programmed into the +A counter.

f_V (Pin 15) — This is the output of the +N counter that is internally connected to the phase detector input. With this output available, the +N counter can be used independently.

ϕ_V, ϕ_R (Pins 16 and 17) — These phase detector outputs can be combined externally for a loop error signal. A single-ended output is also available for this purpose (see PD_{out}).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

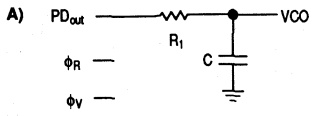
If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

f_R (Pin 18) — This is the output of the +R counter that is internally connected to the phase detector input. With this output available, the +R counter can be used independently.

DESIGN CONSIDERATIONS

PHASE-LOCKED LOOP—LOW PASS FILTER DESIGN

A)

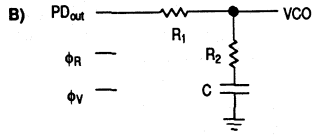


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1sC+1}$$

B)

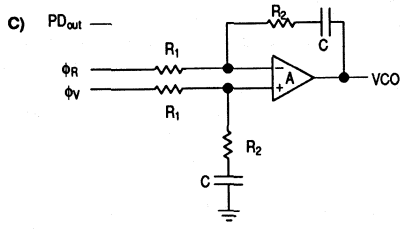


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1+R_2)}}$$

$$\zeta = 0.5\,\omega_n \left(R_2C + \frac{N}{K_\phi K_{VCO}} \right)$$

$$F(s) = \frac{R_2sC+1}{(R_1+R_2)\,sC+1}$$

C)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_nR_2C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2sC+1}{R_1sC}$$

NOTE: Sometimes R_1 is split into two series resistors each R_1+2. A capacitor C_C is then placed from the midpoint to ground to further filter ϕ_V and ϕ_R. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

DEFINITIONS:

N=Total Division Ratio in feedback loop

K_ϕ (Phase Detector Gain)=$V_{DD}/4\pi$ for PD_{out}

K_ϕ (Phase Detector Gain)=$V_{DD}/2\pi$ for ϕ_V and ϕ_R

K_{VCO} (VCO Gain)= $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$

for a typical design w_n (Natural Frequency) $\approx \frac{2\pi fr}{10}$ (at phase detector input).

Damping Factor: $\zeta \cong 1$

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley-Interscience, 1979.
Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley-Interscience, 1980.
Blanchard, Alain, *Phase-Locked Loops: Application to Coherent Receiver Design.* New York, Wiley-Interscience, 1976.
Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley-Interscience, 1981.
Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice-Hall, 1983.
Berlin, Howard M., *Design of Phase-Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.
Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.
AN535, Phase-Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.
AR254, Phase-Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.
BR504/D, Electronic Tuning Address Systems, Motorola Semiconductor Products, Inc., 1986.

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers. The most desirable is discussed first.

USE OF A HYBRID CRYSTAL OSCILLATOR

Commercially available temperature-compensated crystal oscillators (TCXOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or dc coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct-coupled square wave having a rail-to-rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog*, the *Gold Book*, or similar publications.

DESIGN AN OFF-CHIP REFERENCE

The user may design an off-chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), dc coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct-coupled square wave having rail-to-rail voltage swing.

USE OF THE ON-CHIP OSCILLATOR CIRCUITRY

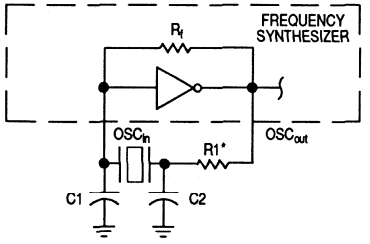
The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 8.

For V_{DD}=5.0 V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8.0 MHz, 20 pF for frequencies in the area of 8.0 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. The shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in}+C_{out}} + C_a + C_o + \frac{C1 \bullet C2}{C1+C2}$$

where

C_{in}=5.0 pF (see Figure 9)
C_{out}=6.0 pF (see Figure 9)
C_a=1.0 pF (see Figure 9)
C_O=the crystal's holder capacitance (see Figure 10)
C1 and C2=external capacitors (see Figure 8)



*May be deleted in certain cases. See text.

Figure 8. Pierce Crystal Oscillator Circuit

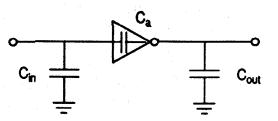
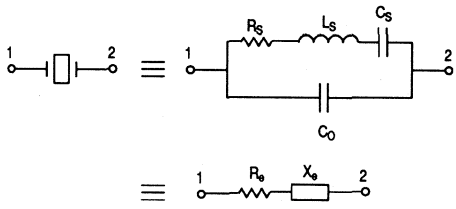


Figure 9. Parasitic Capacitances of the Amplifier



Note: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 10. Equivalent Crystal Networks

The oscillator can be "trimmed" on-frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. In some cases, stray capacitance should be added to the value for C_{in} and C_{out}.

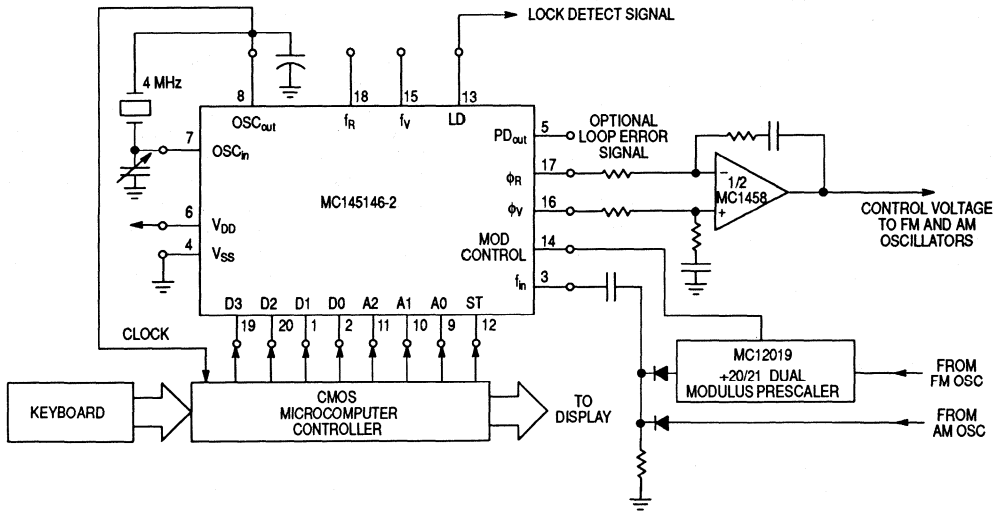
Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 10. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damaging or excessive shift in frequency. R1 in Figure 8 limits the drive level. The use of R1 may not be necessary in some cases; i.e., R1=0 ohms.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize load-

APPLICATIONS

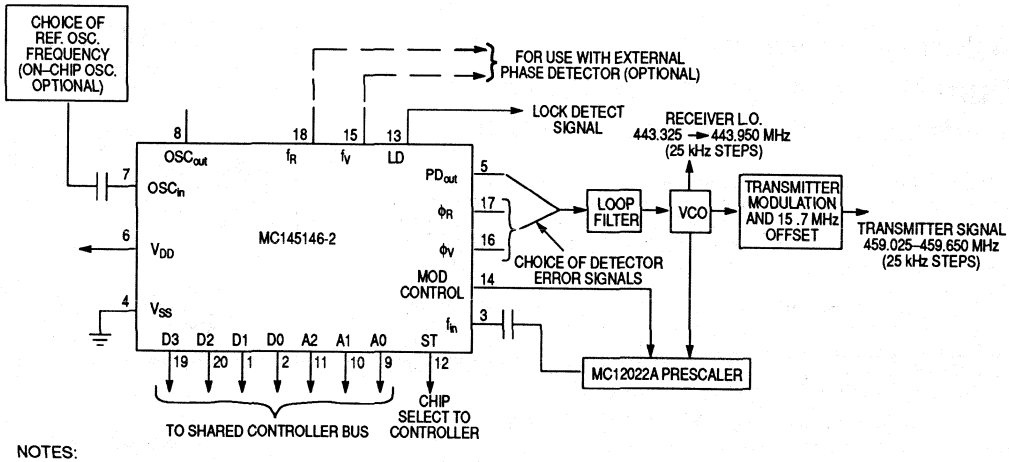
The features of the MC145146-2 permit bus operation with a dedicated wire needed only for the strobe input. In a microprocessor-controlled system this strobe input is accessed when the phase lock loop is addressed. The remaining data and address inputs will directly interface to the microprocessor's data and address buses.

The device architecture allows the user to establish any integer reference divide value between 3 and 4095. The wide selection of +R values permits a high degree of flexibility in choosing the reference oscillator frequency. As a result the reference oscillator can frequently be chosen to serve multiple system functions such as a second local oscillator in a receiver design or a miroprocessor system clock. Typical applications that take advantage of these MC145146-2 features including the dual modulus capability are shown in Figures 11, 12 and 13.



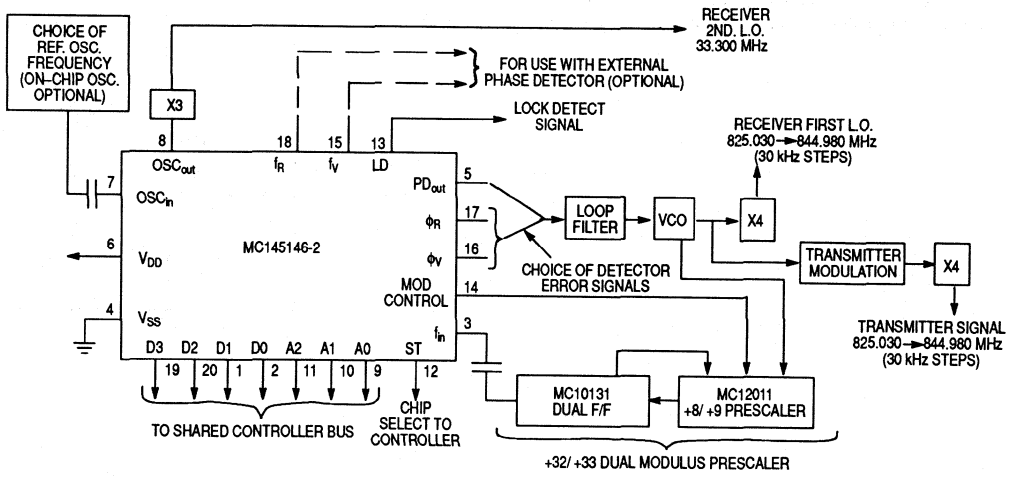
NOTES:
1. For FM: Channel spacing=f_R=25 kHz, R=160.
   For AM: Channel spacing=f_R=1 kHz, R=4000.
2. Various channel spacings and reference oscillator frequencies can be chosen since any R value from 3 to 4095 can be established.
3. Data and address lines are inactive and high impedance when pin 12 is low. Their interface with the controller may therefore be shared with other system functions if desired.

Figure 11. FM/AM Broadcast Radio Synthesizer



NOTES:
1. Receiver I.F.=10.7 MHz, low side injection.
2. Duplex operation with 5 MHz receive/transmit separation.
3. f_R=25 kHz, +R chosen to correspond with desired reference oscillator frequency.
4. N_{total}=17,733 to 17,758=N•P+A; N=277, A=5 to 30 for P=64.

Figure 12. Synthesizer for UHF Mobile Radio Telephone Channels Demonstrates use of the MC145146-2 in Microprocessor/Microcomputer Controlled Systems Operating to Several Hundred MHz



NOTES:
1. Receiver 1st I.F.=45 MHz, low side injection; Receiver 2nd I.F.=11.7 MHz , low side injection.
2. Duplex operation with 45 MHz receive/transmit separation.
3. f_R=7.5 kHz, +R=1480.
4. N_{total}=N•32+A–27,501 to 28,166; N=859 to 880; A=0 to 31.
5. Only one implementation is shown. Various other configurations and dual modulus prescaling values to +128/+129 are possible.

Figure 13. 666 Channel, Computer Controlled, Mobile Radio Telephone Synthesizer for 800 MHz Cellular Radio Systems

Advance Information

Dual PLL Frequency Synthesizer

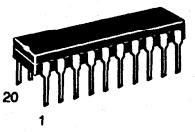
Interfaces with Dual-Modulus Prescalers

MC145149

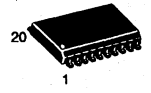
The MC145149 contains two PLL Frequency Synthesizers which share a common serial data port and common reference oscillator. The device contains two 14-stage reference counters, two 10-stage N counters, and two 7-stage A counters. All six counters are fully programmable through a serial port. The divide ratios are latched into the appropriate counter latch according to the last data bits (control bits) entered.

When combined with external low-pass filters and voltage controlled oscillators (VCOs), the MC145149 can provide all the remaining functions for two PLL frequency synthesizers operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or dual-modulus prescaler can be used between the VCO and the synthesizer IC.

- Low Power Consumption Through Use of CMOS Technology
- Wide Operating Voltage Range: 3 to 9 V
- Operating Temperature Range: –40° to 85°C
- ÷R Range=3 to 16,383
- ÷N Range=3 to 1023
- ÷A Range=0 to 127
- Two "Linearized" Three-State Digital Phase Detectors with No Dead Zone
- Two Lock Detect Signals (LD1 and LD2)
- Two Open-Drain Port Expander Outputs (SW1 and SW2)
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs



P SUFFIX
PLASTIC DIP
CASE 738

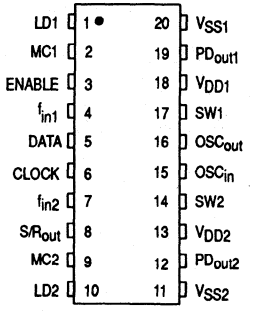


DW SUFFIX
SOG PACKAGE
CASE 751D

ORDERING INFORMATION

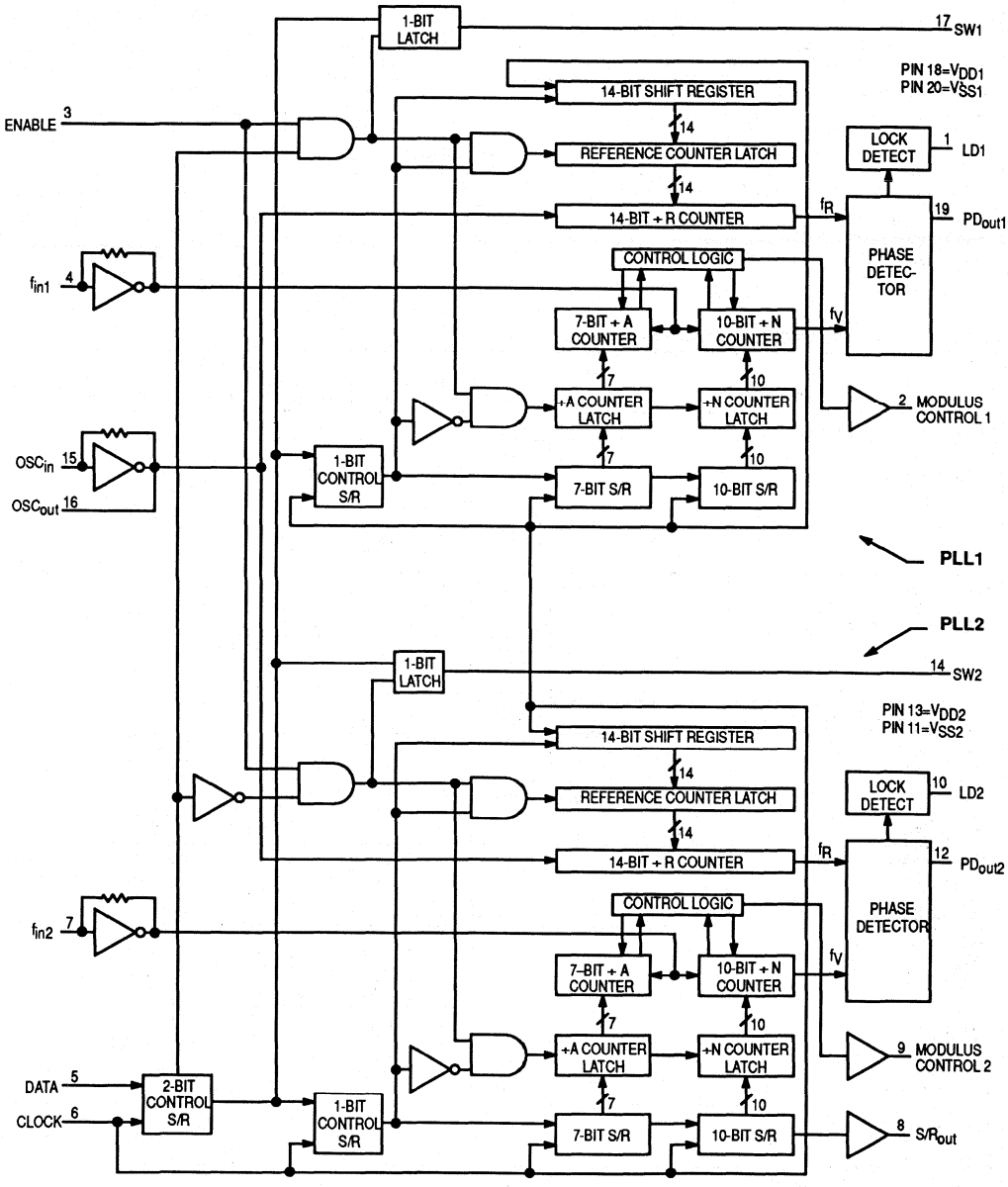
MC145149P	Plastic DIP
MC145149DW	SOG Package

PIN ASSIGNMENT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	–0.5 to +10	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient) except SW1, SW2	–0.5 to V_{DD}+0.5	V
V_{out}	Output Voltage (DC or Transient)—SW1, SW2	–0.5 to 15	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
I_{DD}, I_{SS}	Supply Current, V_{DD} or V_{SS} Pins	±30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	–65 to +150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Power Dissipation Temperature Derating:

Plastic DIP: –12 mW/°C from 65°C to 85°C

SOG Package: –7 mW/°C from 65°C to 85°C

This device contains circuitry to protect against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$ except SW1 and SW2 which may range up to 15 V.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs should be left floating.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} V	–40°C Min	–40°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit
Power Supply Voltage Range		V_{DD}	—	3	9	3	9	3	9	V
Output Voltage V_{in}=0 V or V_{DD} I_{out}=0 µA	0 Level	V_{OL}	3 5 9	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	V
	1 Level	V_{OH}	3 5 9	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	
Input Voltage V_{out}=0.5 V or V_{DD}–0.5 V (All Outputs Except OSC_{out})	0 Level	V_{IL}	3 5 9	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	V
	1 Level	V_{IH}	3 5 9	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	
Output Current—Modulus Control V_{out}=2.7 V V_{out}=4.6 V V_{out}=8.5 V	Source	I_{OH}	3 5 9	–0.60 –0.90 –1.50	— — —	–0.50 –0.75 –1.25	— — —	–0.30 –0.50 –0.80	— — —	mA
V_{out}=0.3 V V_{out}=0.4 V V_{out}=0.5 V	Sink	I_{OL}	3 5 9	1.30 1.90 3.80	— — —	1.10 1.70 3.30	— — —	0.66 1.08 2.10	— — —	
Output Current—SW1, SW2 V_{out}=0.3 V V_{out}=0.4 V V_{out}=0.5 V	Sink	I_{OL}	3 5 9	0.80 1.50 3.50	— — —	0.48 0.90 2.10	— — —	0.24 0.45 1.50	— — —	mA
Output Current—Other Outputs V_{out}=2.7 V V_{out}=4.6 V V_{out}=8.5 V	Source	I_{OH}	3 5 9	–0.44 –0.64 –1.30	— — —	–0.35 –0.51 –1.00	— — —	–0.22 –0.36 –0.70	— — —	mA
V_{out}=0.3 V V_{out}=0.4 V V_{out}=0.5 V	Sink	I_{OL}	3 5 9	0.44 0.64 1.30	— — —	0.35 0.51 1.00	— — —	0.22 0.36 0.70	— — —	
Input Current—Data, Clock Enable		I_{in}	9	—	±0.3	—	±0.1	—	±1.0	µA
Input Current—f_{in}, OSC_{in}		I_{in}	9	—	±50	—	±25	—	±22	µA
Input Capacitance		C_{in}	—	—	10	—	10	—	10	pF
3-State Output Capacitance—PD_{out}		C_{out}	—	—	10	—	10	—	10	pF

(continued)

ELECTRICAL CHARACTERISTICS—continued (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} V	−40°C		25°C		85°C		Unit
			Min	Max	Min	Max	Min	Max	
Quiescent Current V_{in}=0 V or V_{DD} I_{out}=0 μA	I_{DD}	3 5 9	— — —	800 1200 1600	— — —	800 1200 1600	—	1600 2400 3200	μA
3-State Leakage Current—PD_{out} V_{out}=0 V or 9 V	I_{OZ}	9	—	±0.3	—	±0.1	—	±3.0	μA
Off-State Leakage Current—SW1, SW2 V_{out}=9 V	I_{OZ}	9	—	0.3	—	0.1	—	3.0	μA

SWITICHING CHARACTERISTICS (T_A=25°C, C_L=50 pF)

Characteristic	Symbol	V_{DD}	Min	Max	Unit
Output Rise Time, Modulus Control (Figures 1 and 6)	t_{TLH}	3 5 9	— — —	115 60 40	ns
Output Fall Time, Modulus Control (Figures 1 and 6)	t_{THL}	3 5 9	— — —	60 34 30	ns
Output Rise and Fall Time, LD, S/R_{out} (Figures 1 and 6)	t_{TLH}, t_{THL}	3 5 9	— — —	140 80 60	ns
Propagation Delay Time f_{in} to Modulus Control (Figures 2 and 6)	t_{PLH}, t_{PHL}	3 5 9	— — —	125 80 50	ns
Setup Times Data to Clock (Figure 3)	t_{su}	3 5 9	30 20 18	— — —	ns
Clock to Enable (Figure 3)		3 5 9	70 32 25	— — —	
Hold Time Clock to Data (Figure 3)	t_h	3 5 9	12 12 15	— — —	ns
Recovery Time Enable to Clock (Figure 3)	t_{rec}	3 5 9	5 10 20	— — —	ns
Input Rise and Fall Times Any Input (Figure 4)	t_r, t_f	3 5 9	— — —	5 2 0.5	μs
Input Pulse Width, Enable, Clock (Figure 5)	t_w	3 5 9	40 35 25	— — —	ns

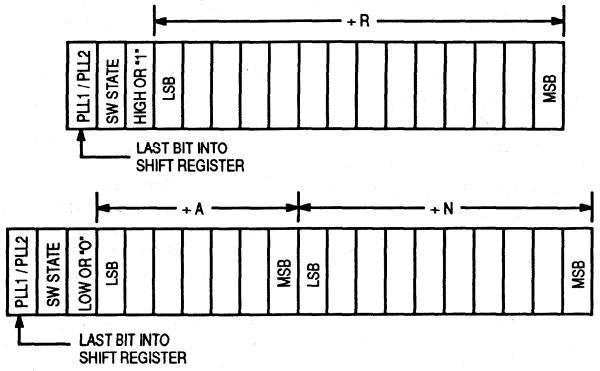
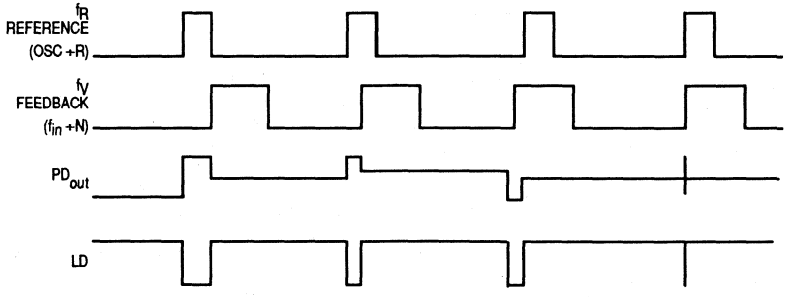
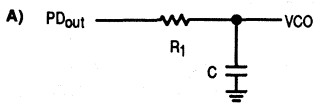


Figure 7. Bit Stream Formats



Note: The PD output state is equal to either V_{DD} or V_{SS} when active. When not active, the output is high impedance and the voltage at that pin is determined by the low pass filter capacitor.

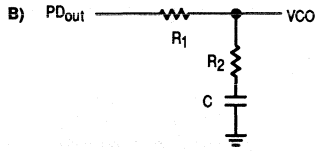
Figure 8. Phase Detector/Lock Detector Output Waveforms



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1sC+1}$$



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1+R_2)}}$$

$$\zeta = 0.5\,\omega_n \left(R_2C + \frac{N}{K_\phi K_{VCO}} \right)$$

$$F(s) = \frac{R_2sC+1}{(R_1+R_2)\,sC+1}$$

DEFINITIONS:

N=Total Division Ratio in feedback loop

K_ϕ (Phase Detector Gain)=$V_{DD}/4\pi$ for PD_{out}

K_{VCO} (VCO Gain)= $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$

for a typical design w_n (Natural Frequency) $\approx \frac{2\pi fr}{10}$ (at phase detector input).

Damping Factor: $\zeta \cong 1$

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley-Interscience, 1979.
Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley-Interscience, 1980.
Blanchard, Alain, *Phase-Locked Loops: Application to Coherent Receiver Design.* New York, Wiley-Interscience, 1976.
Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley-Interscience, 1981.
Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice-Hall, 1983.
Berlin, Howard M., *Design of Phase-Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.
Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.
AN535, Phase-Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.
AR254, Phase-Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.
BR504/D, Electronic Tuning Address Systems, Motorola Semiconductor Products, Inc., 1986.

Figure 9. Phase-Locked Loop Low- Pass Filter Design

DESIGN CONSIDERATIONS

DUAL-MODULUS PRESCALING

OVERVIEW

The technique of dual-modulus prescaling is well established as a method of achieving high performance frequency synthesizer operation at high frequencies. Basically, the approach allows relatively low-frequency programmable counters to be used as high-frequency programmable counters with speed capability of several hundred MHz. This is possible without the sacrifice in system resolution and performance that results if a fixed (single-modulus) divider is used for the prescaler.

In dual-modulus prescaling, the lower speed counters must be uniquely configured. Special control logic is necessary to select the divide value P or P+1 in the prescaler for the required amount of time (see modulus control definition). Motorola's dual-modulus frequency synthesizers contain this feature and can be used with a variety of dual-modulus prescalers to allow speed, complexity and cost to be tailored to the system requirements. Prescalers having P, P+1 divide values in the range of +3/+4 to +128/+129 can be controlled by most Motorola frequency synthesizers.

Several dual-modulus prescaler approaches suitable for use with the MC145149 are:

MC12009	+5/+6	440 MHz
MC12011	+8/+9	500 MHz
MC12013	+10/+11	500 MHz
MC12015	+32/+33	225 MHz
MC12016	+40/+41	225 MHz
MC12017	+64/+65	225 MHz
MC12018	+128/+129	520 MHz
MC12022A	+64/65 or +128/129	1.1 GHz
MC12032A	+64/65 or +128/129	2.0 GHz

DESIGN GUIDELINES

The system total divide value, N_{total} (N_T) will be dictated by the application, i.e.

$$N_T = \frac{\text{frequency into the prescaler}}{\text{frequency into the phase detector}} = N \bullet P + A$$

N is the number programmed into the +N counter, A is the number programmed into the +A counter, P and P+1 are the two selectable divide ratios available in the dual-modulus prescalers. To have a range of N_T values in sequence, the +A counter is programmed from zero through P–1 for a particular value N in the +N counter. N is then incremented to N+1 and the +A is sequenced from zero through P–1 again.

There are minimum and maximum values that can be achieved for N_T. These values are a function of P and the size of the +N and +A counters. The constraint $N \geq A$ always applies. If $A_{max}=P-1$, then $N_{min} \geq P-1$. Then $N_T min=(P-1)\ P+A$ or $(P-1)\ P$ since A is free to assume the value of zero.

$$N_T max = N_{max} \bullet P + A_{max}$$

To maximize system frequency capability, the dual-modulus prescaler output must go from low to high after each group of P or P+1 input cycles. The prescaler should divide by P when its modulus control line is high and by P+1 when its modulus control is low.

For the maximum frequency into the prescaler ($f_{VCO}max$), the value used for P must be large enough such that:

A. f_{VCO} max divided by P may not exceed the frequency capability of f_{in} (input to the +N and +A counters).

B. The period of f_{VCO} divided by P must be greater than the sum of the times:
   a. Propagation delay through the dual-modulus prescaler.
   b. Prescaler setup or release time relative to its modulus control signal.
   c. Propagation time from f_{in} to the modulus control output for the frequency synthesizer device.

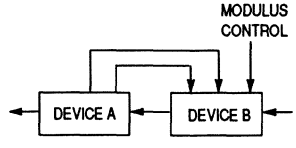
A sometimes useful simplification in the programming code can be achieved by choosing the values for P of 8, 16, 32, or 64. For these cases, the desired value of N_T results when N_T in binary is used as the program code to the +N and +A counters treated in the following manner:

A. Assume the +A counter contains "a" bits where $2^a \geq P$.

B. Always program all higher order +A counter bits above "a" to zero.

C. Assume the +N counter and the +A counter (with all the higher order bits above "a" ignored) combined into a single binary counter of n+a bits in length (n=number of divider stages in the +N counter). The MSB of this "hypothetical" counter is to correspond to the MSB of +N and the LSB is to correspond to the LSB of +A. The system divide value, N_T, now results when the value of N_T in binary is used to program the "new" n+a bit counter.

By using the two devices, several dual-modulus values are achievable:



DEVICE A \ DEVICE B	MC12009	MC12011	MC12013
MC10131	+20/+21	+32/+33	+40/+41
MC10138	+50/+51	+80/+81	+100/+101
MC10154	+40/+41 OR +80/+81	+64/+65 OR +128/+129	+80/+81

NOTE: MC12009, MC12011, and MC12013 are pin equivalent.
MC12015, MC12016, and MC12017 are pin equivalent.

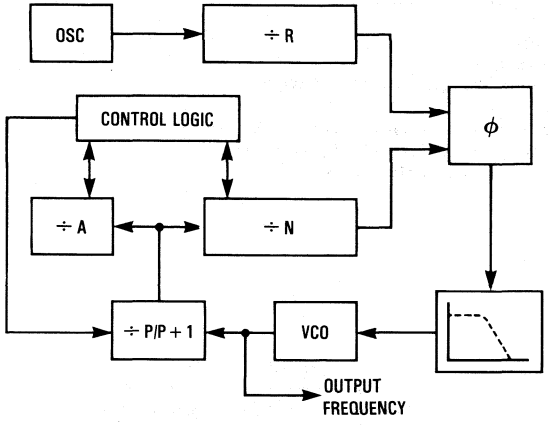
MC145151-2
MC145152-2
MC145155-2
MC145156-2
MC145157-2
MC145158-2

PLL Frequency Synthesizers
CMOS

The devices described in this document are typically used as low-power, phase-locked loop frequency synthesizers. When combined with an external low-pass filter and voltage-controlled oscillator, these devices can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a prescaler can be used between the VCO and the synthesizer IC.

These frequency synthesizer chips can be found in the following and other applications:

CATV	TV Tuning
AM/FM Radios	Scanning Receivers
Two-Way Radios	Amateur Radio



CONTENTS

Page

DEVICE DETAIL SHEETS
MC145151-2 Parallel-Input, Single-Modulus 2
MC145152-2 Parallel-Input, Dual-Modulus 5
MC145155-2 Serial-Input, Single-Modulus 9
MC145156-2 Serial-Input, Dual-Modulus 12
MC145157-2 Serial-Input, Single-Modulus 16
MC145158-2 Serial-Input, Dual-Modulus 19

FAMILY CHARACTERISTICS
Maximum Ratings 22
DC Electrical Characteristics 22
AC Electrical Characteristics 24
Timing Requirements 25
Frequency Characteristics 26
Phase Detector/Lock Detector Output Waveforms 26

DESIGN CONSIDERATIONS
Phase-Locked Loop—Low Pass Filter Design 27
Crystal Oscillator Considerations 28
Dual-Modulus Prescaling 30

MC145151-2

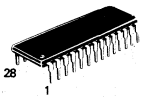
Parallel-Input PLL Frequency Synthesizer

Interfaces with Single-Modulus Prescalers

The MC145151-2 is programmed by 14 parallel input-data lines for the N counter and 3 input lines for the R counter. The device features consist of a reference oscillator, selectable-reference divider, digital-phase detector, and 14-bit programmable divide-by-N counter.

The MC145151-2 is an improved-performance drop-in replacement for the MC145151-1. The power consumption has decreased and ESD and latch-up performance have improved.

- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On- or Off-Chip Reference Oscillator Operation
- Lock Detect Signal
- ÷ N Counter Output Available
- Single Modulus/Parallel Programming
- 8 User-Selectable ÷ R Values: 8, 128, 256, 512, 1024, 2048, 2410, 8192
- ÷ N Range = 3 to 16383
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options: Single Ended (Three-State) or Double Ended
- Chip Complexity: 8000 FETs or 2000 Equivalent Gates



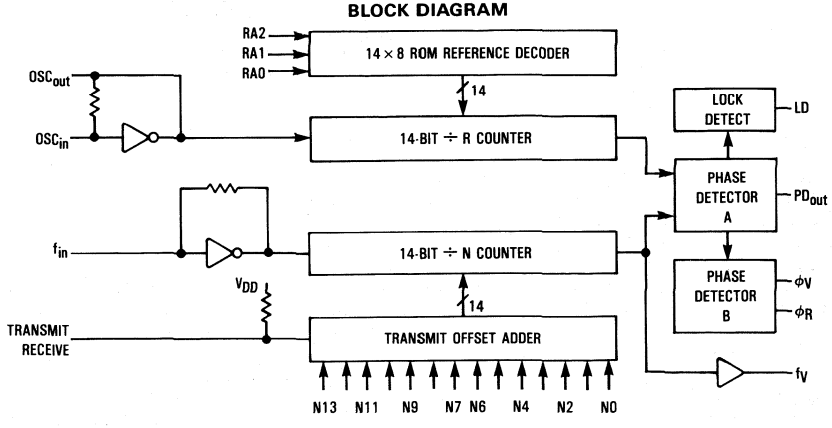
P SUFFIX
PLASTIC
CASE 710

FN SUFFIX
PLCC
CASE 776

ORDERING INFORMATION

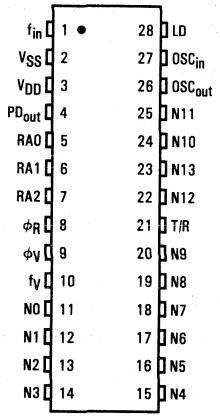
MC145151P2	Plastic DIP
MC145151FN2	PLCC Package

BLOCK DIAGRAM

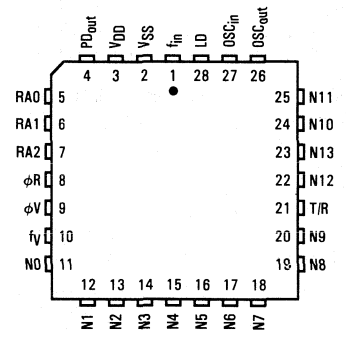


NOTE: N0 through N13 inputs and inputs RA0, RA1, and RA2 have pullup resistors not shown.

PIN ASSIGNMENTS



PLASTIC DIP



PLCC PACKAGE

PIN DESCRIPTIONS

INPUTS

f_{in}—Frequency Input

Input to the ÷ N portion of the synthesizer. f_{in} is typically derived from loop VCO and is ac coupled into the device. For larger amplitude signals (standard CMOS logic levels) dc coupling may be used.

RA0, RA1, RA2—Reference Address Inputs

These three inputs establish a code defining one of eight possible divide values for the total reference divider, as defined by the table below.

Pullup resistors ensure that inputs left open remain at a logic one and require only a SPST switch to alter data to the zero state.

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	8
0	0	1	128
0	1	0	256
0	1	1	512
1	0	0	1024
1	0	1	2048
1	1	0	2410
1	1	1	8192

N Inputs—N Counter Programming Inputs

These inputs provide the data that is preset into the ÷ N counter when it reaches the count of zero. N0 is least significant and N13 is most significant. Pullup resistors ensure that inputs left open remain at a logic one and require only a SPST switch to alter data to the zero state.

Transmit/Receive—Offset Adder Input

This input controls the offset added to the data provided at the N inputs. This is normally used for offsetting the VCO frequency by an amount equal to the IF frequency of the transceiver. This offset is fixed at 856 when T/R is low and gives no offset when T/R is high. A pullup resistor ensures that no connection will appear as a logic one causing no offset addition.

OSC_{in}, OSC_{out}—Reference Oscillator Input/Output

These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally-generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

OUTPUTS

PD_{out}—Phase Detector A Output

Three-state output of phase detector for use as loop error signal. Double-ended outputs are also available for this purpose (see ϕ_V and ϕ_R).

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High-Impedance State

ϕ_R, ϕ_V—Phase Detector B Outputs

These phase detector outputs can be combined externally for a loop-error signal. A single-ended output is also available for this purpose (see PD_{out}).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

f_V—N Counter Output

This is the buffered output of the ÷ N counter that is internally connected to the phase detector input. With this output available, the ÷ N counter can be used independently.

LD—Lock Detector Output

Lock detector signal. Essentially a high level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

POWER SUPPLY

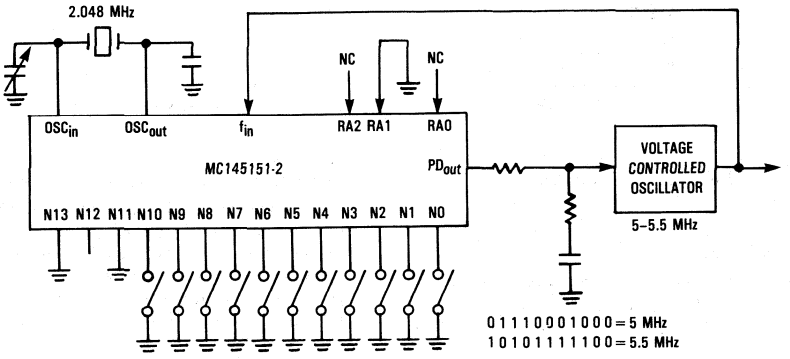
V_{DD}

The positive power supply potential. This pin may range from +3 to +9 V with respect to V_{SS}.

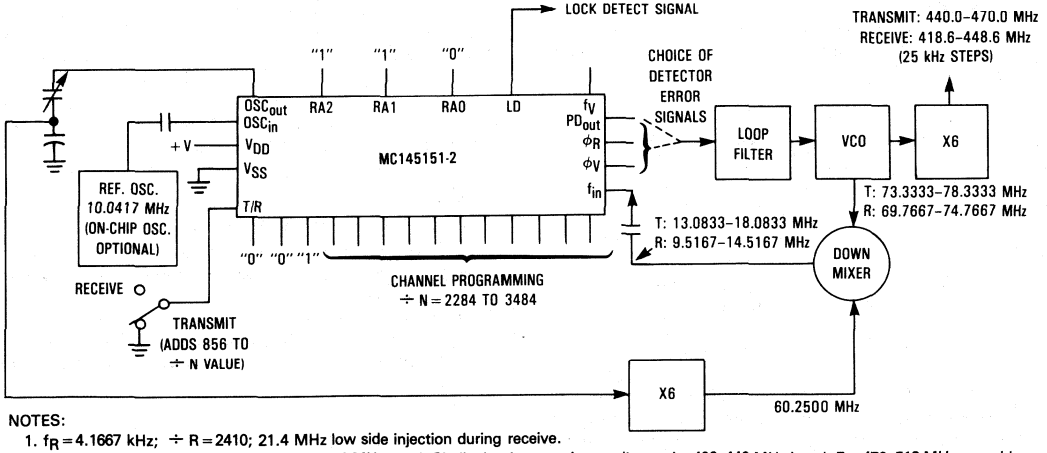
V_{SS}

The most negative supply potential. This pin is usually ground.

TYPICAL APPLICATIONS



5 MHz to 5.5 MHz Local Oscillator Channel Spacing = 1 kHz



NOTES:
1. f_R = 4.1667 kHz; ÷ R = 2410; 21.4 MHz low side injection during receive.
2. Frequency values shown are for the 440-470 MHz band. Similar implementation applies to the 406-440 MHz band. For 470-512 MHz, consider reference oscillator frequency X9 for mixer injection signal (90.3750 MHz).

Synthesizer for Land Mobile Radio UHF Bands

MC145152-2

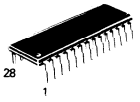
Parallel-Input PLL Frequency Synthesizer

Interfaces with Dual-Modulus Prescalers

The MC145152-2 is programmed by sixteen parallel inputs for the N and A counters and three input lines for the R counter. The device features consist of a reference oscillator, selectable-reference divider, two-output phase detector, 10-bit programmable divide-by-N counter, and 6-bit programmable ÷ A counter.

The MC145152-2 is an improved-performance drop-in replacement for the MC145152-1. Power consumption has decreased and ESD and latch-up performance have improved.

- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On- or Off-Chip Reference Oscillator Operation
- Lock Detect Signal
- Dual Modulus/Parallel Programming
- 8 User-Selectable ÷ R Values: 8, 64, 128, 256, 512, 1024, 1160, 2048
- ÷ N Range = 3 to 1023, ÷ A Range = 0 to 63
- Chip Complexity: 8000 FETs or 2000 Equivalent Gates



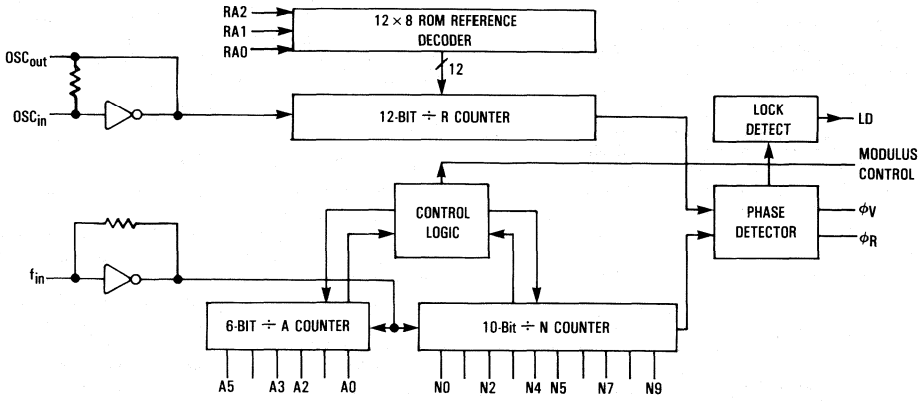
P SUFFIX
PLASTIC
CASE 710

FN SUFFIX
PLCC
CASE 776

ORDERING INFORMATION

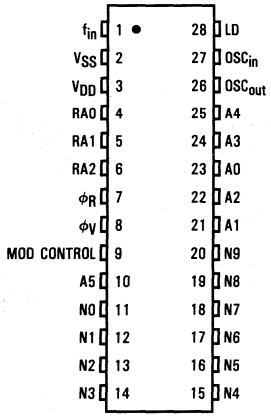
MC145152P2	Plastic DIP
MC145152FN2	PLCC Package

BLOCK DIAGRAM

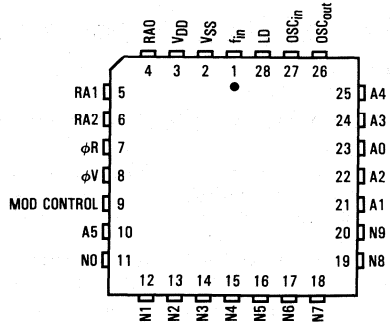


NOTE: N0 through N9, A0 through A5, and RA0 through RA2 have pullup resistors not shown.

PIN ASSIGNMENTS



PLASTIC DIP



PLCC PACKAGE

PIN DESCRIPTIONS

INPUTS

f_{in}—Frequency Input

Input to the positive edge triggered ÷ N and ÷ A counters. f_{in} is typically derived from a dual-modulus prescaler and is ac coupled into the device. For larger amplitude signals (standard CMOS logic levels) dc coupling may be used.

RA0, RA1, RA2—Reference Address Inputs

These three inputs establish a code defining one of eight possible divide values for the total reference divider. The total reference divide values are as follows:

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	8
0	0	1	64
0	1	0	128
0	1	1	256
1	0	0	512
1	0	1	1024
1	1	0	1160
1	1	1	2048

N Inputs—N Counter Programming Inputs

The N inputs provide the data that is preset into the ÷ N counter when it reaches the count of zero. N0 is least significant digit and N9 is most significant. Pullup resistors ensure that inputs left open remain at a logic one and require only a SPST switch to alter data to the zero state.

A Inputs—A Counter Programming Inputs

The A inputs define the number of clock cycles of f_{in} that require a logic zero on the modulus control output. (See Dual-Modulus Prescaling section.) The A inputs all have internal pullup resistors that ensure that inputs left open will remain at a logic one.

OSC_{in}, OSC_{out}—Reference Oscillator Input/Output

These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as input for an externally-generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

OUTPUTS

ϕ_R, ϕ_V—Phase Detector Outputs

These phase detector outputs can be combined externally for a loop error signal.

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

Modulus Control—Dual-Modulus Prescale Control Output

Signal generated by the on-chip control logic circuitry for controlling an external dual-modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the ÷ A counter has counted down from its programmed value. At this time, modulus control goes high

and remains high until the ÷ N counter has counted the rest of the way down from its programmed value (N – A additional counts since both ÷ N and ÷ A are counting down during the first portion of the cycle). Modulus control is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (N_T) = N•P + A where P and P + 1 represent the dual-modulus prescaler divide values respectively for high and low modulus control levels, N the number programmed into the ÷ N counter, and A the number programmed into the ÷ A counter.

LD—Lock Detector Output

Lock detector signal. Essentially a high level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

POWER SUPPLY

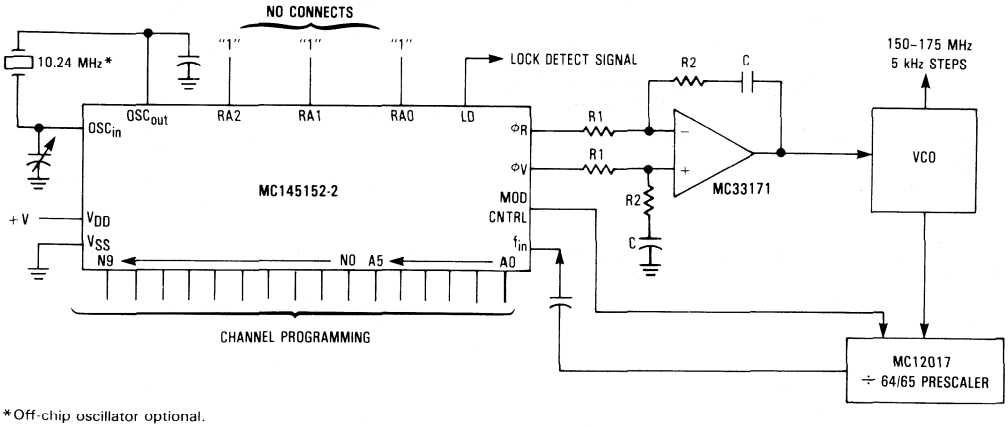
V_{DD}

The positive power supply potential. This pin may range from +3 to +9 V with respect to V_{SS}.

V_{SS}

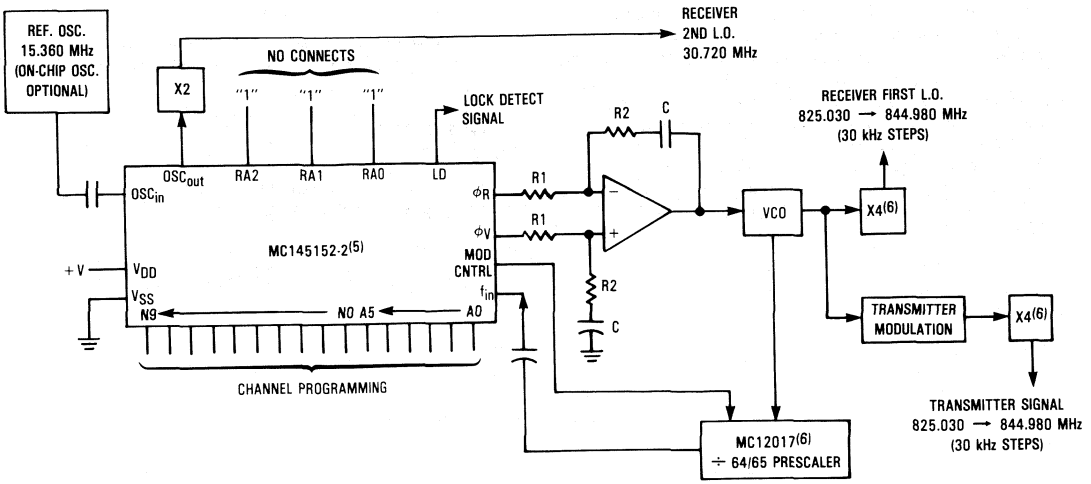
The most negative supply potential. This pin is usually ground.

TYPICAL APPLICATIONS



*Off-chip oscillator optional.

Synthesizer for Land Mobile Radio VHF Bands



NOTES:
1. Receiver 1st. I.F. = 45 MHz, low side injection; Receiver 2nd. I.F. = 11.7 MHz, low side injection.
2. Duplex operation with 45 MHz receiver/transmit separation.
3. $f_R = 7.5$ kHz, $\div R = 2048$.
4. $N_{total} = N \cdot 64 + A = 27501$ to 28166; N = 429 to 440; A = 0 to 63.
5. MC145158-2 may be used where serial data entry is desired.
6. High frequency prescalers—e.g., MC12018 (520 MHz) and MC12022 (1 GHz)—may be used for higher frequency VCO and f_{ref} implementations.

666-Channel, Computer-Controlled, Mobile Radiotelephone Synthesizer for 800 MHz Cellular Radio Systems

MC145155-2

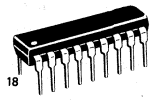
Serial-Input PLL Frequency Synthesizer

Interfaces with Single-Modulus Prescalers

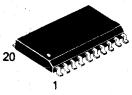
The MC145155-2 is programmed by a clocked, serial input, 16-bit data stream. The device features consist of a reference oscillator, selectable-reference divider, digital-phase detector, 14-bit programmable divide-by-N counter, and the necessary shift register and latch circuitry for accepting serial input data.

The MC145155-2 is an improved-performance drop-in replacement for the MC145155-1. Power consumption has decreased and ESD and latch-up performance have improved.

- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On- or Off-Chip Reference Oscillator Operation with Buffered Output
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- Lock Detect Signal
- Two Open-Drain Switch Outputs
- 8 User-Selectable ÷ R Values: 16, 512, 1024, 2048, 3668, 4096, 6144, 8192
- Single Modulus/Serial Programming
- ÷ N Range = 3 to 16383
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options: Single Ended (Three-State) or Double Ended
- Chip Complexity: 6504 FETs or 1626 Equivalent Gates



P SUFFIX
PLASTIC
CASE 707



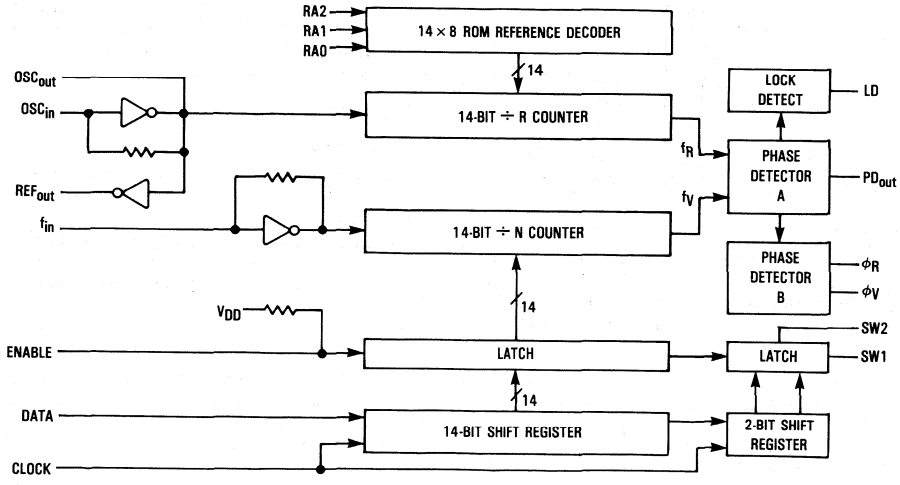
DW SUFFIX
SOG
CASE 751D

FN SUFFIX
PLCC
CASE 775

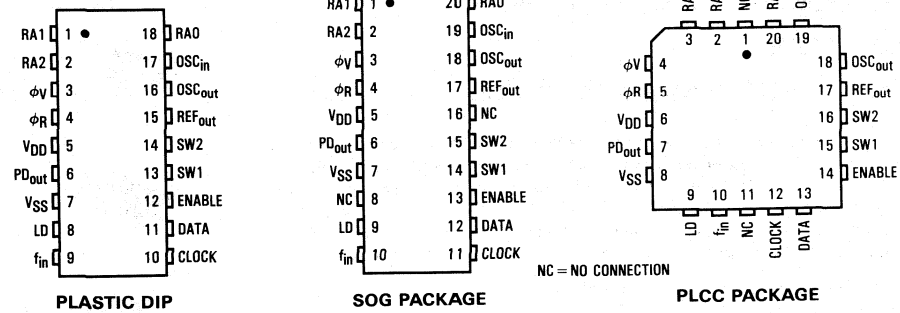
ORDERING INFORMATION

MC145155P2	Plastic DIP
MC145155DW2	SOG Package
MC145155FN2	PLCC Package

BLOCK DIAGRAM



PIN ASSIGNMENTS



PLASTIC DIP | SOG PACKAGE | PLCC PACKAGE

PIN DESCRIPTIONS

INPUTS

f_{in}—Frequency Input

Input to the ÷ N portion of synthesizer. f_{in} is typically derived from loop VCO and is ac coupled into the device. For larger amplitude signals (standard CMOS logic levels) dc coupling may be used.

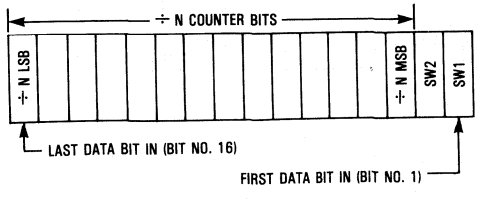
RA0, RA1, RA2—Reference Address Inputs

These three inputs establish a code defining one of eight possible divide values for the total reference divider, as defined by the table below:

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	16
0	0	1	512
0	1	0	1024
0	1	1	2048
1	0	0	3668
1	0	1	4096
1	1	0	6144
1	1	1	8192

CLOCK, DATA—Shift Clock, Serial Data Inputs

Shift register clock and data input. Each low-to-high transition clocks one bit into the on-chip 16-bit shift register. The Data input provides programming information for the 14-bit ÷ N counter and the two switch signals SW1 and SW2. The entry format is as follows:



ENABLE—Latch Enable Input

When high ("1") transfers contents of the shift register into the latches, and to the programmable counter inputs, and the switch outputs SW1 and SW2. When low ("0") inhibits the above action and thus allows changes to be made in the shift register data without affecting the counter programming and switch outputs. An on-chip pullup establishes a continuously high level for Enable when no external signal is applied. Enable is normally low and is pulsed high to transfer data to the latches.

OSC_{in}, OSC_{out}—Reference Oscillator Input/Output

These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as input for an externally-generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

OUTPUTS

PD_{out}—Phase Detector A Output

Three state output of phase detector for use as loop error signal. Double-ended outputs are also available for this purpose (see ϕV and ϕR).

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses.

Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses.

Frequency $f_V = f_R$ and Phase Coincidence: High-Impedance State.

ϕV, ϕR—Phase Detector B Outputs

These phase detector outputs can be combined externally for a loop error signal. A single-ended output is also available for this purpose (see PD_{out}).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕV pulsing low. ϕR remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕR pulsing low. ϕV remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕV and ϕR remain high except for a small minimum time period when both pulse low in phase.

LD—Lock Detector Output

Lock detector signal. Essentially a high level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

SW1, SW2—Band Switch Outputs

SW1 and SW2 provide latched open-drain outputs corresponding to data bits numbers one and two. These outputs can be tied through external resistors to voltages as high as 15 V dc, independent of the V_{DD} supply voltage. These are typically used for band switch functions. A logic one causes the output to assume a high-impendance state, while a logic zero causes the output to be low.

REF_{out}—Buffered Oscillator Output

Buffered output of on-chip reference oscillator or externally provided reference-input signal.

POWER SUPPLY

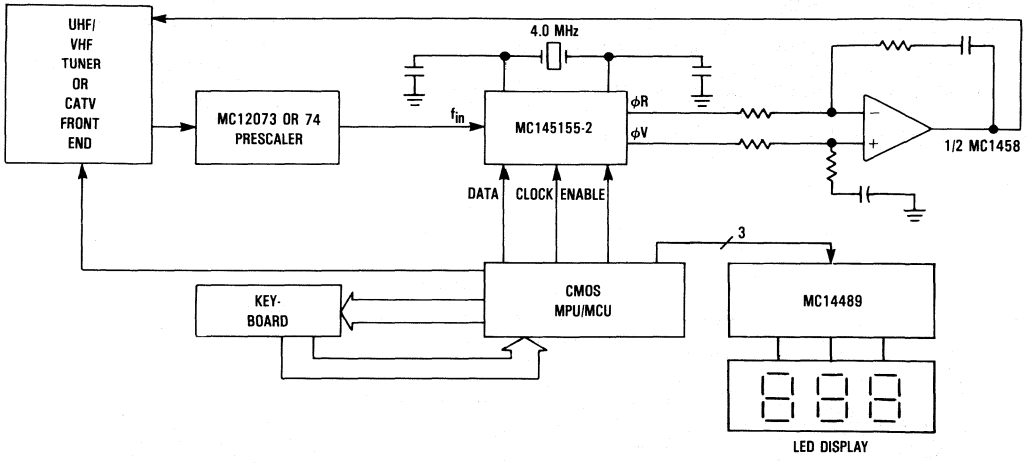
V_{DD}

The positive power supply potential. This pin may range from +3 to +9 V with respect to V_{SS}.

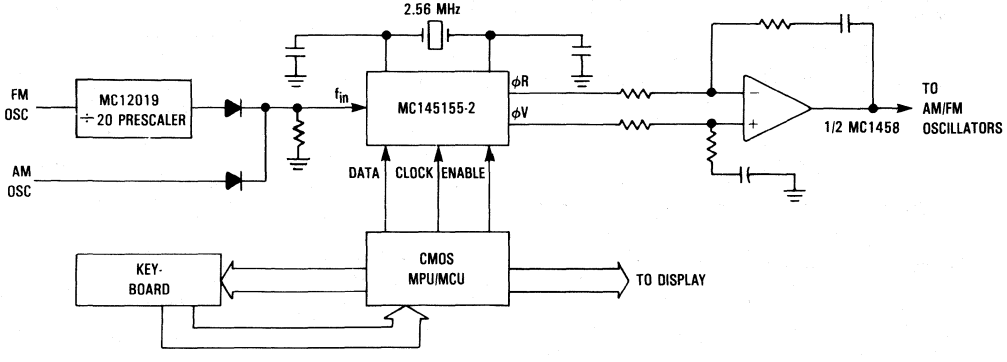
V_{SS}

The most negative supply potential. This pin is usually ground.

TYPICAL APPLICATIONS



Microprocessor-Controlled TV/CATV Tuning System with Serial Interface



AM/FM Radio Synthesizer

MC145156-2

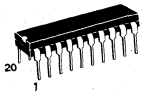
Serial-Input PLL Frequency Synthesizer

Interfaces with Dual-Modulus Prescalers

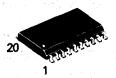
The MC145156-2 is programmed by a clocked, serial input, 19-bit data stream. The device features consist of a reference oscillator, selectable-reference divider, digital-phase detector, 10-bit programmable divide-by-N counter, 7-bit programmable divide-by-A counter, and the necessary shift register and latch circuitry for accepting serial input data.

The MC145156-2 is an improved-performance drop-in replacement for the MC145156-1. Power consumption has decreased and ESD and latch-up performance have improved.

- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On- or Off-Chip Reference Oscillator Operation with Buffered Output
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- Lock Detect Signal
- Two Open-Drain Switch Outputs
- Dual Modulus/Serial Programming
- 8 User-Selectable ÷ R Values: 8, 64, 128, 256, 640, 1000, 1024, 2048
- ÷ N Range = 3 to 1023, ÷ A Range = 0 to 127
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options: Single Ended (Three-State) or Double Ended
- Chip Complexity: 6504 FETs or 1626 Equivalent Gates



P SUFFIX
PLASTIC
CASE 738



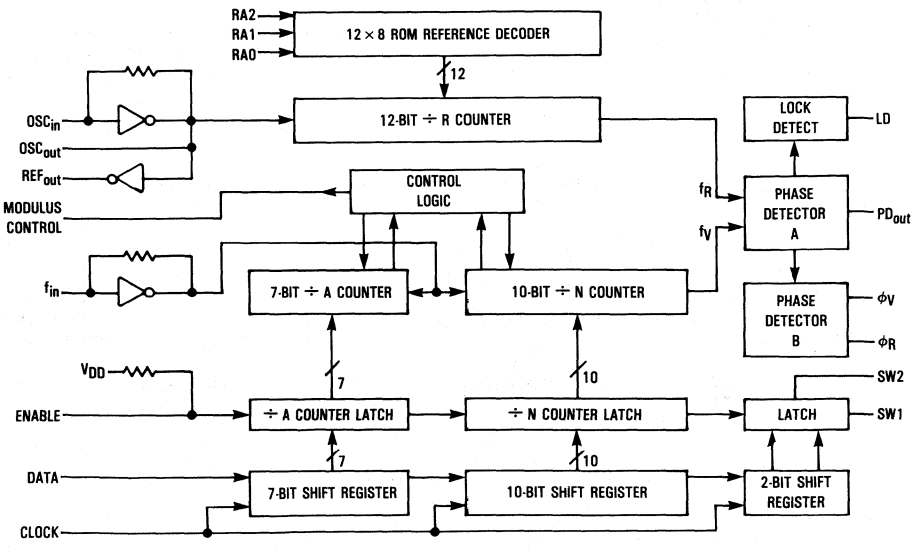
DW SUFFIX
SOG
CASE 751D

FN SUFFIX
PLCC
CASE 775

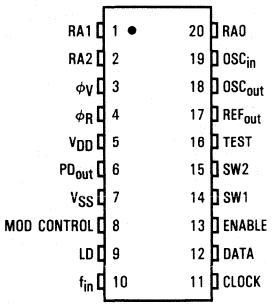
ORDERING INFORMATION

MC145156P2	Plastic DIP
MC145156DW2	SOG Package
MC145156FN2	PLCC Package

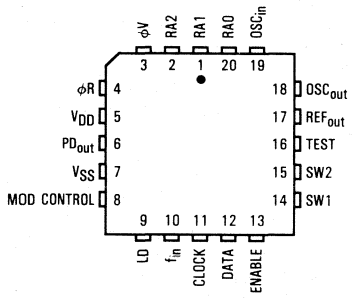
BLOCK DIAGRAM



PIN ASSIGNMENTS



PLASTIC DIP
SOG PACKAGE



PLCC PACKAGE

PIN DESCRIPTIONS

INPUTS

f_{in}—Frequency Input

Input to the positive edge triggered ÷ N and ÷ A counters. f_{in} is typically derived from a dual-modulus prescaler and is ac coupled into the device. For larger amplitude signals (standard CMOS logic levels) dc coupling may be used.

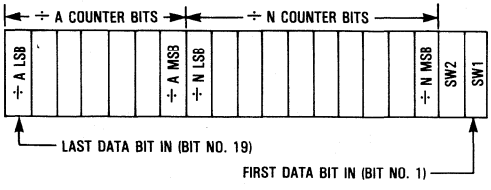
RA0, RA1, RA2—Reference Address Inputs

These three inputs establish a code defining one of eight possible divide values for the total reference divider, as defined by the table below:

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	8
0	0	1	64
0	1	0	128
0	1	1	256
1	0	0	640
1	0	1	1000
1	1	0	1024
1	1	1	2048

CLOCK, DATA—Shift Clock, Serial Data Inputs

Shift register clock and data input. Each low-to-high transition clocks one bit into the on-chip 19-bit shift register. The Data input provides programming information for the 10-bit ÷ N counter, the 7-bit ÷ A counter, and the two switch signals SW1 and SW2. The entry format is as follows:



ENABLE—Latch Enable Input

When high ("1") transfers contents of the shift register into the latches, and to the programmable counter inputs, and the switch outputs SW1 and SW2. When low ("0") inhibits the above action and thus allows changes to be made in the shift register data without affecting the counter programming and switch outputs. An on-chip pullup establishes a continuously high level for Enable when no external signal is applied. Enable is normally low and is pulsed high to transfer data to the latches.

OSC_{in}, OSC_{out}—Reference Oscillator Input/Output

These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as input for an externally-generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

TEST—Factory Test Input

Used in manufacturing. Must be left open or tied to V_{SS}.

OUTPUTS

PD_{out}—Phase Detector A Output

Three state output of phase detector for use as loop error signal. Double-ended outputs are also available for this purpose (see ϕV and ϕR).

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High-Impedance State

ϕV, ϕR—Phase Detector B Outputs

These phase detector outputs can be combined externally for a loop-error signal. A single-ended output is also available for this purpose (see PD_{out}).

If frequency f_V is greater than f_R or if the phase of f_V is

leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

Modulus Control—Dual-Modulus Prescale Control Output

Signal generated by the on-chip control logic circuitry for controlling an external dual-modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the ÷ A counter has counted down from its programmed value. At this time, modulus control goes high and remains high until the ÷ N counter has counted the rest of the way down from its programmed value (N – A additional counts since both ÷ N and ÷ A are counting down during the first portion of the cycle). Modulus control is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (N_T) = N•P + A where P and P + 1 represent the dual-modulus prescaler divide values respectively for high and low modulus control levels, N the number programmed into the ÷ N counter, and A the number programmed into the ÷ A counter.

LD—Lock Detector Output

Lock detector signal. Essentially a high level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

SW1, SW2—Band Switch Outputs

SW1 and SW2 provide latched open-drain outputs corresponding to data bits numbers one and two. These outputs can be tied through external resistors to voltages as high as 15 V dc, independent of the V_{DD} supply voltage. These are typically used for band switch functions. A logic one causes the output to assume a high-impedance state, while a logic zero causes the output to be low.

REF_{out}—Buffered Oscillator Output

Buffered output of on-chip reference oscillator or externally provided reference-input signal.

POWER SUPPLY

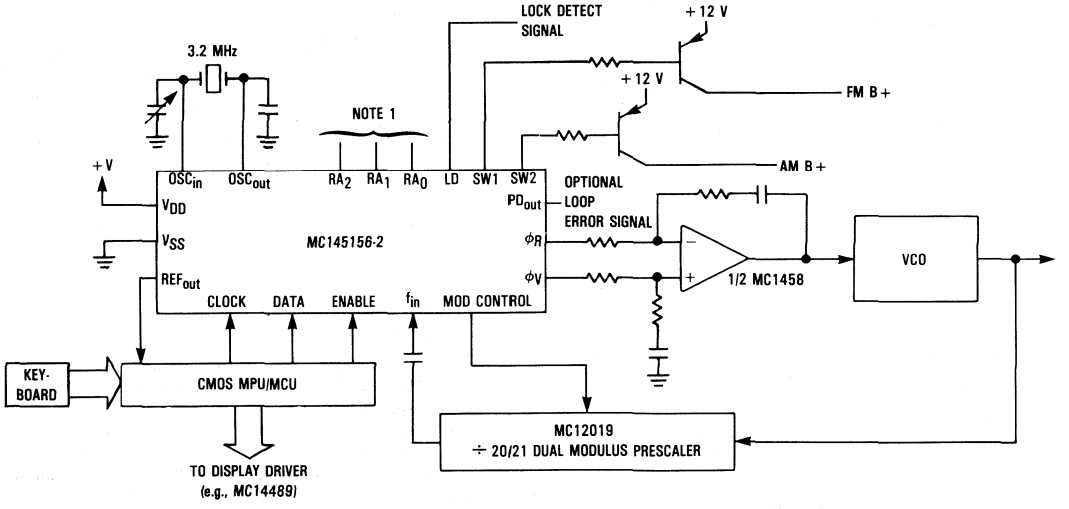
V_{DD}

The positive power supply potential. This pin may range from +3 to +9 V with respect to V_{SS}.

V_{SS}

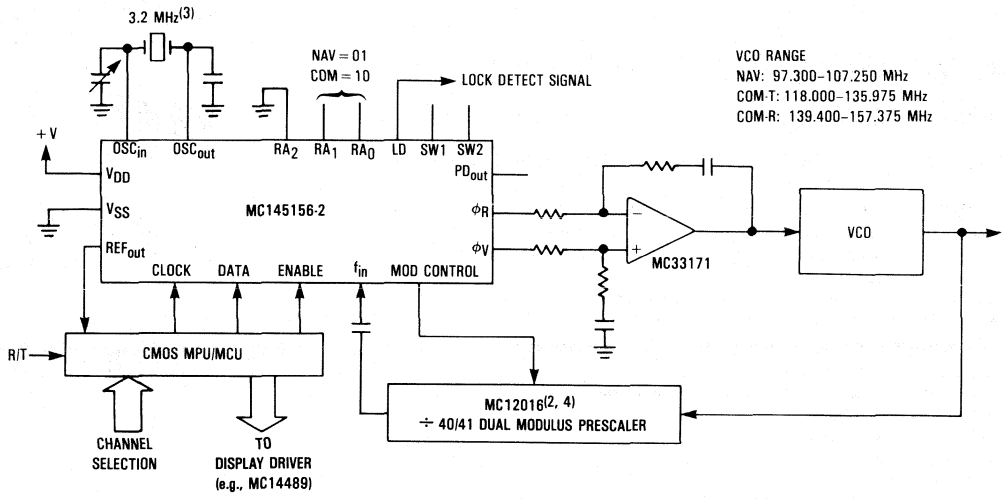
The most negative supply potential. This pin is usually ground.

TYPICAL APPLICATIONS



NOTE 1
for AM: channel spacing = 5 kHz, ÷ R = ÷ 640 (code 100)
for FM: channel spacing = 25 kHz, ÷ R = ÷ 128 (code 010)

AM/FM Radio Broadcast Synthesizer



NOTES:
1. For NAV: $f_R = 50$ kHz, ÷ R = 64 using 10.7 MHz lowside injection, $N_{total} = 1946\text{-}2145$.
   For COM-T: $f_R = 25$ kHz, ÷ R = 128, $N_{total} = 4720\text{-}5439$.
   For COM-R: $f_R = 25$ kHz, ÷ R = 128 using 21.4 MHz highside injection, $N_{total} = 5576\text{-}6295$.
2. A ÷ 32/33 dual modulus approach is provided by substituting an MC12015 for the MC12016. The devices are pin equivalent.
3. A 6.4 MHz oscillator crystal can be used by selecting ÷ R = 128 (code 010) for NAV and ÷ R = 256 (code 011) for COM.
4. MC12013 + MC10131 combination may also be used to form the ÷ 40/41 prescaler.

Avionics Navigation or Communication Synthesizer

MC145157-2

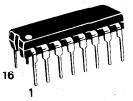
Serial-Input PLL Frequency Synthesizer

Interfaces with Single-Modulus Prescalers

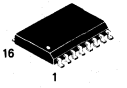
The MC145157-2 has a fully programmable 14-bit reference counter, as well as a fully programmable ÷ N counter. The counters are programmed serially through a common data input and latched into the appropriate counter latch, according to the last data bit (control bit) entered.

The MC145157-2 is an improved-performance drop-in replacement for the MC145157-1. Power consumption has decreased and ESD and latch-up performance have improved.

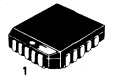
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- Fully Programmable Reference and ÷ N Counters
- ÷ R Range = 3 to 16383
- ÷ N Range = 3 to 16383
- f_V and f_R Outputs
- Lock Detect Signal
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- "Linearized" Digital Phase Detector
- Single-Ended (Three-State) or Double-Ended Phase Detector Outputs
- Chip Complexity: 6504 FETs or 1626 Equivalent Gates



P SUFFIX
PLASTIC
CASE 648



DW SUFFIX
SOG
CASE 751G

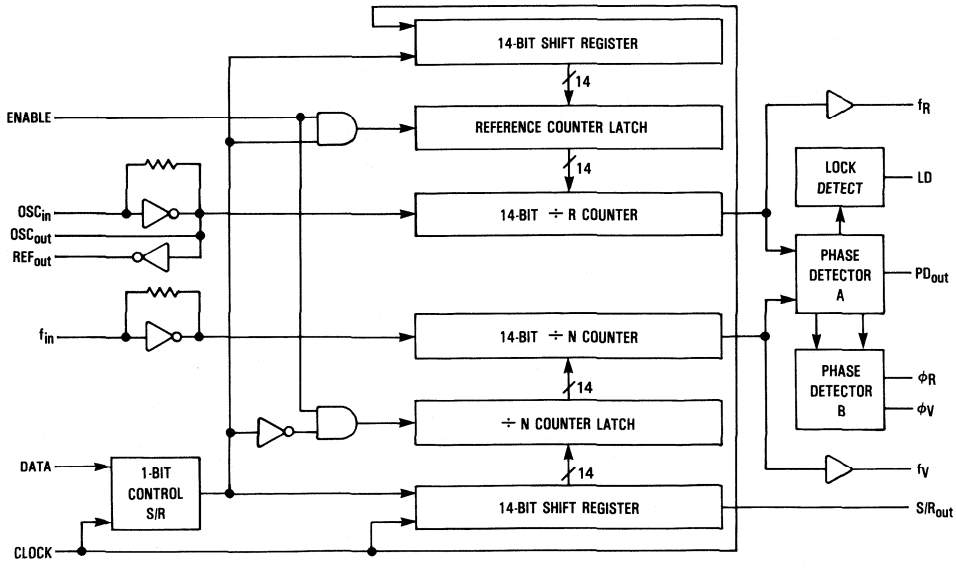


FN SUFFIX
PLCC
CASE 775

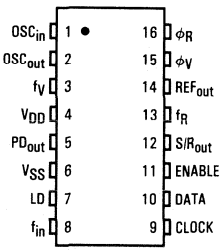
ORDERING INFORMATION

MC145157P2	Plastic DIP
MC145157DW2	SOG Package
MC145157FN2	PLCC Package

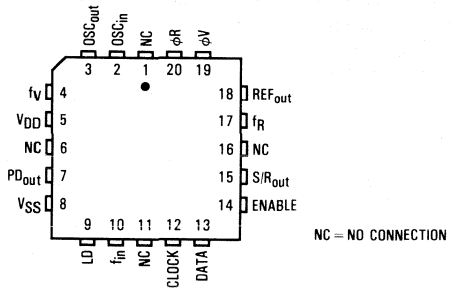
BLOCK DIAGRAM



PIN ASSIGNMENTS



PLASTIC DIP
SOG PACKAGE



PLCC PACKAGE

PIN DESCRIPTIONS

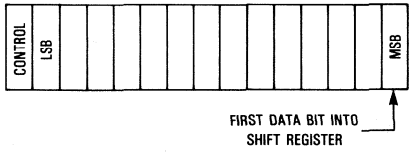
INPUTS

f_{in}—Frequency Input

Input frequency from VCO output. A rising edge signal on this input decrements the ÷ N counter. This input has an inverter biased in the linear region to allow use with ac coupled signals as low as 500 mV p-p. For larger amplitude signals (standard CMOS logic levels) dc coupling may be used.

CLOCK, DATA—Shift Clock, Serial Data Inputs

Each low-to-high transition of the clock shifts one bit of data into the on-chip shift registers. The last data bit entered determines which counter storage latch is activated; a logic one selects the reference counter latch and a logic zero selects the ÷ N counter latch. The data entry format is as follows:



ENABLE—Latch Enable Input

A logic high on this pin latches the data from the shift register into the reference divider or ÷ N latches depending on the control bit. The reference divider latches are activated if the control bit is at a logic high and the ÷ N latches are activated if the control bit is at a logic low. A logic low on this pin allows the user to change the data in the shift registers without affecting the counters. Enable is normally low and is pulsed high to transfer data to the latches.

OSC_{in}, OSC_{out}—Reference Oscillator Input/Output

These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as input for an externally-generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

OUTPUTS

PD_{out}—Phase Detector A Output

This single ended (three-state) phase detector output produces a loop error signal that is used with a loop filter to control a VCO.

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High-Impedance State

ϕV, ϕR—Phase Detector B Outputs

Double-ended phase detector outputs. These outputs can be combined externally for a loop-error signal. A single-ended output is also available for this purpose (see PD_{out}).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕV pulsing low. ϕR remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕR pulsing low. ϕV remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕV and ϕR remain high except for a small minimum time period when both pulse low in phase.

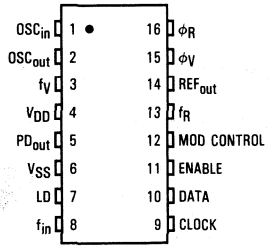
f_R, f_V—R Counter Output, N Counter Output

Buffered, divided reference and f_{in} frequency outputs. The f_R and f_V outputs are connected internally to the ÷ R and ÷ N counter outputs respectively, allowing the counters to be used independently, as well as monitoring the phase detector inputs.

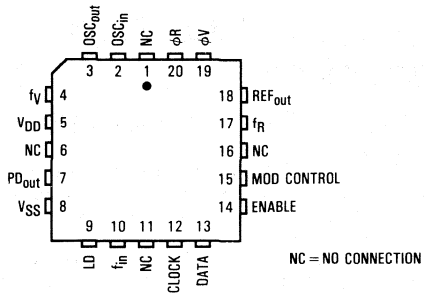
LD—Lock Detector Output

This output is essentially at a high level when the loop is locked (f_R, f_V of same phase and frequency), and pulses low when loop is out of lock.

PIN ASSIGNMENTS



PLASTIC DIP
SOG PACKAGE



PLCC PACKAGE

PIN DESCRIPTIONS

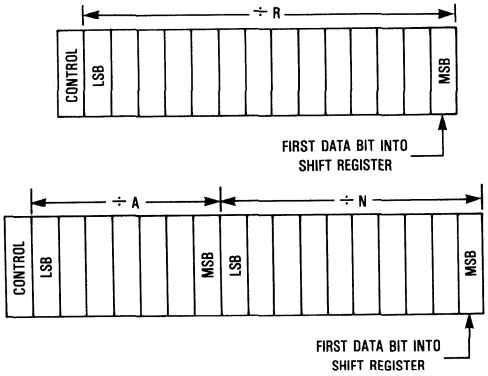
INPUTS

f_{in}—Frequency Input

Input frequency from VCO output. A rising edge signal on this input decrements the ÷ A and ÷ N counters. This input has an inverter biased in the linear region to allow use with ac coupled signals as low as 500 mV p-p. For larger amplitude signals (standard CMOS logic levels) dc coupling may be used.

CLOCK, DATA—Shift Clock, Serial Data Inputs

Each low-to-high transition of the clock shifts one bit of data into the on-chip shift registers. The last data bit entered determines which counter storage latch is activated; a logic one selects the reference counter latch and a logic zero selects the ÷ A, ÷ N counter latch. The data entry format is as follows:



ENABLE—Latch Enable Input

A logic high on this pin latches the data from the shift register into the reference divider or ÷ N, ÷ A latches depending on the control bit. The reference divider latches are activated if the control bit is at a logic high and the ÷ N, ÷ A latches are activated if the control bit is at a logic low. A logic low on this pin allows the user to change the data in the shift registers without affecting the counters. Enable is normally low and is pulsed high to transfer data to the latches.

OSC_{in}, OSC_{out}—Reference Oscillator Input/Output

These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally-generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

OUTPUTS

PD_{out}—Phase Detector A Output

This single ended (three-state) phase detector output produces a loop error signal that is used with a loop filter to control a VCO.

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High-Impedance State

ϕV, ϕR—Phase Detector B Outputs

Double-ended phase detector outputs. These outputs can be combined externally for a loop error signal. A single-ended output is also available for this purpose (see PD_{out}).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕV pulsing low. ϕR remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕR pulsing low. ϕV remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕV and ϕR remain high except for a small minimum time period when both pulse low in phase.

Modulus Control—Dual-Modulus Prescale Control Output

This output generates a signal by the on-chip control logic circuitry for controlling an external dual-modulus prescaler. The modulus control level is low at the beginning of a count cycle and remains low until the ÷ A counter has counted down from its programmed value. At this time, modulus control goes high and remains high until the ÷ N counter has counted the rest of the way down from its programmed value (N – A additional counts since both ÷ N and ÷ A are counting down during the first portion of the cycle). Modulus Control is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (N_T) = N•P + A where P and P + 1 represent the dual-modulus prescaler divide values respectively for high and low modulus control levels, N the number programmed into the ÷ N counter, and A the number programmed into the ÷ A counter. Note that when a prescaler is needed, the dual-modulus version offers a distinct advantage. The dual-modulus prescaler allows a higher reference frequency at the phase detector input, increasing system performance capability, and simplifying the loop filter design.

f_R, f_V—R Counter Output, N Counter Output

Buffered, divided reference and f_{in} frequency outputs. The f_R and f_V outputs are connected internally to the ÷ R and ÷ N counter outputs respectively, allowing the counters to be used independently, as well as monitoring the phase detector inputs.

LD—Lock Detector Output

This output is essentially at a high level when the loop is locked (f_R, f_V of same phase and frequency), and pulses low when loop is out of lock.

REF_{out}—Buffered Oscillator Output

This output can be used as a second local oscillator, reference oscillator to another frequency synthesizer, or as the system clock to a microprocessor controller.

POWER SUPPLY

V_{DD}

The positive power supply potential. This pin may range from +3 to +9 V with respect to V_{SS}.

V_{SS}

The most negative supply potential. This pin is usually ground.

FAMILY CHARACTERISTICS

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 10 ns)

Symbol	Parameter	V_{DD} V	Guaranteed Limit 25°C	Guaranteed Limit −40°C to 85°C	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, f_{in} to Modulus Control (Figures 1 and 4)	3 5 9	110 60 35	120 70 40	ns
t_{PHL}	Maximum Propagation Delay, Enable to SW1, SW2 (Figures 1 and 5)	3 5 9	160 80 50	180 95 60	ns
t_W	Output Pulse Width, ϕ_R, ϕ_V, and LD with f_R in Phase with f_V (Figures 2 and 4)	3 5 9	25 to 200 20 to 100 10 to 70	25 to 260 20 to 125 10 to 80	ns
t_{TLH}	Maximum Output Transition Time, Modulus Control (Figures 3 and 4)	3 5 9	115 60 40	115 75 60	ns
t_{THL}	Maximum Output Transition Time, Modulus Control (Figures 3 and 4)	3 5 9	60 34 30	70 45 38	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Lock Detect (Figures 3 and 4)	3 5 9	180 90 70	200 120 90	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Other Outputs (Figures 3 and 4)	3 5 9	160 80 60	175 100 65	ns

SWITCHING WAVEFORMS

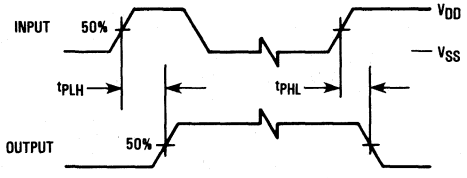
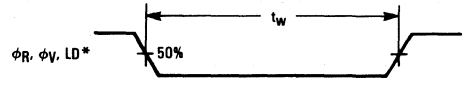


Figure 1



*f_R in phase with f_V.

Figure 2

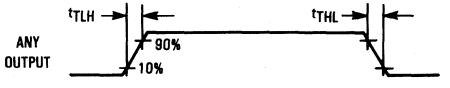
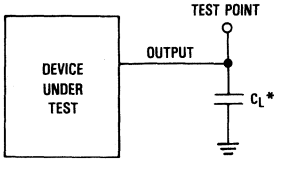
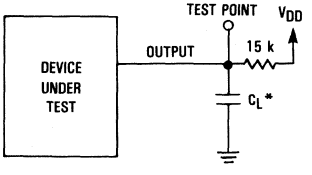


Figure 3



*Includes all probe and jig capacitance.

Figure 4. Test Circuit



*Includes all probe and jig capacitance.

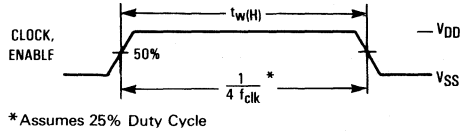
Figure 5. Test Circuit

FAMILY CHARACTERISTICS

TIMING REQUIREMENTS (Input $t_r = t_f = 10$ ns unless otherwise indicated)

Symbol	Parameter	V_{DD} V	Guaranteed Limit 25°C	Guaranteed Limit −40°C to 85°C	Unit
f_{clk}	Serial Data Clock Frequency, Assuming 25% Duty Cycle NOTE: Refer to Clock $t_{w(H)}$ below (Figure 6)	3 5 9	dc to 5.0 dc to 7.1 dc to 10	dc to 3.5 dc to 7.1 dc to 10	MHz
t_{su}	Minimum Setup Time, Data to Clock (Figure 7)	3 5 9	30 20 18	30 20 18	ns
t_h	Minimum Hold Time, Clock to Data (Figure 7)	3 5 9	40 20 15	40 20 15	ns
t_{su}	Minimum Setup Time, Clock to Enable (Figure 7)	3 5 9	70 32 25	70 32 25	ns
t_{rec}	Minimum Recovery Time, Enable to Clock (Figure 7)	3 5 9	5 10 20	5 10 20	ns
$t_{w(H)}$	Minimum Pulse Width, Clock, Enable (Figure 6)	3 5 9	50 35 25	70 35 25	ns
t_r, t_f	Maximum Input Rise and Fall Times—Any Input (Figure 8)	3 5 9	5 4 2	5 4 2	μs

SWITCHING WAVEFORMS



*Assumes 25% Duty Cycle

Figure 6

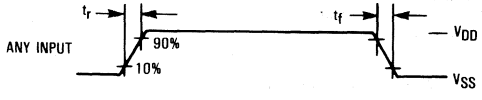


Figure 8

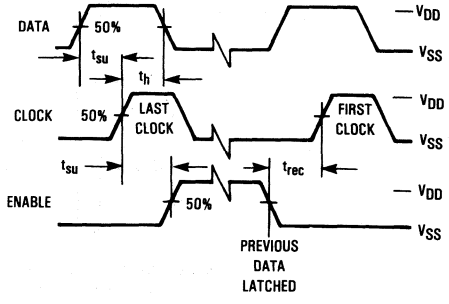


Figure 7

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers. The most desirable is discussed first.

USE OF A HYBRID CRYSTAL OSCILLATOR

Commercially available temperature-compensated crystal oscillators (TCXOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or dc coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct-coupled square wave having a rail-to-rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog*, the *Gold Book*, or similar publications.

DESIGN AN OFF-CHIP REFERENCE

The user may design an off-chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), dc coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct-coupled square wave having rail-to-rail voltage swing.

USE OF THE ON-CHIP OSCILLATOR CIRCUITRY

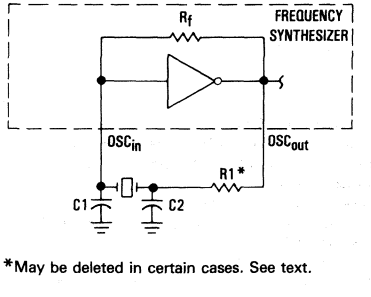
The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 10.

For V_{DD} = 5 V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8 MHz, 20 pF for frequencies in the area of 8 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. The shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in}+C_{out}} + C_a + C_O + \frac{C1 \cdot C2}{C1+C2}$$

where

C_{in} = 5 pF (see Figure 11)
C_{out} = 6 pF (see Figure 11)
C_a = 1 pF (see Figure 11)
C_O = the crystal's holder capacitance (see Figure 12)
C1 and C2 = external capacitors (see Figure 10)



*May be deleted in certain cases. See text.

Figure 10. Pierce Crystal Oscillator Circuit

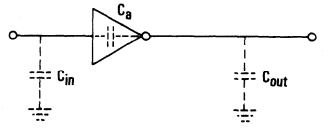
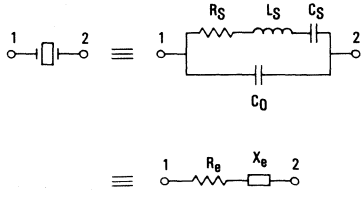


Figure 11. Parasitic Capacitances of the Amplifier



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 12. Equivalent Crystal Networks

The oscillator can be "trimmed" on-frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. In some cases, stray capacitance should be added to the values for C_{in} and C_{out}.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 12. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 in Figure 10 limits the drive level. The use of R1 may not be necessary in some cases; i.e., R1 = 0 ohms.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize

DESIGN CONSIDERATIONS

loading.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdiven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. See Table 1.

RECOMMENDED FOR READING

Technical Note TN-24, Statek Corp.

Technical Note TN-7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit—Definitions and Method of Measurement", *Proc. IEEE*, Vol. 57, No. 2; Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro-Technology*, June, 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May, 1966.

Table 1. Partial List of Crystal Manufacturers

Name	Address	Phone
United States Crystal Corp.	3605 McCart St., Ft. Worth, TX 76110	(817) 921-3013
Crystek Crystal	2371 Crystal Dr., Ft. Myers, FL 33907	(813) 936-2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639-7810

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

DESIGN CONSIDERATIONS

DUAL-MODULUS PRESCALING

OVERVIEW

The technique of dual-modulus prescaling is well established as a method of achieving high performance frequency synthesizer operation at high frequencies. Basically, the approach allows relatively low-frequency programmable counters to be used as high-frequency programmable counters with speed capability of several hundred MHz. This is possible without the sacrifice in system resolution and performance that results if a fixed (single-modulus) divider is used for the prescaler.

In dual-modulus prescaling, the lower speed counters must be uniquely configured. Special control logic is necessary to select the divide value P or P + 1 in the prescaler for the required amount of time (see modulus control definition). Motorola's dual-modulus frequency synthesizers contain this feature and can be used with a variety of dual-modulus prescalers to allow speed, complexity and cost to be tailored to the system requirements. Prescalers having P, P+1 divide values in the range of ÷ 3/ ÷ 4 to ÷ 128/ ÷ 129 can be controlled by most Motorola frequency synthesizers.

Several dual-modulus prescaler approaches suitable for use with the MC145152-2, MC145156-2, or MC145158-2 are:

MC12009	÷ 5/ ÷ 6	440 MHz
MC12011	÷ 8/ ÷ 9	500 MHz
MC12013	÷ 10/ ÷ 11	500 MHz
MC12015	÷ 32/ ÷ 33	225 MHz
MC12016	÷ 40/ ÷ 41	225 MHz
MC12017	÷ 64/ ÷ 65	225 MHz
MC12018	÷ 128/ ÷ 129	520 MHz
MC12022A	÷ 64/65 or ÷ 128/129	1.1 GHz
MC12032A	÷ 64/65 or ÷ 128/129	2.0 GHz

DESIGN GUIDELINES

The system total divide value, N_{total} (N_T) will be dictated by the application,i.e.

$$N_T = \frac{\text{frequency into the prescaler}}{\text{frequency into the phase detector}} = N \cdot P + A$$

N is the number programmed into the ÷ N counter, A is the number programmed into the ÷ A counter, P and P+1 are the two selectable divide ratios available in the dual-modulus prescalers. To have a range of N_T values in sequence, the ÷ A counter is programmed from zero through P − 1 for a particular value N in the ÷ N counter. N is then incremented to N+1 and the ÷ A is sequenced from zero through P − 1 again.

There are minimum and maximum values that can be achieved for N_T. These values are a function of P and the size of the ÷ N and ÷ A counters. The constraint $N \geq A$ always applies. If $A_{max} = P - 1$, then $N_{min} \geq P - 1$. Then $N_{Tmin} = (P-1)\,P + A$ or $(P-1)\,P$ since A is free to assume the value of zero.

$$N_{Tmax} = N_{max} \cdot P + A_{max}$$

To maximize system frequency capability, the dual-modulus prescaler output must go from low to high after each group of P or P+1 input cycles. The prescaler should divide by P when its modulus control line is high and by P+1 when its modulus control is low.

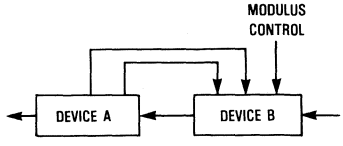
For the maximum frequency into the prescaler (f_{VCO}max), the value used for P must be large enough such that:

A. f_{VCO} max divided by P may not exceed the frequency capability of f_{in} (input to the ÷ N and ÷ A counters).
B. The period of f_{VCO} divided by P must be greater than the sum of the times:
   a. Propagation delay through the dual-modulus prescaler.
   b. Prescaler setup or release time relative to its modulus control signal.
   c. Propagation time from f_{in} to the modulus control output for the frequency synthesizer device.

A sometimes useful simplification in the programming code can be achieved by choosing the values for P of 8, 16, 32, or 64. For these cases, the desired value for N_T results when N_T in binary is used as the program code to the ÷ N and ÷ A counters treated in the following manner:

A. Assume the ÷ A counter contains "a" bits where $2^a \geq P$.
B. Always program all higher order ÷ A counter bits above "a" to zero.
C. Assume the ÷ N counter and the ÷ A counter (with all the higher order bits above "a" ignored) combined into a single binary counter of n+a bits in length (n = number of divider stages in the ÷ N counter). The MSB of this "hypothetical" counter is to correspond to the MSB of ÷ N and the LSB is to correspond to the LSB of ÷ A. The system divide value, N_T, now results when the value of N_T in binary is used to program the "new" n+a bit counter.

By using two devices, several dual-modulus values are achievable:



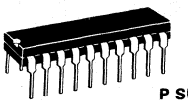
DEVICE A \ DEVICE B	MC12009	MC12011	MC12013
MC10131	÷ 20/ ÷ 21	÷ 32/ ÷ 33	÷ 40/ ÷ 41
MC10138	÷ 50/ ÷ 51	÷ 80/ ÷ 81	÷ 100/ ÷ 101
MC10154	÷ 40/ ÷ 41 OR ÷ 80/ ÷ 81	÷ 64/ ÷ 65 OR ÷ 128/ ÷ 129	÷ 80/ ÷ 81

NOTE: MC12009, MC12011, and MC12013 are pin equivalent.
MC12015, MC12016, and MC12017 are pin equivalent.

MC145159-1

Serial Input PLL Frequency Synthesizer with Analog Phase Detector

Interfaces with Dual-Modulus Prescalers



P SUFFIX
PLASTIC DIP
CASE 738

FN SUFFIX
PLCC
CASE 775

ORDERING INFORMATION

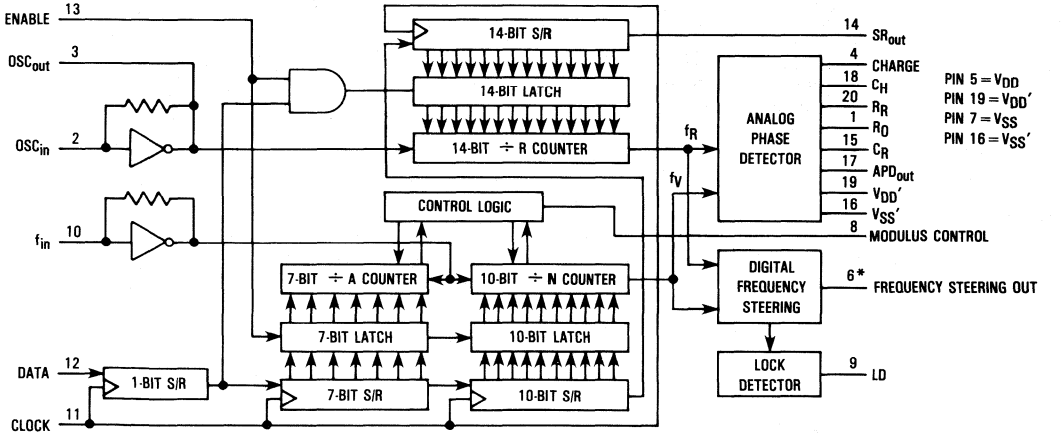
MC145159P1	Plastic DIP
MC145159FN1	PLCC

The MC145159-1 has a programmable 14-bit reference counter, as well as programmable divide-by-N/divide-by-A counters. The counters are programmed serially through a common data input and latched into the appropriate counter latch, according to the last data bit (control bit) entered.

When combined with a loop filter and VCO, this device can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operations, a down mixer or a dual modulus prescaler can be used between the VCO and the PLL.

- General Purpose Applications:
  - CATV — TV Tuning
  - AM/FM Radios — Scanning Receivers
  - Two Way Radios — Amateur Radio
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On- or Off-Chip Reference Oscillator Operation
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- ÷ R Range = 3 to 16383
- ÷ N Range = 16 to 1023, ÷ A Range = 0 to 127
- High-Gain Analog Phase Detector
- See Application Note AN969

BLOCK DIAGRAM



*NOTE: Pin 6 is not and cannot be used as a digital phase detector output.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +10.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD}+0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
I_{DD}, I_{SS}	Supply Current, V_{DD} or V_{SS} Pins	±30	mA
P_D	Power Dissipation, per Package	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

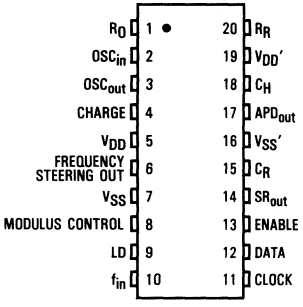
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

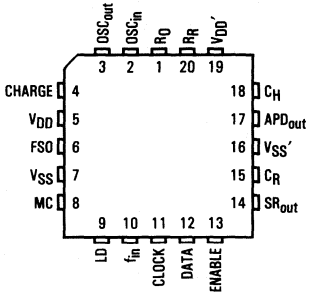
5

PIN ASSIGNMENTS

PLASTIC DIP



PLCC



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS} except I_{CR} and I_{APD} which are referenced to V_{SS}')

Characteristic	Symbol	V_{DD}	−40°C		25°C		85°C		Unit
			Min	Max	Min	Max	Min	Max	
Power Supply Voltage Range	V_{DD}	—	3	9	3	9	3	9	V
Output Voltage 0 Level V_{in} = 0 V or V_{DD} I_{out} = 0 μA (Except OSC_{out} and APD_{out})	V_{OL}	3	—	0.05	—	0.05	—	0.05	V
		5	—	0.05	—	0.05	—	0.05	
		9	—	0.05	—	0.05	—	0.05	
1 Level	V_{OH}	3	2.95	—	2.95	—	2.95	—	
		5	4.95	—	4.95	—	4.95	—	
		9	8.95	—	8.95	—	8.95	—	
Output Voltage 0 Level OSC_{out} V_{in} = 0 V or V_{DD}	V_{OL}	3	—	0.9	—	0.9	—	0.9	V
		5	—	1.5	—	1.5	—	1.5	
		9	—	2.7	—	2.7	—	2.7	
1 Level	V_{OH}	3	2.1	—	2.1	—	2.1	—	
		5	3.5	—	3.5	—	3.5	—	
		9	6.3	—	6.3	—	6.3	—	
ΔVoltage, $V_{CH} - V_{APDout}$ $I_{APDout} \approx 0$ μA	ΔV	—	—	—	—	1.05	—	—	V
Input Voltage 0 Level V_{out} = 0.5 V or V_{DD} − 0.5 V (All Outputs Except OSC_{out})	V_{IL}	3	—	0.9	—	0.9	—	0.9	V
		5	—	1.5	—	1.5	—	1.5	
		9	—	2.7	—	2.7	—	2.7	
1 Level	V_{IH}	3	2.1	—	2.1	—	2.1	—	
		5	3.5	—	3.5	—	3.5	—	
		9	6.3	—	6.3	—	6.3	—	
Input Voltage* — OSC_{in}	V_{IL}								V
V_O = 2.1 V or 0.9 V 0 Level		3	—	0	—	0	—	0	
V_O = 3.5 V or 1.5 V		5	—	0	—	0	—	0	
V_O = 6.3 V or 2.7 V		9	—	0	—	0	—	0	
V_O = 0.9 V or 2.1 V 1 Level	V_{IH}	3	3.0	—	3.0	—	3.0	—	
V_O = 1.5 V or 3.5 V		5	5.0	—	5.0	—	5.0	—	
V_O = 2.7 V or 6.3 V		9	9.0	—	9.0	—	9.0	—	
Output Current — Modulus Control	I_{OH}								mA
V_{out} = 2.7 V Source		3	−0.60	—	−0.50	—	−0.30	—	
V_{out} = 4.6 V		5	−0.90	—	−0.75	—	−0.50	—	
V_{out} = 8.5 V		9	−1.50	—	−1.25	—	−0.80	—	
V_{out} = 0.3 V Sink	I_{OL}	3	1.30	—	1.10	—	0.66	—	
V_{out} = 0.4 V		5	1.90	—	1.70	—	1.08	—	
V_{out} = 0.5 V		9	3.80	—	3.30	—	2.10	—	
Output Current, C_R V_{CR} = 4.5 V, R_R = 240 k	I_{CR}	9	—	—	−90	−110	—	—	μA
Output Current, APD_{out} R_o = 240 k, V_{CH} = 0 V V_{APDout} = 4.5 V	I_{APD}	9	—	—	170	350	—	—	μA
Output Current — Other Outputs	I_{OH}								mA
V_{out} = 2.7 V Source		3	−0.44	—	−0.35	—	−0.22	—	
V_{out} = 4.6 V		5	−0.64	—	−0.51	—	−0.36	—	
V_{out} = 8.5 V		9	−1.30	—	−1.00	—	−0.70	—	
V_{out} = 0.3 V Sink	I_{OL}	3	0.44	—	0.35	—	0.22	—	
V_{out} = 0.4 V		5	0.64	—	0.51	—	0.36	—	
V_{out} = 0.5 V		9	1.30	—	1.00	—	0.70	—	
Input Current — Data, Clock, Enable	I_{in}	9	—	±0.3	—	±0.1	—	±1.0	μA
Input Current — f_{in}, OSC_{in}	I_{in}	9	±2	±50	±2	±25	±2	±22	μA
Input Capacitance	C_{in}	—	—	10	—	10	—	10	pF
3-State Output Capacitance — Frequency Steering Out	C_{out}	—	—	10	—	10	—	10	pF
Quiescent Current V_{in} = 0 V or V_{DD} I_{out} = 0 μA	I_{DD}	3	—	800	—	800	—	1600	μA
		5	—	1200	—	1200	—	2400	
		9	—	1600	—	1600	—	3200	
3-State Leakage Current V_{out} = 0 V or 9 V	I_{OZ}	9	—	±0.3	—	±0.1	—	±3.0	μA

*DC-coupled square wave.

goes low. If the counted down VCO frequency is lower than that of the counted down OSC_{in}, this output goes high.

The repetition rate of the frequency steering output pulses is approximately equal to the difference of the frequencies of the two counted down inputs from the VCO and OSC_{in}. See Application Note AN969 for further information.

LD—Phase Lock Indicator (Pin 9)

This output is high during lock and goes low to indicate a non-lock condition. The frequency and duration of the non-lock pulses will be the same as either polarity of the frequency steering output.

Modulus Control—Dual Modulus Prescaler Control (Pin 8)

The modulus control level is low at the beginning of a count cycle and remains low until the divide-by-A counter has counted down from its programmed value. At that time, the modulus control goes high and remains high until the divide-by-N counter has counted the rest of the way down from its programmed value (N – A additional counts, since both divide-by-N and divide-by-A are counting down during the first portion of the cycle). Modulus control is then set back low, the counters preset to their respective programmed values, and the above sequence is repeated. This provides a total programmable divide value of $N_T = N \cdot P + A$, where P and P + 1 represent the dual modulus prescaler divide values, respectively, for high and low modulus control levels; N is the number programmed into the divide-by-N counter, and A is the number programmed into the divide-by-A counter.

SR_{out}—Shift Register Output (Pin 14)

This pin is the non-inverted output of the last stage of the 32-bit serial data shift register. It is not latched by the Enable line. If unused, SR_{out} should be floated.

POWER PINS

V_{DD}—Positive Power Supply (Pin 5)

Positive power supply input for all sections of the device except the analog phase detector. V_{DD} and V_{DD}' should be powered up at the same time to avoid damage to the MC145159-1.

V_{SS}—Negative Power Supply (Pin 7)

Circuit ground for all sections of the MC145159-1 except the analog phase detector.

V_{SS}'—Analog Phase Detector Circuit Ground (Pin 16)
V_{DD}'—Analog Power Supply (Pin 19)

Separate power supply and ground inputs are provided to help reduce the effects in the analog section of noise coming from the digital sections of this device and the surrounding circuitry.

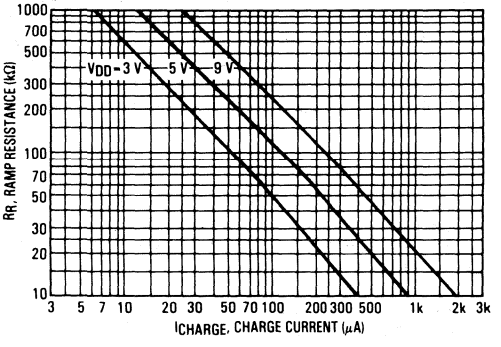


Figure 1. Charge Current vs Ramp Resistance

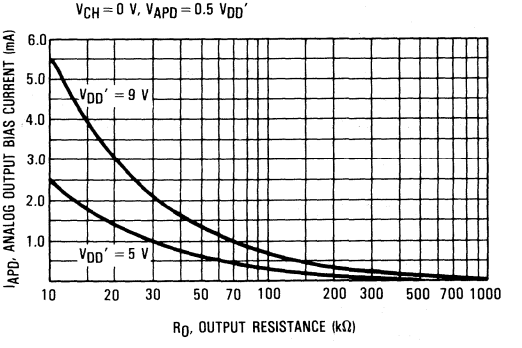


Figure 2. APD_{out} Bias Current versus Output Resistance

DESIGN EQUATION

$$K_\phi = \frac{I_{CHARGE}}{2\pi f_R C_R}$$

where

K_ϕ = phase detector gain, I_{CHARGE} is from Figure 1
f_R = reference frequency
C_R = ramp capacitor (in farads)

SWITCHING WAVEFORMS

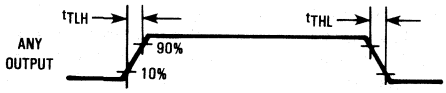


Figure 3

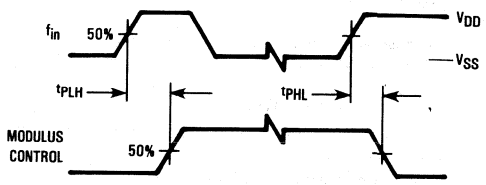


Figure 4

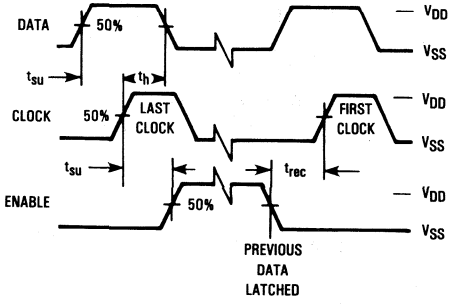


Figure 5

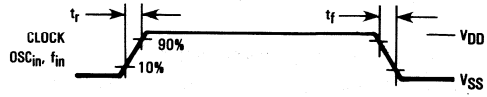


Figure 6

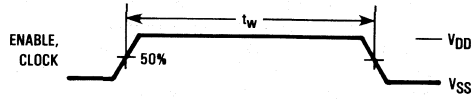


Figure 7

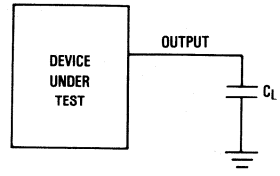


Figure 8. Test Circuit

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

USE OF A HYBRID CRYSTAL OSCILLATOR

Commercially available temperature-compensated crystal oscillators (TCXOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or dc coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct-coupled square wave having a rail-to-rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog*, the *Gold Book*, or similar publications.

DESIGN AN OFF-CHIP REFERENCE

The user may design an off-chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), dc coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct-coupled square wave having rail-to-rail voltage swing.

USE OF THE ON-CHIP OSCILLATOR CIRCUITRY

The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 9.

For $V_{DD} = 5$ V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8 MHz, 20 pF for frequencies in the area of 8 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. Assuming R1 = 0 Ω, the shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in}+C_{out}} + C_a + C_{stray} + \frac{C1 \cdot C2}{C1+C2}$$

where

$C_{in} = 5$ pF (see Figure 10)
$C_{out} = 6$ pF (see Figure 10)
$C_a = 1$ pF (see Figure 10)
C1 and C2 = external capacitors (see Figure 9)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

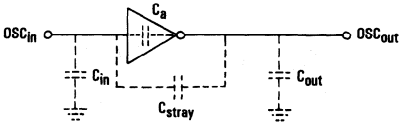
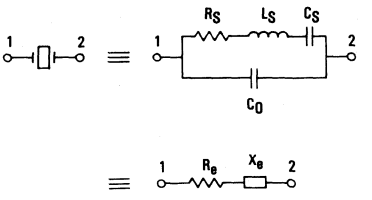
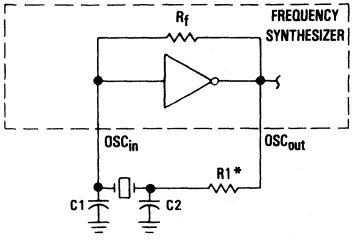


Figure 10. Parasitic Capacitances of the Amplifier and C_{stray}



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 11. Equivalent Crystal Networks



*May be needed in certain cases. See text.

Figure 9. Pierce Crystal Oscillator Circuit

The oscillator can be "trimmed" on-frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes zero in the above expression for C_L.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 11. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 9 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize loading.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. See Table 1.

RECOMMENDED READING

Technical Note TN-24, Statek Corp.

Technical Note TN-7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit—Definitions and Method of Measurement", *Proc. IEEE*, Vol. 57, No. 2, Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro-Technology*, June, 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May, 1966.

D. Babin, "Designing Crystal Oscillators", *Machine Design*, March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", *Machine Design*, April 25, 1985.

Table 1. Partial List of Crystal Manufacturers

Name	Address	Phone
United States Crystal Corp.	3605 McCart Ave., Ft. Worth, TX 76110	(817) 921-3013
Crystek Crystal	2371 Crystal Dr., Ft. Myers, FL 33907	(813) 936-2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639-7810

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

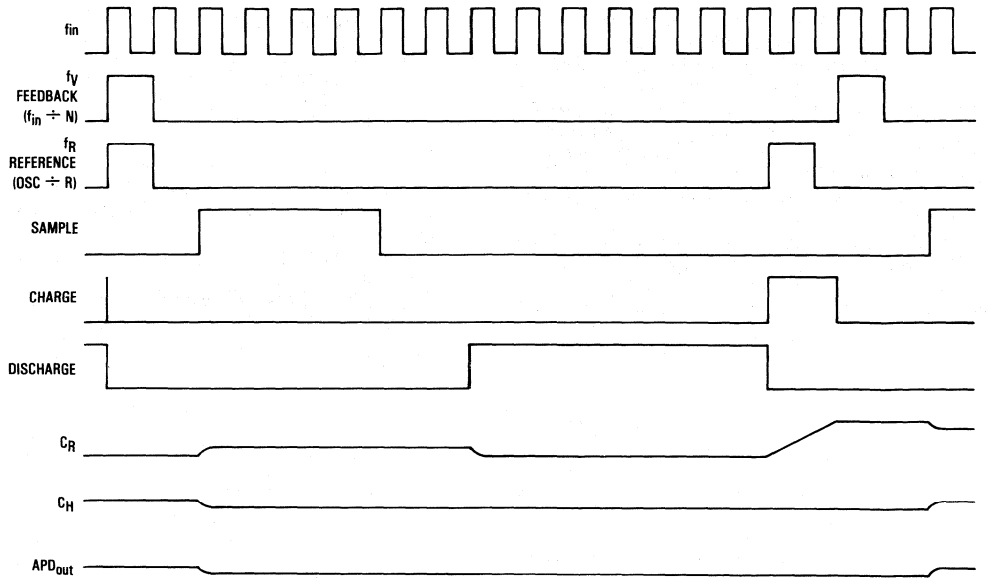


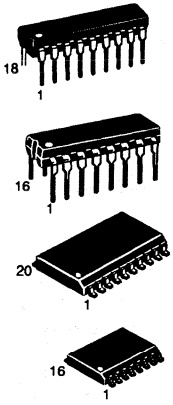
Figure 12. Timing Diagram for Minimum Divide Value (N = 16)

Advance Information

Dual PLLs for 46/49 MHz Cordless Telephones

CMOS

MC145160
MC145166
MC145167



P SUFFIX
PLASTIC DIP
CASE 707

P SUFFIX
PLASTIC DIP
CASE 648

DW SUFFIX
SOG
CASE 751D

DW SUFFIX
SOG
CASE 751G

These devices are dual phase-locked loop frequency synthesizers intended for use primarily in 46/49 MHz cordless phones with up to 10 channels. These parts contain two mask-programmable counter ROMs for receive and transmit loops with two independent phase detect circuits. A common reference oscillator and reference divider are shared by the receive and transmit circuits.

Frequency selection is accomplished via a 4-bit parallel input for the MC145160 and MC145166. The MC145167 utilizes a serial interface.

Other features include a lock detect circuit for the transmit loop, illegal code default, and a 5.0 kHz tone output.

- Synthesizes Up to Ten Channel Pairs
- Maximum Operating Frequency: 60 MHz @ V_{in}=200 mV p-p
- Operating Temperature Range: –40°C to 75°C
- Operating Voltage Range: 2.5 to 5.5 V
- On-Chip Oscillator Circuit Supports External Crystal
- Lock Detect Signal
- Operating Power Consumption: 3.0 mA @ 3.0 V
- Standby Mode for Power Savings: 1.5 mA @ 3.0 V

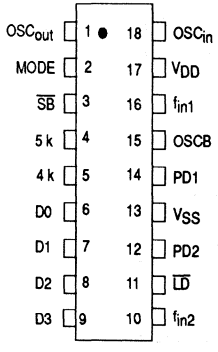
Part Number	4.0 kHz Output	Transmit Frequency	Channel Programming
MC145160	Yes	Half of Fundamental	BCD
MC145166	No	Fundamental	BCD
MC145167	No	Fundamental	Serial

ORDERING INFORMATION

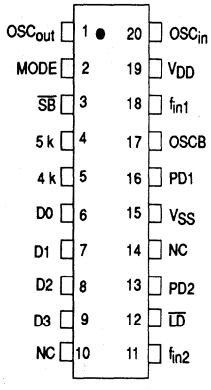
MC145160P	Plastic DIP
MC145160DW	SOG Package
MC145166P	Plastic DIP
MC145166DW	SOG Package
MC145167P	Plastic DIP
MC145167DW	SOG Package

PIN ASSIGNMENTS

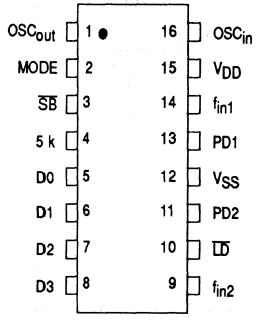
MC145160P



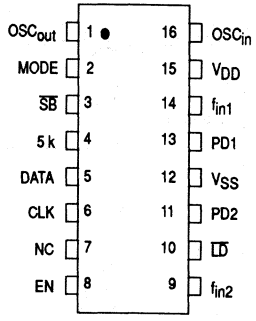
MC145160DW



MC145166P
MC145166DW



MC145167P
MC145167DW



NC=NO CONNECTION

This document contains information on a new product. Specifications and information herein are subject to change without notice.

SWITCHING CHARACTERISTICS (T_A=25°C, C_L=50 pF)

Symbol	Characteristic		V_{DD}	Guaranteed Limit		Unit
				Min	Max	
t_{TLH}	Output Rise Time (Figures 1 and 5)		3.0 5.0	— —	200 100	ns
t_{THL}	Output Fall Time (Figures 1 and 5)		3.0 5.0	— —	200 100	ns
t_r, t_f	Input Rise and Fall Time, OSC_{in} (Figure 2)		3.0 5.0	— —	5.0 4.0	µs
f_{max}	Input Frequency Input=Sine Wave 200 mV p-p	OSC_{in} f_{in1} f_{in2}	3.0-5.0 3.0-5.0 3.0-5.0	— — —	12 60 60	MHz
t_{su}	Setup Time (MC145167) (Figure 3)	Data to Clock	3.0 5.0	100 50	— —	ns
		Enable to Clock	3.0 5.0	200 100	— —	
t_h	Hold Time (MC145167), Clock to Data (Figure 3)		3.0 5.0	80 40	— —	ns
t_{rec}	Recovery Time (MC145167), Enable to Clock (Figure 3)		3.0 5.0	80 40	— —	ns
t_w	Input Pulse Width (MC145167), Clock and Enable (Figure 4)		3.0 5.0	80 60	— —	ns

SWITCHING WAVEFORMS

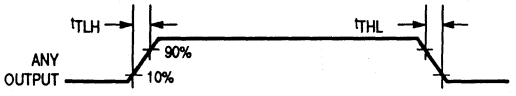


Figure 1.

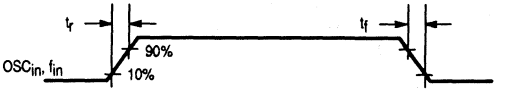


Figure 2.

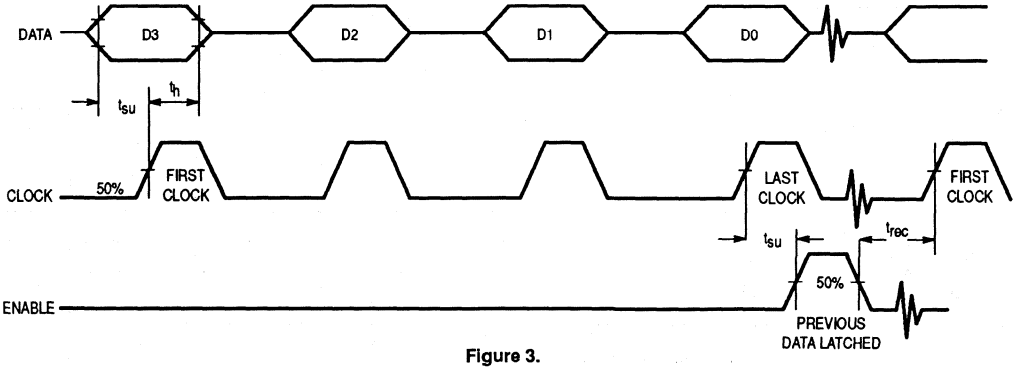


Figure 3.

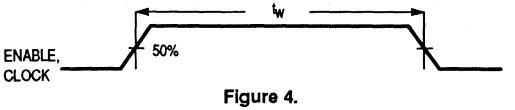


Figure 4.

PIN DESCRIPTIONS

INPUTS

OSC_{in}, OSC_{out}

These pins form a reference oscillator when connected to an external parallel-resonant crystal. For a 46/49 MHz cordless phone application, a 10.24 MHz crystal is needed. OSC_{in} may also serve as input for an externally generated reference signal. This signal is typically ac-coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required for OSC_{out}.

Mode

Mode is for determining whether the part is to be used in the base or handset of a cordless phone. Internally, this pin is used in the decoding logic for selecting the ROM address. When high, the device is set in the base mode, and when low, it is set in the handset mode. This input has an internal pull down device.

$\overline{SB}$

The standby pin is used to save power when not transmitting. When high, both the transmit and receive loops are in operation. When low, the transmit loop is disabled, thereby reducing power consumption. This input has an internal pull down device.

D0 through D3

These inputs provide the BCD code for selecting the one of ten channels to be locked in both the transmit and receive loop. When address data other than 1–10 are input, the decoding logic defaults to channel 10. The frequency assignments with reference to Mode and D0–D3 are shown in Table 2. These inputs have internal pull down devices.

f_{in1}, f_{in2}

f_{in1} and f_{in2} are inputs to the divide-by-N receive and transmit counters, respectively. These signals are typically derived from the loop VCO and are ac coupled. For larger amplitude signals (standard CMOS logic levels), dc coupling may be used. The minimum input level is 200 mV p-p.

Clock, Data

These pins provide the BCD input by using serial channel programming instead of parallel. Logical high represents a "1". Each low to high transition of the clock shifts one bit of data into the on-chip shift register.

Enable

The enable pin controls the data transfer from the shift register to the 4-bit latch. A positive pulse latches the data.

OUTPUTS

5 k, 4k

These are 5 kHz and 4 kHz tone signals derived from the reference oscillator, these are N-channel open drain outputs.

$\overline{LD}$

Lock detect signal associated with the transmit loop. The lock output goes high to indicate an out-of-lock condition. This is a P-channel open-drain output.

PD1, PD2

These are 3-state outputs of the transmit and receive phase detectors for use as loop error signals.
Frequency $f_V > f_r$ or f_V leading: Output=Negative pulses
Frequency $f_V < f_r$ or f_V lagging: Output=Positive pulses
Frequency $f_V = f_r$ and phase coincidence:
Output=High impedance state

OSCB

Buffered output of the on-chip reference oscillator or externally provided reference. This output is available on the MC145160 only.

POWER

V_{SS}

This pin is the negative supply potential and is usually ground.

V_{DD}

This pin is the positive supply potential and may range from +2.5 to +5.5 volts with respect to V_{SS}.

Table 2. MC145166/7 Divide Ratios and VCO Frequencies

Channels					Handset (Mode=0)				Base (Mode=1)			
					f_{in2}—Transmit		f_{in1}—Receive		f_{in2}—Transmit		f_{in1}—Receive	
D3	D2	D1	D0	CH#	F_{vco} (MHz)	÷N	F_{vco} (MHz)	÷N	F_{vco} (MHz)	÷N	F_{vco} (MHz)	÷N
0	0	0	1	1	49.670	9934	35.915	7183	46.610	9322	38.975	7795
0	0	1	0	2	49.845	9969	35.935	7187	46.630	9326	39.150	7830
0	0	1	1	3	49.860	9972	35.975	7195	46.670	9334	39.165	7833
0	1	0	0	4	49.770	9954	36.015	7203	46.710	9342	39.075	7815
0	1	0	1	5	49.875	9975	36.035	7207	46.730	9346	39.180	7836
0	1	1	0	6	49.830	9966	36.075	7215	46.770	9354	39.135	7827
0	1	1	1	7	49.890	9978	36.135	7227	46.830	9366	39.195	7839
1	0	0	0	8	49.930	9986	36.175	7235	46.870	9374	39.235	7847
1	0	0	1	9	49.990	9998	36.235	7247	46.930	9386	39.295	7859
1	0	1	0	10	49.970	9994	36.275	7255	46.970	9394	39.275	7855

NOTES:
1. Other input combinations will be defaulted to channel 10
2. Half the frequency of f_{in2} for MC145160
3. 0=logic low, 1=logic high.

MC145168
MC145169

Advance Information

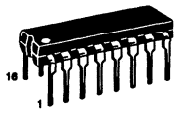
Dual PLLs for 46/49 MHz Cordless Telephones

CMOS

These devices are dual phase-locked loop frequency synthesizers intended for use primarily in 46/49 MHz cordless phones with up to 15 channels. These parts contain two mask-programmable counter ROMs for receive and transmit loops with two independent phase detect circuits. A common reference oscillator and reference divider are shared by the receive and transmit circuits.

Other features include a lock detect circuit for the transmit loop, illegal code default, a buffered oscillator output for mixing purposes in the system, and a 5.0 kHz tone output.

- Maximum Operating Frequency: 60 MHz @ V_{in}=200 mV p-p
- Operating Temperature Range: –40°C to 75°C
- Operating Voltage Range: 2.5 to 5.5 V
- On-Chip Oscillator Circuit Supports External Crystal
- Operating Power Consumption: 3.0 mA @ 3.0 V
- Lock Detect Signal
- Standby Mode for Power Savings: 1.5 mA @ 3.0 V
- Two Versions:
  - MC145168—Up to 15-Channel ROM with 4-Bit Binary Code Input for Channel Pair Selection
  - MC145169—Up to 15-Channel ROM with Serial Interface for Channel Pair Selection
- Custom 20-Channel ROM Versions of the MC145169 are Possible; Consult Factory



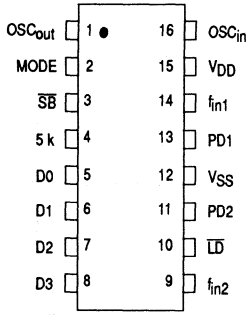
P SUFFIX
PLASTIC DIP
CASE 648

DW SUFFIX
SOG
CASE 751G

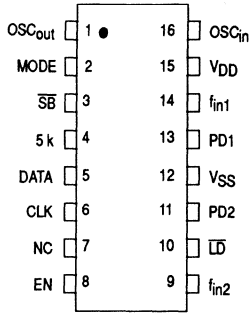
ORDERING INFORMATION

MC145168P	Plastic DIP
MC145168DW	SOG Package
MC145169P	Plastic DIP
MC145169DW	SOG Package

MC145168



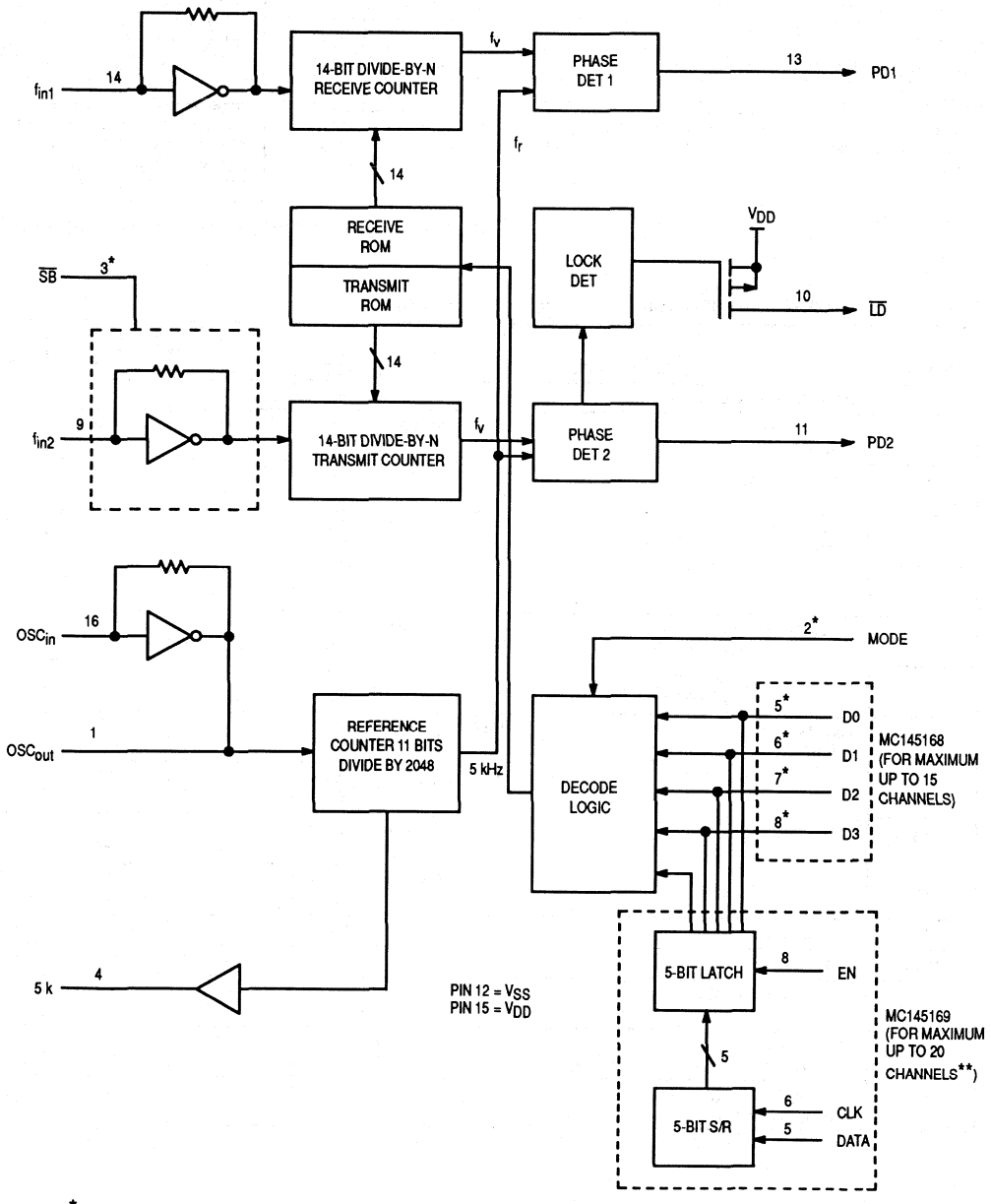
MC145169



NC=NO CONNECTION

This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM



*On chip pull down.

**The standard MC145169 is 15 channels; see Tables 1 and 2. Custom versions up to 20 channels are possible.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Rating	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +6.0	V
V_{in}	Input Voltage, All Inputs	−0.5 to V_{DD}+0.5	V
I_{in}, I_{out}	DC Current Drain Per Pin	10	mA
I_{DD}, I_{SS}	DC Current Drain V_{DD} or V_{SS} Pins	30	mA
T_{stg}	Storage Temperature Range	−65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A=25°C)

Symbol	Characteristic		V_{DD}	Guaranteed Limit Min	Guaranteed Limit Max	Unit
V_{DD}	Power Supply Voltage Range		—	2.5	5.5	V
V_{OL}	Output Voltage (I_{out}=0)	0 Level	2.5 5.5	— —	0.05 0.05	
V_{OH}	(V_{in}=V_{DD} or 0)	1 Level	2.5 5.5	2.45 5.45	— —	V
V_{IL}	Input Voltage (V_{out}=0.5 V or V_{DD}−0.5 V)	0 Level	2.5 5.5	— —	0.75 1.65	V
V_{IH}		1 Level	2.5 5.5	1.75 3.85	— —	
I_{OH}	Output Current (V_{out}=2.2 V) (V_{out}=5.0 V)	Source	2.5 5.5	−0.18 −0.55	— —	mA
I_{OL}	(V_{out}=0.3 V) (V_{out}=0.5 V)	Sink	2.5 5.5	0.18 0.55	— —	
I_{IL}	Input Current (V_{in}=0)	OSC_{in}, f_{in1}, f_{in2}	2.5 5.5	— —	−30 −66	µA
		Data, $\overline{SB}$, Mode	2.5 5.5	— —	−0.05 −0.11	
I_{IH}	(V_{in}=V_{DD}−0.5)	OSC_{in}, f_{in1}, f_{in2}	2.5 5.5	— —	30 66	µA
		Data, $\overline{SB}$, Mode	2.5 5.5	— —	50 121	
C_{in}	Input Capacitance		—	—	8.0	pF
C_{out}	Output Capacitance		—	—	8.0	pF
I_{DD}	Standby Current, $\overline{SB}$=V_{SS} or Open		2.5 5.5	— —	1.4 3.6	mA
I_{dd}	Operating Current (200 mV p-p input at f_{in1}, f_{in2}, $\overline{SB}$=V_{DD})		2.5 5.5	— —	2.8 6.2	mA
I_{OZ}	Three-State Leakage Current (V_{out}=0 V or 5.5 V)		5.5	—	±1.0	µA

SWITCHING CHARACTERISTICS (T_A=25°C, C_L=50 pF)

Symbol	Characteristic		V_{DD}	Guaranteed Limit		Unit
				Min	Max	
t_{TLH}	Output Rise Time (Figures 1 and 5)		3.0 5.0	— —	200 100	ns
t_{THL}	Output Fall Time (Figures 1 and 5)		3.0 5.0	— —	200 100	ns
t_r, t_f	Input Rise and Fall Time, OSC_{in} (Figure 2)		3.0 5.0	— —	5.0 4.0	µs
f_{max}	Input Frequency Input=Sine Wave 200 mV p-p	OSC_{in} f_{in1} f_{in2}	3.0-5.0 3.0-5.0 3.0-5.0	— — —	12 60 60	MHz
t_{su}	Setup Time (MC145169) (Figure 3)	Data to Clock	3.0 5.0	100 50	— —	ns
		Enable to Clock	3.0 5.0	200 100	— —	
t_h	Hold Time (MC145169), Clock to Data (Figure 3)		3.0 5.0	80 40	— —	ns
t_{rec}	Recovery Time (MC145169), Enable to Clock (Figure 3)		3.0 5.0	80 40	— —	ns
t_w	Input Pulse Width (MC145169), Clock and Enable (Figure 4)		3.0 5.0	80 60	— —	ns

SWITCHING WAVEFORMS

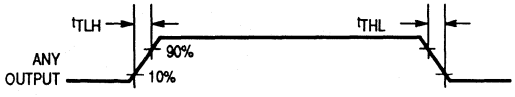


Figure 1.

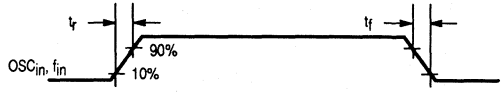


Figure 2.

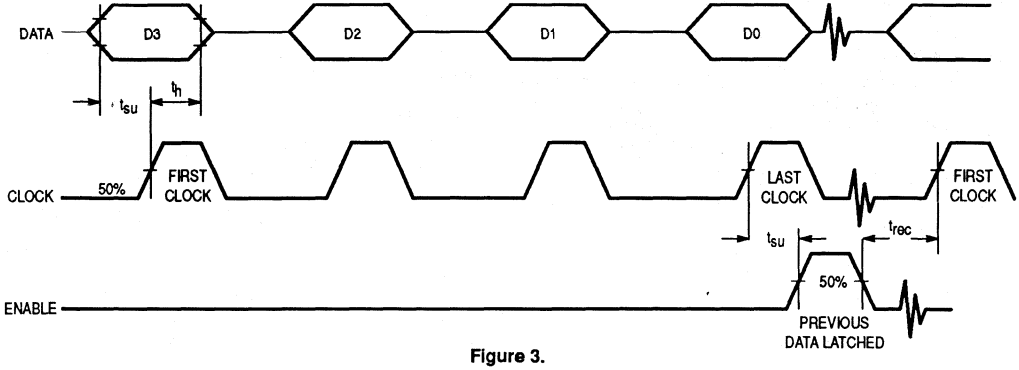


Figure 3.

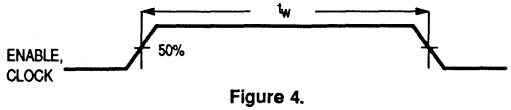


Figure 4.

PIN DESCRIPTIONS

INPUTS

OSC_{in}, OSC_{out} (Pins 16, 1)

These pins form a reference oscillator when connected to an external parallel-resonant crystal. For a 46/49 MHz cordless phone application, a 10.24 MHz crystal is needed. OSC_{in} may also serve as input for an externally generated reference signal. This signal is typically ac-coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required for OSC_{out}.

Mode (Pin 2)

Mode is for determining whether the part is to be used in the base or handset of a cordless phone. Internally, this pin is used in the decoding logic for selecting the ROM address. When high, the device is set in the base mode, and when low, it is set in the handset mode. This input has an internal pull down device.

$\overline{SB}$ (Pin 3)

The standby pin is used to save power when not transmitting. When high, both the transmit and receive loops are in operation. When low, the transmit loop is disabled, thereby reducing power consumption. This input has an internal pull down device.

D0 through D3 (Pins 5, 6, 7, 8) — MC145168 only

These inputs provide the 4-bit binary code for selecting the one of 15 channels for the transmit and receive loops. When address data other than 1–15 are input, the decoding logic defaults to channel 1. The frequency assignments, with reference to Mode and D0–D3, are shown in Tables 1 and 2. These inputs have internal pull down devices.

f_{in1}, f_{in2} (Pins 14, 9)

f_{in1} and f_{in2} are inputs to the divide-by-N receive and transmit counters, respectively. These signals are typically derived from the loop VCO and are ac coupled. The mininum input level is 200 mV p-p. For larger amplitude signals (standard CMOS logic levels), dc coupling may be used.

Data, Clk (Pins 5, 6) — MC145169 only

These pins provide the binary input by using serial channel programming. A logic high represents a "1." Each low-to-high transition of the clock shifts one bit of data into the on-chip shift register. Data is entered MSB first, see Figure 3.

EN (Pin 8) — MC145169 only

The enable pin controls the data transfer from the shift register to the latch. A positive pulse transfers the data. This pin should normally be held low to avoid loading erroneous data into the latch.

OUTPUTS

5 k (Pin 4)

This is a 5 kHz tone signal derived from the reference oscillator. This pin is a push pull output.

$\overline{LD}$ (Pin 10)

Lock detect signal associated with the transmit loop. The lock output goes high to indicate an out-of-lock condition. This is a P-channel open-drain output.

PD1, PD2 (Pins 13, 11)

These are 3-state outputs of the transmit and receive phase detectors for use as loop error signals.

Frequency $f_V > f_r$ or f_V leading: Negative pulses

Frequency $f_V < f_r$ or f_V lagging: Positive pulses

Frequency $f_V = f_r$ and phase coincidence: High impedance state

NOTE: f_V is the output of the N counter. f_r is the output of the reference counter.

POWER

V_{SS} (Pin 12)

This pin is the negative supply potential and is usually ground.

V_{DD} (Pin 15)

This pin is the positive supply potential and may range from +2.5 to +5.5 volts with respect to V_{SS}.

Table 1. Handset Frequencies of Each Corresponding Channel in a 46/49 MHz Cordless Phone for the Korean Market

Channels					RX Freq. (MHz)	Receive (Note 3)		TX Freq. (MHz)	Transmit		Mode
D3	D2	D1	D0	CH#		f_{in1} (MHz)	+N		f_{in2} (MHz)	+N	
0	0	0	1	1	46.610	35.915	7183	49.670	49.670	9934	0
0	0	1	0	2	46.630	35.935	7187	49.845	49.845	9969	0
0	0	1	1	3	46.670	35.975	7195	49.860	49.860	9972	0
0	1	0	0	4	46.710	36.015	7203	49.770	49.770	9954	0
0	1	0	1	5	46.730	36.035	7207	49.875	49.875	9975	0
0	1	1	0	6	46.770	36.075	7215	49.830	49.830	9966	0
0	1	1	1	7	46.830	36.135	7227	49.890	49.890	9978	0
1	0	0	0	8	46.870	36.175	7235	49.930	49.930	9986	0
1	0	0	1	9	46.930	36.235	7247	49.990	49.990	9998	0
1	0	1	0	10	46.970	36.275	7255	49.970	49.970	9994	0
1	0	1	1	11	46.510	35.815	7163	49.695	49.695	9939	0
1	1	0	0	12	46.530	35.835	7167	49.710	49.710	9942	0
1	1	0	1	13	46.550	35.855	7171	49.725	49.725	9945	0
1	1	1	0	14	46.570	35.875	7175	49.740	49.740	9948	0
1	1	1	1	15	46.590	35.895	7179	49.755	49.755	9951	0

NOTES:
1. 0=logic low, 1=logic high.
2. Power up and illegal inputs are defaulted to channel 1 in the MC145169. Illegal inputs are defaulted to channel 1 in MC145168.
3. 1st IF frequency of receive is 10.695 MHz, 2nd IF is 455 kHz.
4. $+N=\frac{f_{in}}{f_{ref}}$ where f_{in} is the VCO frequency and f_{ref} is the reference frequency (5.0 kHz).

Table 2. Base Frequencies of Each Corresponding Channel in a 46/49 MHz Cordless Phone for the Korean Market

Channels					RX Freq. (MHz)	Receive (Note 3)		TX Freq. (MHz)	Transmit		Mode
D3	D2	D1	D0	CH#		f_{in1} (MHz)	+N		f_{in2} (MHz)	+N	
0	0	0	1	1	49.670	38.975	7795	46.610	46.610	9322	1
0	0	1	0	2	49.845	39.150	7830	46.630	46.630	9326	1
0	0	1	1	3	49.860	39.165	7833	46.670	46.670	9334	1
0	1	0	0	4	49.770	39.075	7815	46.710	46.710	9342	1
0	1	0	1	5	49.875	39.180	7836	46.730	46.730	9346	1
0	1	1	0	6	49.830	39.135	7827	46.770	46.770	9354	1
0	1	1	1	7	49.890	39.195	7839	46.830	46.830	9366	1
1	0	0	0	8	49.930	39.235	7847	46.870	46.870	9374	1
1	0	0	1	9	49.990	39.295	7859	46.930	46.930	9386	1
1	0	1	0	10	49.970	39.275	7855	46.970	46.970	9394	1
1	0	1	1	11	49.695	39.000	7800	46.510	46.510	9302	1
1	1	0	0	12	49.710	39.015	7803	46.530	46.530	9306	1
1	1	0	1	13	49.725	39.030	7806	46.550	46.550	9310	1
1	1	1	0	14	49.740	39.045	7809	46.570	46.570	9314	1
1	1	1	1	15	49.755	39.060	7812	46.590	46.590	9318	1

NOTES:
1. 0=logic low, 1=logic high.
2. Power up and illegal inputs are defaulted to channel 1 in the MC145169. Illegal inputs are defaulted to channel 1 in MC145168.
3. 1st IF frequency of receive is 10.695 MHz, 2nd IF is 455 kHz.
4. $+N=\frac{f_{in}}{f_{ref}}$ where f_{in} is the VCO frequency and f_{ref} is the reference frequency (5.0 kHz).

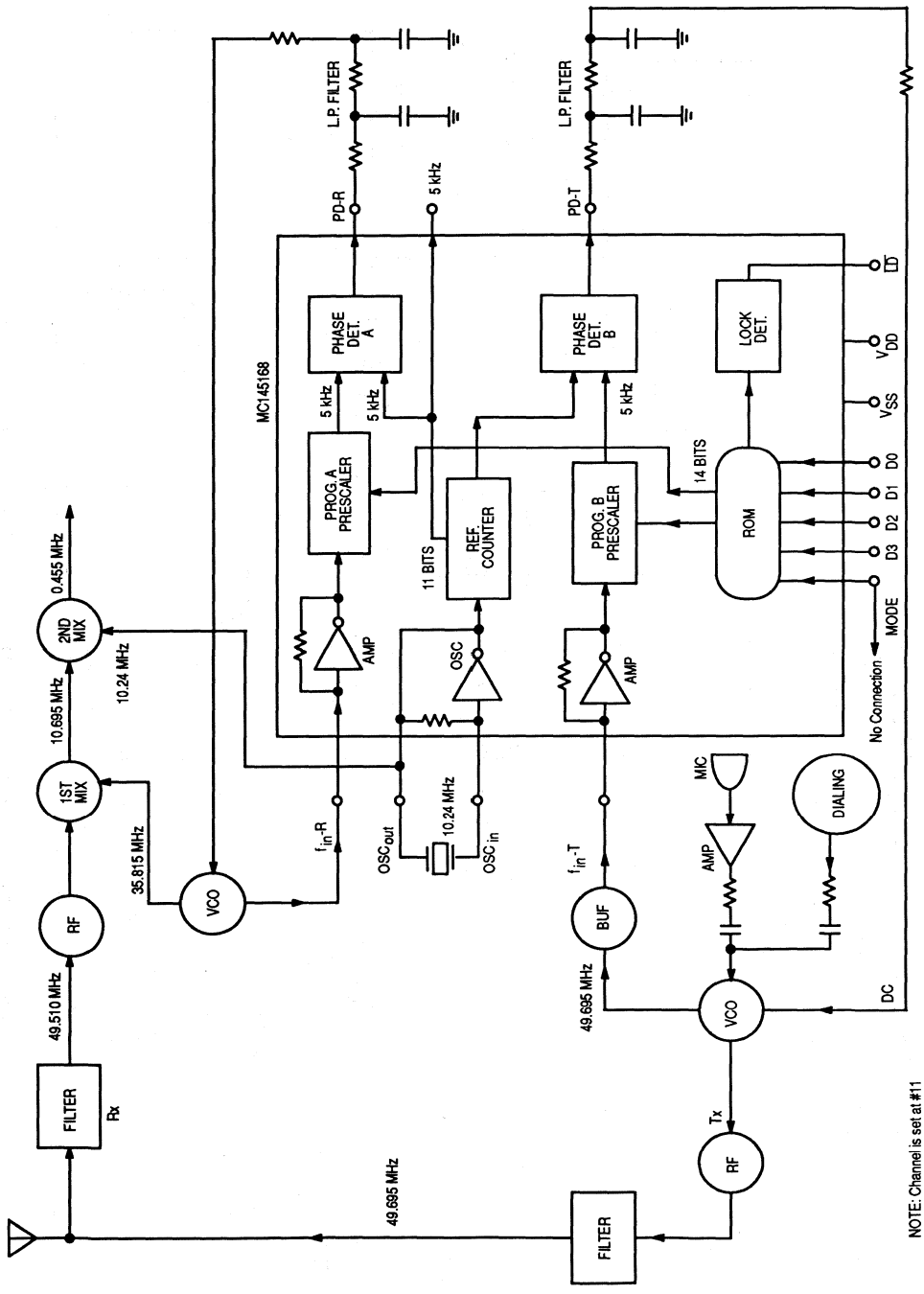
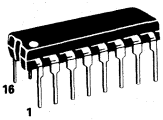


Figure 6b. DPLL Application In 46/49 MHz Cordless Phone 15-Channel Handset

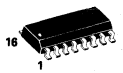
MC145170

Product Preview

PLL Frequency Synthesizer with Serial Interface
CMOS



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOG
CASE 751B

ORDERING INFORMATION

MC145170P	Plastic DIP
MC145170D	SOG Package

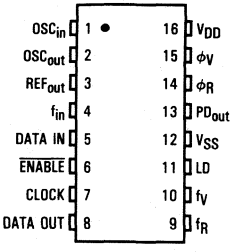
The MC145170 is a single-chip synthesizer capable of direct usage in the MF, HF, and VHF bands. A special architecture makes this PLL the easiest to program in the industry. Either a bit- or byte-oriented format may be used. Due to the BitGrabber registers,* no address/steering bits are required for random access of the three registers. Thus, tuning can be accomplished via a 2-byte serial transfer to the 16-bit N register.

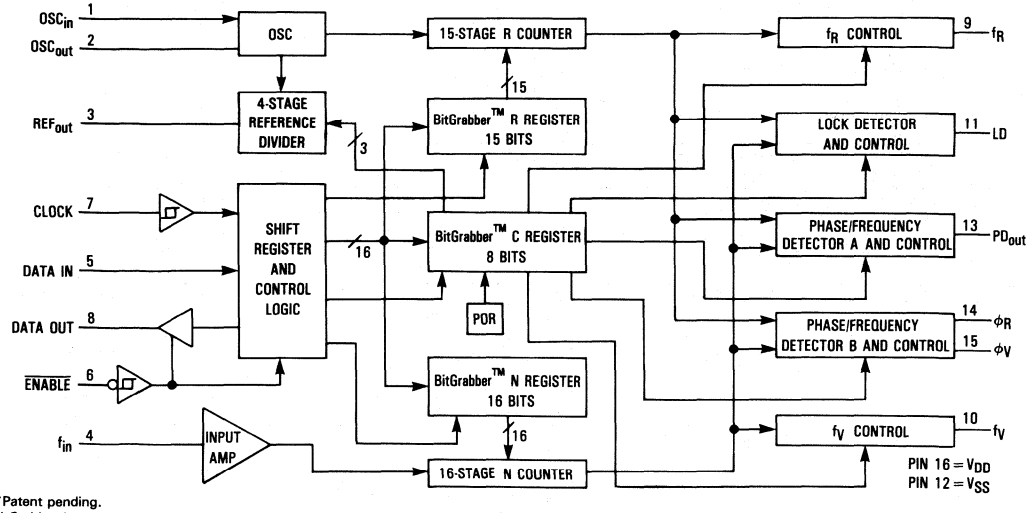
The device features fully-programmable R and N counters, an amplifier at the f_{in} pin, on-chip support of an external crystal, a programmable reference output, and both single- and double-ended phase detectors with linear transfer functions. A new feature on the MC145170 is the C register (configuration register). The C register allows the part to be configured to meet various applications. Also, the C register allows unused outputs to be shut off,* thereby minimizing system noise and interference.

In order to reduce lock times and prevent erroneous data from being loaded into the counters, a patented jam-load feature is included. Whenever a new divide ratio is loaded into the N register, both the N and R counters are jam loaded with their respective values and begin counting down together. The phase detectors are also initialized during the jam load.

- Operating Voltage Range: 2.5 to 6 V
- Maximum f_{in} Operating Frequency: 160 MHz @ V_{in} = 500 mV_{p-p}, 4.5 to 6 V Supply
- Operating Temperature Range: −40° to 85°C
- R Counter Division Range: 5 to 32,767 Plus Direct Access to Phase Detector Input
- N Counter Division Range: 40 to 65,535
- Direct Interface to Motorola/RCA SPI and National MICROWIRE Serial Data Ports
- 180 MHz Version Available (Part Number SC370566), Consult Factory
- Chip Complexity: 4800 FETs or 1200 Equivalent Gates

PIN ASSIGNMENT





*Patent pending.

BitGrabber is a trademark of Motorola Inc. MICROWIRE is a trademark of National Semiconductor Corp.

MAXIMUM RATINGS* (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +6.0	V
V_{in}	DC Input Voltage	−0.5 to V_{DD}+0.5	V
V_{out}	DC Output Voltage	−0.5 to V_{DD}+0.5	V
I_{in}	DC Input Current, per Pin	±10	mA
I_{out}	DC Output Current, per Pin	±20	mA
I_{DD}	DC Supply Current, V_{DD} and V_{SS} Pins	±30	mA
P_D	Power Dissipation, per Package	300	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A = −40° to 85°C unless otherwise indicated)

Symbol	Parameter	Test Condition	V_{DD} V	Guaranteed Limit	Unit
V_{DD}	Power Supply Voltage Range		–	2.5 to 6.0	V
V_{IL}	Maximum Low-Level Input Voltage (Data In, Clock, $\overline{\text{Enable}}$)		2.5 4.5 6.0	0.5 1.35 1.8	V
V_{IH}	Minimum High-Level Input Voltage (Data In, Clock, $\overline{\text{Enable}}$)		2.5 4.5 6.0	2.0 3.15 4.2	V
V_{Hys}	Minimum Hysteresis Voltage (Clock, $\overline{\text{Enable}}$)		2.5 6.0	0.15 0.2	V
V_{OL}	Maximum Low-Level Output Voltage (Any Output)	I_{out} = 20 μA	2.5 6.0	0.1 0.1	V
V_{OH}	Minimum High-Level Output Voltage (Any Output)	I_{out} = −20 μA	2.5 6.0	2.4 5.9	V
I_{OL}	Minimum Low-Level Output Current (PD_{out}, REF_{out}, f_R, f_V, LD, ϕ_R, ϕ_V)	V_{out} = 0.3 V V_{out} = 0.4 V V_{out} = 0.5 V	2.5 4.5 6.0	0.12 0.36 0.5	mA
I_{OH}	Minimum High-Level Output Current (PD_{out}, REF_{out}, f_R, f_V, LD, ϕ_R, ϕ_V)	V_{out} = 2.2 V V_{out} = 4.1 V V_{out} = 5.5 V	2.5 4.5 6.0	−0.12 −0.36 −0.5	mA
I_{OL}	Minimum Low-Level Output Current (Data Out)	V_{out} = 0.4 V	4.5	1.6	mA
I_{OH}	Minimum High-Level Output Current (Data Out)	V_{out} = 4.1 V	4.5	−1.6	mA
I_{in}	Maximum Input Leakage Current (Data In, Clock, $\overline{\text{Enable}}$, OSC_{in})	$V_{in} = V_{DD}$ or V_{SS}	6.0	±1.0	μA
		$V_{in} = V_{DD}$ or V_{SS}, T_A = 25°C only	6.0	±0.1	
I_{in}	Maximum Input Current (f_{in})	$V_{in} = V_{DD}$ or V_{SS}	6.0	±120	μA
I_{OZ}	Maximum Output Leakage Current (PD_{out})	$V_{in} = V_{DD}$ or V_{SS}, Output in High-Impedance State	6.0	±100	nA
	(Data Out)		6.0	±5	μA
I_{DD}	Maximum Quiescent Supply Current	$V_{in} = V_{DD}$ or V_{SS}, Outputs Open, Excluding f_{in} Amp Input Current Component	6.0	100	μA
		Same as Above, T_A = 25°C only	6.0	TBD	
I_{dd}	Maximum Operating Supply Current	f_{in} = 160 MHz @ 500 mV_{p-p}; OSC_{in} = 10 MHz @ 1 V_{p-p}; f_R, f_V, REF_{out} = Inactive and No Connect; OSC_{out}, ϕ_V, ϕ_R, PD_{out}, LD = No Connect; Data In, $\overline{\text{Enable}}$, Clock = V_{DD} or V_{SS}	4.5 6.0	TBD TBD	mA

AC INTERFACE CHARACTERISTICS ($T_A = -40°$ to 85°C, $C_L = 50$ pF, Input $t_r = t_f = 10$ ns unless otherwise indicated)

Symbol	Parameter	V_{DD} V	Guaranteed Limit	Unit
f_{clk}	Serial Data Clock Frequency NOTE: Refer to Clock t_w below (Figure 1)	2.5 4.5 6.0	dc to TBD dc to 4.0 dc to 4.0	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Data Out (Figures 1 and 5)	2.5 4.5 6.0	TBD 85 85	ns
t_{PLZ}, t_{PHZ}	Maximum Disable Time, Data Out Active to High Impedance (Figures 2 and 6)	2.5 4.5 6.0	TBD 200 200	ns
t_{PZL}, t_{PZH}	Access Time, Data Out High Impedance to Active (Figures 2 and 6)	2.5 4.5 6.0	TBD 0 to 100 0 to 100	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Data Out (Figures 1 and 5), $C_L = 50$ pF	2.5 4.5 6.0	TBD 50 50	ns
	$C_L = 200$ pF	2.5 4.5 6.0	TBD 150 150	
C_{in}	Maximum Input Capacitance—Data In, Clock, $\overline{\text{Enable}}$	—	10	pF
C_{out}	Maximum Output Capacitance—Data Out	—	15	pF

TIMING REQUIREMENTS ($T_A = -40°$ to 85°C, Input $t_r = t_f = 10$ ns unless otherwise indicated)

Symbol	Parameter	V_{DD} V	Guaranteed Limit	Unit
t_{su}, t_h	Minimum Setup and Hold Times, Data In versus Clock (Figure 3)	2.5 4.5 6.0	TBD 40 40	ns
t_{su}, t_h, t_{rec}	Minimum Setup, Hold, and Recovery Times, $\overline{\text{Enable}}$ versus Clock (Figure 4)	2.5 4.5 6.0	TBD 100 100	ns
$t_{w(H)}$	Minimum Inactive-High Pulse Width, $\overline{\text{Enable}}$ (Figure 4)	2.5 4.5 6.0	TBD 300 300	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	2.5 4.5 6.0	TBD 125 125	ns
t_r, t_f	Maximum Input Rise and Fall Times—Clock, $\overline{\text{Enable}}$ (Figure 1)	2.5 4.5 6.0	100 100 100	μs

SWITCHING WAVEFORMS

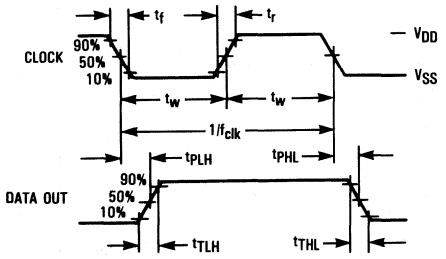


Figure 1

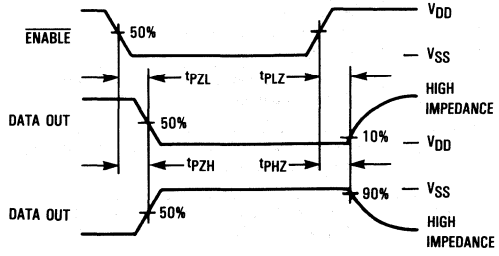


Figure 2

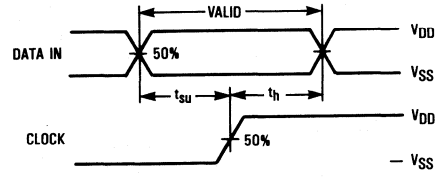


Figure 3

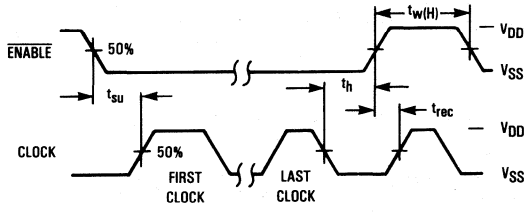
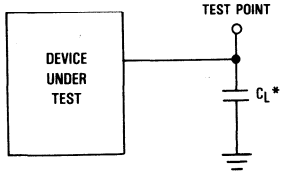
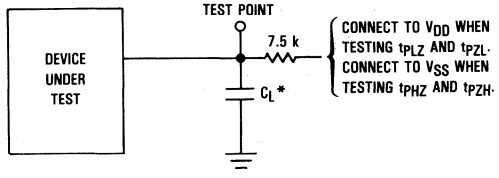


Figure 4



*Includes all probe and jig capacitance.

Figure 5. Test Circuit



*Includes all probe and jig capacitance.

Figure 6. Test Circuit

LOOP SPECIFICATIONS (T_A = −40° to 85°C)

Symbol	Parameter	Test Condition	V_{DD} V	Guaranteed Limit		Unit
				Min	Max	
f_{in}	Input Frequency, f_{in} (Figure 7)	V_{in} = 500 mV_{p-p} Sine Wave, N Counter set to divide ratio such that $f_V \leq 2$ MHz	2.5	TBD	TBD	MHz
			3.0	TBD	100	
			4.5	TBD	160	
			6.0	TBD	160	
f_{in}	Input Frequency, OSC_{in} Externally Driven (Figure 8)	V_{in} = 1 V_{p-p}, OSC_{out} = No Connect, R Counter set to divide ratio such that $f_R \leq 2$ MHz	2.5	1	12	MHz
			3.0	1	14	
			4.5	1	20	
			6.0	1	20	
f_{XTAL}	Crystal Frequency, OSC_{in} and OSC_{out} (Figure 9)	C1 ≤ 30 pF, C2 ≤ 30 pF, Includes Stray Capacitance	2.5	2	12	MHz
			3.0	2	12	
			4.5	2	15	
			6.0	2	15	
f_{out}	Output Frequency, REF_{out} (Figures 10 and 12)	C_L = 30 pF	2.5	dc	TBD	MHz
			3.0	dc	TBD	
			4.5	dc	10	
			6.0	dc	10	
f	Operating Frequency of the Phase Detectors		2.5	dc	TBD	MHz
			3.0	dc	TBD	
			4.5	dc	2	
			6.0	dc	2	
t_W	Output Pulse Width, ϕ_R, ϕ_V, and LD (Figures 11 and 12)	f_R in Phase with f_V, C_L = 50 pF	2.5	TBD	TBD	ns
			3.0	TBD	TBD	
			4.5	20	100	
			6.0	16	90	
t_{TLH}, t_{THL}	Output Transition Times, LD, f_V, f_R, ϕ_V, and ϕ_R (Figures 11 and 12)	C_L = 50 pF	2.5	–	TBD	ns
			3.0	–	TBD	
			4.5	–	65	
			6.0	–	60	
C_{in}	Input Capacitance, f_{in}		–	–	5	pF
	OSC_{in}		–	–	5	

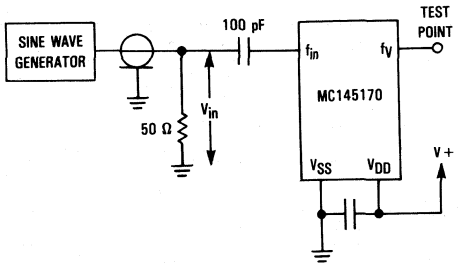


Figure 7. Test Circuit

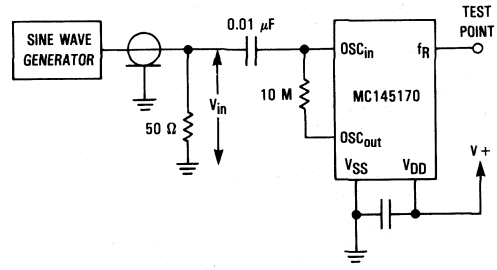


Figure 8. Test Circuit

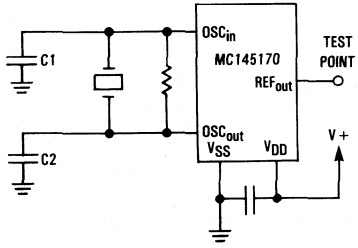


Figure 9. Test Circuit

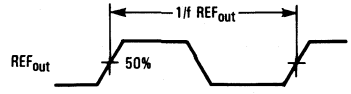


Figure 10. Switching Waveform

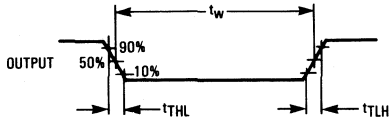
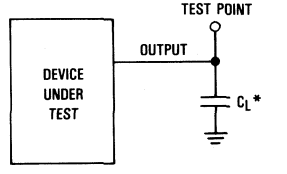


Figure 11. Switching Waveform



*Includes all probe and jig capacitance.

Figure 12. Test Circuit

PIN DESCRIPTIONS

DIGITAL INTERFACE

Data In (Pin 5)

Serial Data Input. The bit stream begins with the MSB and is shifted in on the low-to-high transition of Clock. The bit pattern is 1 byte (8 bits) long to access the C or configuration register, 2 bytes (16 bits) to access the N register, or 3 bytes (24 bits) to access the R or reference register. Optionally, the R register can be accessed with a 15-bit transfer. See Table 1. The values in the C, N, and R registers do not change during shifting because the transfer of data to the registers is controlled by $\overline{\text{Enable}}$.

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the three registers. Random access of any register is provided. That is, the registers may be accessed in any sequence. Data is retained in the registers over a supply range of 2.5 to 6 V. The formats are shown in Figures 13, 14, and 15.

Data In typically switches near 50% of V_{DD} to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail-to-rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pullup resistor of 1 kΩ to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst-case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Table 1. Register Access

(MSBs are shifted in first. C0, N0, and R0 are the LSBs)

No. of Clocks	Accessed Register	Bit Nomenclature
8	C Register	C7, C6, C5, . . ., C0
16	N Register	N15, N14, N13, . . ., N0
15 or 24	R Register	R14, R13, R12, . . ., R0
Other Values ≤32	None	
Values >32	Not Allowed	

Clock (Pin 7)

Serial Data Clock Input. Low-to-high transitions on Clock shift bits available at Data In, while high-to-low transitions shift bits from Data Out. The chip's 16-1/2-stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Eight clock cycles are required to access the C register. Sixteen clock cycles are needed for the N register. Either 15 or 24 can be used to access the R register. See Table 1 and Figures 13, 14, and 15.

Clock typically switches near 50% of V_{DD} and has a Schmitt-triggered input buffer. Slow Clock rise and fall times are allowed. See the last paragraph of **Data In** for more information.

$\overline{\text{Enable}}$ (Pin 6)

Active-Low Enable Input. This pin is used to activate the serial interface to allow the transfer of data to/from the MC145170. When $\overline{\text{Enable}}$ is in an inactive high state, Data Out is forced to the high-impedance state, shifting is inhibited, and the port is held in the initialized state. To transfer data to the device, $\overline{\text{Enable}}$ (which must start inactive high) is taken low, a serial transfer is made via Data In and Clock, and $\overline{\text{Enable}}$ is taken back high. The low-to-high transition on $\overline{\text{Enable}}$ transfers data to the C, N, or R register, depending on the data stream length per Table 1.

CAUTION

Transitions on $\overline{\text{Enable}}$ must not be attempted while Clock is high.

This input is also Schmitt-triggered and switches near 50% of V_{DD}, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of **Data In** for more information.

Data Out (Pin 8)

Three-State Serial Data Output. Data is transferred out of the 16-1/2-stage shift register through Data Out on the high-to-low transition of Clock. This output is a no connect, unless used in one of the manners discussed below.

Data Out could be fed back to an MCU/MPU to perform a wrap-around test of serial data. This could be part of a system check conducted at power up to test the integrity of the system's processor, PC board traces, solder joints, etc.

The pin could be monitored at an in-line QA test during board manufacturing.

Finally, Data Out facilitates troubleshooting a system.

REFERENCE PINS

OSC_{in} and OSC_{out} (Pins 1 and 2)

Oscillator Input and Output. These pins form a reference oscillator when connected to terminals of an external parallel-resonant crystal. Frequency-setting capacitors of appropriate values as recommended by the crystal supplier are connected from each pin to ground (up to a maximum of 30 pF each, including stray capacitance). An external feedback resistor of 1 MΩ to 15 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The MC145170 is designed to operate with crystals up to 15 MHz with a 4.5 to 6 V supply. With supplies less than 4.5 V, up to 12 MHz crystals may be used. See Figure 9.

If desired, an external clock source can be ac coupled to OSC_{in}. A 0.01 μF coupling capacitor is used for measurement purposes and is the minimum size recommended for applications. An external feedback resistor of approximately 10 MΩ is required across the OSC_{in} and OSC_{out} pins in the ac-coupled case. (See Figure 8.) *OSC_{out} is an internal node on the device and should not be used to drive any loads.* That is, OSC_{out} is unbuffered. However, the buffered REF_{out} is available to drive external loads.

The external signal level must be at least 1 V_{p-p}; the maximum frequencies are given in the **Loop Specifications** table. These maximum frequencies apply for R Counter divide ratios as indicated in the table. For very small ratios, the maximum frequency is limited to the divide ratio times 2 MHz when the internal phase/frequency detectors are used. (Reason: the phase/frequency detectors are limited to a maximum input frequency of 2 MHz.)

If an external source is available which swings from at least the V_{IL} to V_{IH} levels listed in the **Electrical Characteristics** table, then dc coupling can be used. In the dc-coupled case, no external feedback resistor is needed. OSC_{out} must be a no connect to avoid loading an internal node on the MC145170, as above.

Each rising edge on the OSC_{in} pin causes the R counter to decrement by one.

REF_{out} (Pin 3)

Reference Frequency Output. This output is the buffered output of the crystal-generated reference frequency or externally-provided reference source. This output may be enabled, disabled, or scaled via bits in the C register. See Figure 13.

REF_{out} can be used to drive a microprocessor clock input, thereby saving a crystal. Upon power up, the on-chip power-on-initialize circuit forces REF_{out} to the OSC_{in} divided-by-8 mode.

REF_{out} is capable of operation to 10 MHz; see the **Loop Specifications** table. Therefore, divide values for the reference divider are restricted to two or higher for OSC_{in} frequencies above 10 MHz.

If unused, the pin should be floated and should be disabled via the C register to minimize dynamic power consumption and electromagnetic interference (EMI).

COUNTER OUTPUTS

f_R (Pin 9)

Reference Counter Output. This signal is the buffered output of the 15-stage R counter. f_R can be enabled or disabled via the C register. (Patent pending.) The output is disabled (static low logic level) upon power up. If unused, the output should be left disabled and unconnected to minimize interference with external circuitry.

The f_R signal can be used to verify the R counter's divide ratio. This ratio extends from 5 to 32,767 and is determined by the binary value loaded into the R register. Also, direct access to the phase detector via the OSC_{in} pin is allowed by choosing a divide value of one. See Figure 14. The maximum frequency which the phase detectors operate is 2 MHz. Therefore, the frequency of f_R must not exceed 2 MHz unless an external phase detector is used. The maximum frequency for driving external phase detectors is TBD.

When activated, the f_R signal appears as normally low. f_R pulses high whenever the R counter is loading the value from the R register.

f_V (Pin 10)

N Counter Output. This signal is the buffered output of the 16-stage N counter. f_V can be enabled or disabled via the C register. (Patent pending.) The output is disabled (static low logic level) upon power up. If unused, the output should be left disabled and unconnected to minimize interference with external circuitry.

The f_V signal can be used to verify the N counter's divide ratio. This ratio extends from 40 to 65,535 and is determined by the binary value loaded into the N register. The maximum frequency which the phase detectors operate is 2 MHz. Therefore, the frequency of f_V must not exceed 2 MHz unless an external phase detector is used. The maximum frequency for driving external phase detectors is TBD.

When activated, the f_V signal appears as normally low. f_V pulses high whenever the N counter is loading the value from the N register.

LOOP PINS

f_{in} (Pin 4)

Frequency Input from the VCO. This pin feeds the on-chip amplifier which drives the N counter. This signal is normally sourced from an external voltage-controlled oscillator (VCO), and is ac-coupled into f_{in}. A 100 pF coupling capacitor is used for measurement purposes and is the minimum size recommended for applications. (See Figure 7.) The frequency capability of this input is dependent on the input signal level for the divide ratios listed in the **Loop Specifications** table. For small divide ratios, the maximum frequency is limited to the divide ratio times 2 MHz when the internal phase/frequency detectors are used. (Reason: the phase/frequency detectors are limited to a maximum frequency of 2 MHz.)

For signals which swing from at least the V_{IL} to V_{IH} levels listed in the **Electrical Characteristics** table, dc coupling may be used.

Each rising edge on the f_{in} pin causes the N counter to *decrement by one.*

PD_{out} (Pin 13)

Single-Ended Phase/Frequency Detector Output. This is a 3-state output for use as a loop error signal when combined with an external low-pass filter. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 16.

POL bit (C7) in the C register = low (see Figure 13)
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: negative pulses from high impedance
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: positive pulses from high impedance
- Frequency and Phase of $f_V = f_R$: essentially high-impedance state; voltage at pin determined by loop filter

POL bit (C7) = high
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: positive pulses from high impedance
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: negative pulses from high impedance
- Frequency and Phase of $f_V = f_R$: essentially high-impedance state; voltage at pin determined by loop filter

This output can be enabled, disabled, and inverted via the C register. If desired, PD_{out} can be forced to the high-impedance state by utilization of the disable feature in the C register. (Patent pending.)

ϕ_R and ϕ_V (Pins 14 and 15)

Doubled-Ended Phase/Frequency Detector Outputs. These outputs can be combined externally to generate a loop error signal. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 16.

POL bit (C7) in the C register = low (see Figure 13)
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_V = negative pulses, ϕ_R = essentially high
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_V = essentially high, ϕ_R = negative pulses
- Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

POL bit (C7) = high
Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_R = negative pulses, ϕ_V = essentially high
Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_R = essentially high, ϕ_V = negative pulses
Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, and interchanged via the C register. (Patent pending.)

LD (Pin 11)

Lock Detector Output. This output is essentially at a high level with narrow low-going pulses when the loop is locked (f_R and f_V of the same phase and frequency). The output pulses low when f_V and f_R are out of phase or different frequencies. See Figure 16.

This output can be enabled and disabled via the C register. (Patent pending.) Upon power up, on-chip initialization circuitry disables LD to a static low logic level to prevent a false "lock" signal. If unused, LD should be disabled and left open.

POWER SUPPLY

V_{DD} (Pin 16)

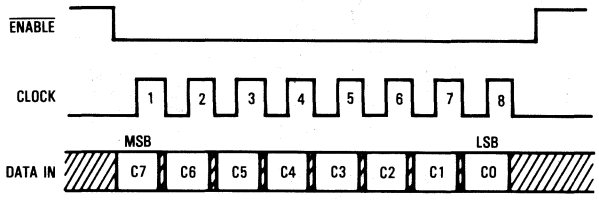
Most-Positive Supply Potential. This pin may range from +2.5 to +6 V with respect to V_{SS}.

For optimum performance, V_{DD} should be bypassed to V_{SS} using (a) low-inductance capacitor(s) mounted very close to the MC145170. Lead lengths on the capacitor(s) should be minimized. (The very-fast switching speed of the device causes current spikes on the power leads.)

V_{SS} (Pin 12)

Most-Negative Supply Potential. This pin is usually ground.

For measurement purposes, the V_{SS} pin is tied to a ground plane.



NOTE:

C7-POL: Selects the output polarity of the phase/frequency detectors. When set high, this bit inverts PD_{out} and interchanges ϕ_R function with ϕ_V as depicted in Figure 16. Also see the phase detector output pin descriptions for more information. This bit is cleared low at power up.

C6-PDA/B: Selects which phase/frequency detector is to be used. When set high, enables the output of phase/frequency detector A (PD_{out}) and disables phase/frequency detector B by forcing ϕ_R and ϕ_V to the static high state. When cleared low, phase/frequency detector B is enabled (ϕ_R and ϕ_V) and phase/frequency detector A is disabled with PD_{out} forced to the high-impedance state. This bit is cleared low at power up.

C5-LDE: Enables the lock detector output when set high. When the bit is cleared low, the LD output is forced to a static low level. This bit is cleared low at power up.

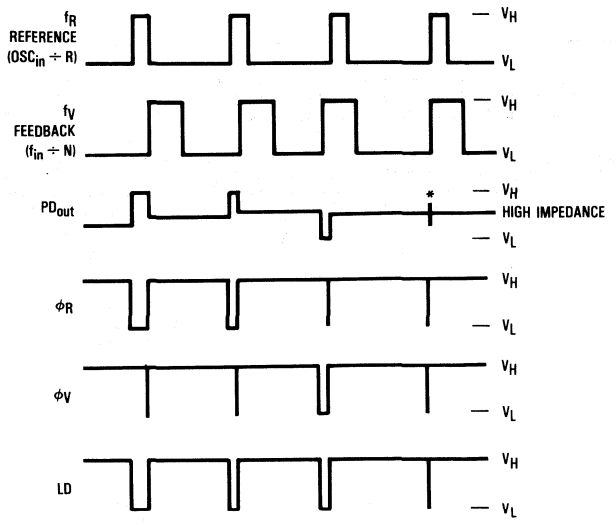
C4, C3, C2-OSC2, OSC1, OSC0: Reference output controls which determine the REF_{out} characteristics as shown below. Upon power up, the bits are initialized such that $OSC_{in}/8$ is selected.

C4	C3	C2	REF_{out} Frequency
0	0	0	dc (Static Low)
0	0	1	OSC_{in}
0	1	0	$OSC_{in}/2$
0	1	1	$OSC_{in}/4$
1	0	0	$OSC_{in}/8$
1	0	1	$OSC_{in}/16$
1	1	0	$OSC_{in}/8$
1	1	1	$OSC_{in}/16$

C1-f_VE: Enables the f_V output when set high. When cleared low, the f_V output is forced to a static low level. The bit is cleared low upon power up.

C0-f_RE: Enables the f_R output when set high. When cleared low, the f_R output is forced to a static low level. The bit is cleared low upon power up.

Figure 13. C Register Access and Format (8 Clock Cycles Are Used)



V_H = High voltage level
V_L = Low voltage level
*At this point, when both f_R and f_V are in phase, the output is forced to near mid supply.
NOTE: The PD_{out} output generates error pulses during out-of-lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low-pass filter capacitor. PD_{out}, ϕR, and ϕV are shown with the polarity bit (POL) = low; see Figure 13 for POL.

Figure 16. Phase/Frequency Detectors and Lock Detector Output Waveforms

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

USE OF A HYBRID CRYSTAL OSCILLATOR

Commercially available temperature-compensated crystal oscillators (TCXOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to OSC_{in}. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. See Figure 8.

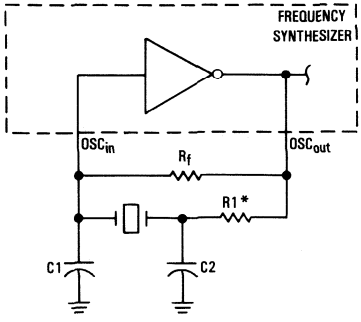
For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

DESIGN AN OFF-CHIP REFERENCE

The user may design an off-chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to OSC_{in}. (See Figure 8.) For large amplitude signals (standard CMOS logic levels), dc coupling is used.

USE OF THE ON-CHIP OSCILLATOR CIRCUITRY

The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 17.



*May be needed in certain cases. See text.

Figure 17. Pierce Crystal Oscillator Circuit

For $V_{DD} = 5$ V, the crystal should be specified for a loading capacitance, C_L, which does not exceed approximately 12 pF when used at the highest operating frequency of 15 MHz. Larger C_L values are possible for lower frequencies. Assuming R1 = 0 Ω, the shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in}+C_{out}} + C_a + C_{stray} + \frac{C1 \cdot C2}{C1+C2}$$

where

C_{in} = 5 pF (see Figure 18)
C_{out} = 6 pF (see Figure 18)
C_a = 1 pF (see Figure 18)
C1 and C2 = external capacitors (see Figure 17)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

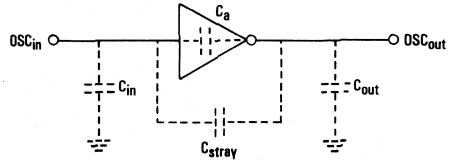
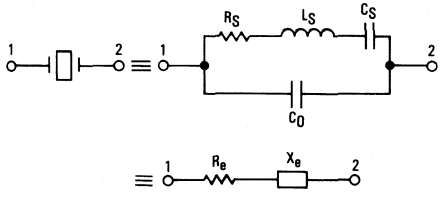


Figure 18. Parasitic Capacitances of the Amplifier and C_{stray}



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 19. Equivalent Crystal Networks

The oscillator can be "trimmed" on-frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes zero in the above expression for C_L.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 19. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 17 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of supply voltage at REF_{out}. (OSC_{out} is not used because loading impacts the oscillator.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. See Table 2.

RECOMMENDED READING

Technical Note TN-24, Statek Corp.

Technical Note TN-7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit—Definitions and Method of Measurement", *Proc. IEEE*, Vol. 57, No. 2, February 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro-Technology*, June 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May 1966.

D. Babin, "Designing Crystal Oscillators", *Machine Design*, March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", *Machine Design*, April 25, 1985.

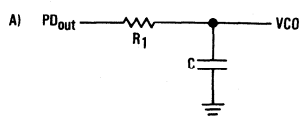
Table 2. Partial List of Crystal Manufacturers

Name	Address	Phone
United States Crystal Corp.	3605 McCart Ave., Ft. Worth, TX 76110	(817) 921-3013
Crystek Crystal	2371 Crystal Dr., Ft. Myers, FL 33907	(813) 936-2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639-7810

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

PHASE-LOCKED LOOP—LOW PASS FILTER DESIGN

A)

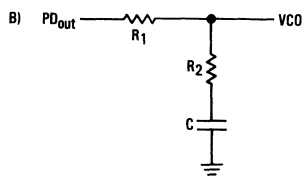


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1sC + 1}$$

B)

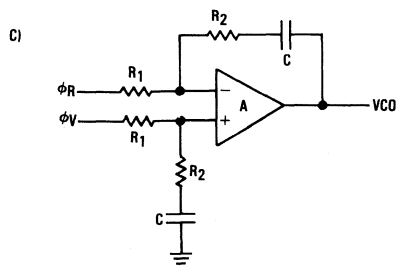


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\ \omega_n \left(R_2C + \frac{N}{K_\phi K_{VCO}}\right)$$

$$F(s) = \frac{R_2sC + 1}{(R_1 + R_2)sC + 1}$$

C)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2sC + 1}{R_1sC}$$

NOTE:

For C), R_1 is frequently split into two series resistors each $R_1 \div 2$. A capacitor C_C is then placed from the midpoint to ground to further filter the error pulses. The value of C_C should be such that the corner frequency of this network does not significantly effect ω_n.

DEFINITIONS:

N = Total Division Ratio in Feedback Loop

K_ϕ (Phase Detector Gain) = $V_{DD}/4\pi$ volts/radian for PD_{out}

K_ϕ (Phase Detector Gain) = $V_{DD}/2\pi$ volts/radian for ϕ_V and ϕ_R

K_{VCO} (VCO Gain) = $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$

For a nominal design starting point, the user might consider a damping factor $\zeta \approx 0.7$ and a natural loop frequency $\omega_n \approx (2\pi f_R/50)$ where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R-related VCO sidebands.

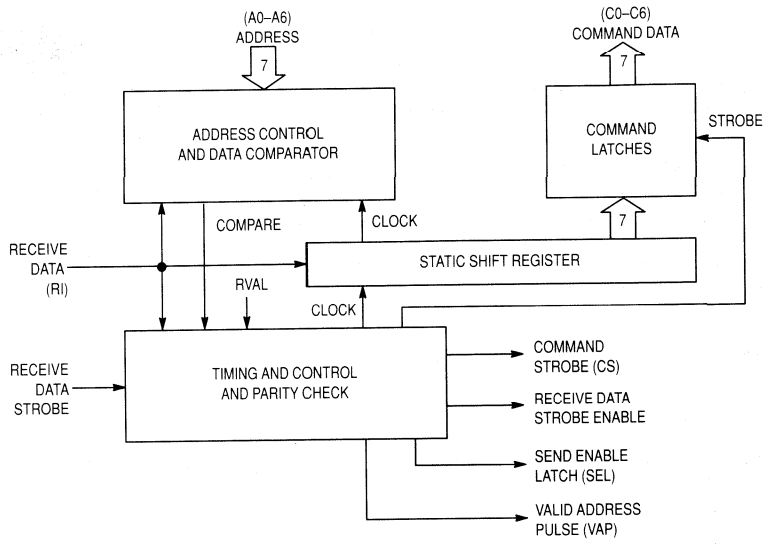
RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition)*. New York, Wiley-Interscience, 1979.
Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition)*. New York, Wiley-Interscience, 1980.
Blanchard, Alain, *Phase-Locked Loops: Application to Coherent Receiver Design*, New York, Wiley-Interscience, 1976.
Egan, William F., *Frequency Synthesis by Phase Lock*. New York, Wiley-Interscience, 1981.
Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design*. Englewood Cliffs, NJ, Prentice-Hall, 1983.
Berlin, Howard M., *Design of Phase-Locked Loop Circuits, with Experiments*. Indianapolis, Howard W. Sams and Co., 1978.
Kinley, Harold, *The PLL Synthesizer Cookbook*. Blue Ridge Summit, PA, Tab Books, 1980.
Seidman, Arthur H., *Integrated Circuits Applications Handbook*, Chapter 17, pp. 538-586. New York, John Wiley & Sons.
Fadrhons, Jan, "Design and Analyze PLLs on a Programmable Calculator" *EDN*. March 5, 1980.
AN535, Phase-Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.
AR254, Phase-Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design*, 1987.
BR504/D, Electronic Tuning Address Systems, Motorola Semiconductor Products, Inc., 1986.

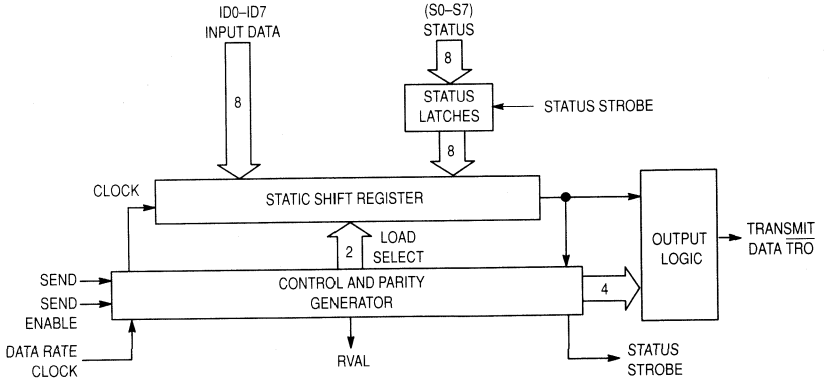
Remote Control Functions

BLOCK DIAGRAM

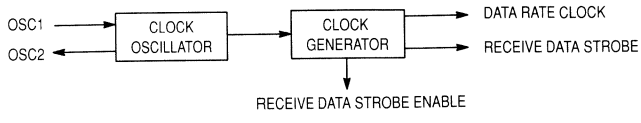
RECEIVE



TRANSMIT



CLOCKS



MAXIMUM RATINGS (Voltages referenced to V_{SS})

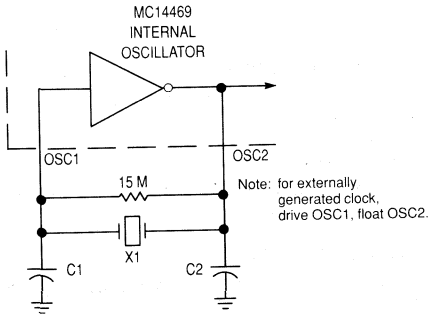
Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	V
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD}+0.5	V
DC Current Drain per Pin	I	10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} V	−40°C Min	−40°C Max	25°C Min	25°C Max	+85°C Min	+85°C Max	Unit
Output Voltage "0" Level	V_{OL}								V
V_{in} = V_{DD} or 0		5.0	—	0.05	—	0.05	—	0.05	
		10	—	0.05	—	0.05	—	0.05	
		15	—	0.05	—	0.05	—	0.05	
"1" Level	V_{OH}								V
V_{in} = 0 or V_{DD}		5.0	4.95	—	4.95	—	4.95	—	
		10	9.95	—	9.95	—	9.95	—	
		15	14.95	—	14.95	—	14.95	—	
Input Voltage (Except OSC1) "0" Level	V_{IL}								V
(V_O = 4.5 or 0.5 V)		5.0	—	1.5	—	1.5	—	1.5	
(V_O = 9.0 or 1.0 V)		10	—	3.0	—	3.0	—	3.0	
(V_O = 13.5 or 1.5 V)		15	—	4.0	—	4.0	—	4.0	
"1" Level	V_{IH}								V
(V_O = 0.5 or 4.5 V)		5.0	3.5	—	3.5	—	3.5	—	
(V_O = 1.0 or 9.0 V)		10	7.0	—	7.0	—	7.0	—	
(V_O = 1.5 or 13.5 V)		15	11	—	11	—	11	—	
Output Drive Current (Except OSC2)	I_{OH}								mA
(V_{OH} = 2.5 V) Source		5.0	−1.0	—	−0.8	—	−0.6	—	
(V_{OH} = 4.6 V)		5.0	−0.2	—	−0.16	—	−0.12	—	
(V_{OH} = 9.5 V)		10	−0.5	—	−0.4	—	−0.3	—	
(V_{OH} = 13.5 V)		15	−1.4	—	−1.2	—	−1.0	—	
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	0.52	—	0.44	—	0.36	—	mA
(V_{OL} = 0.5 V)		10	1.3	—	1.1	—	0.9	—	
(V_{OL} = 1.5 V)		15	3.6	—	3.0	—	2.4	—	
Output Drive Current (OSC2 Only)	I_{OH}								mA
(V_{OH} = 2.5 V) Source		5.0	−0.19	—	−0.16	—	−0.13	—	
(V_{OH} = 4.6 V)		5.0	−0.04	—	−0.035	—	−0.03	—	
(V_{OH} = 9.5 V)		10	−0.09	—	−0.08	—	−0.06	—	
(V_{OH} = 13.5 V)		15	−0.29	—	−0.27	—	−0.2	—	
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	0.1	—	0.085	—	0.07	—	mA
(V_{OL} = 0.5 V)		10	0.17	—	0.14	—	0.1	—	
(V_{OL} = 1.5 V)		15	0.5	—	0.42	—	0.3	—	
OSC Frequency	f_{OSC}	4.5	0	400	0	365	0	310	kHz
		12	0	800	0	730	0	620	
Input Current	I_{in}	15	—	±0.3	—	±0.3	—	±1.0	µA
Pull-Up Current (A0–A6, ID0–ID7)	I_{UP}	15	12	120	10	100	8.0	85	µA
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	75	—	75	—	565	µA
		10	—	150	—	150	—	1125	
		15	—	300	—	300	—	2250	
Supply Voltage	V_{DD}	—	+4.5	+18	+4.5	+18	+4.5	+18	V



X1 = Ceramic Resonator: 307.2 kHz ± 1 kHz for 4800 baud rate.
C1 and C2 are sized per the ceramic resonator supplier's recommendation.

Ceramic Resonator Suppliers:*
1. Morgan Matroc, Inc., Bedford, OH, 216/232-8600
2. Radio Materials Co., Attica, IN, 317/762-2491

* Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of ceramic resonator suppliers.

Figure 1. Oscillator Circuit

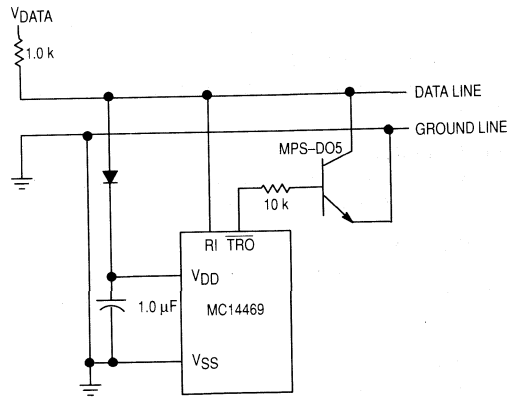


Figure 2. Rectified Power from Data Lines Circuit

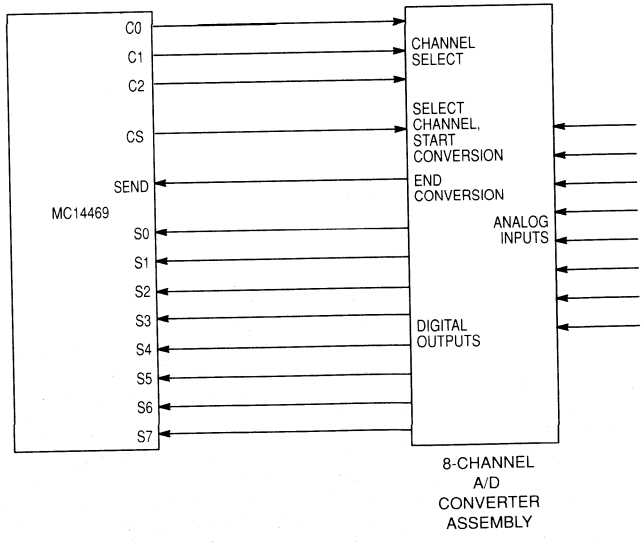


Figure 3. A-D Converter Interface

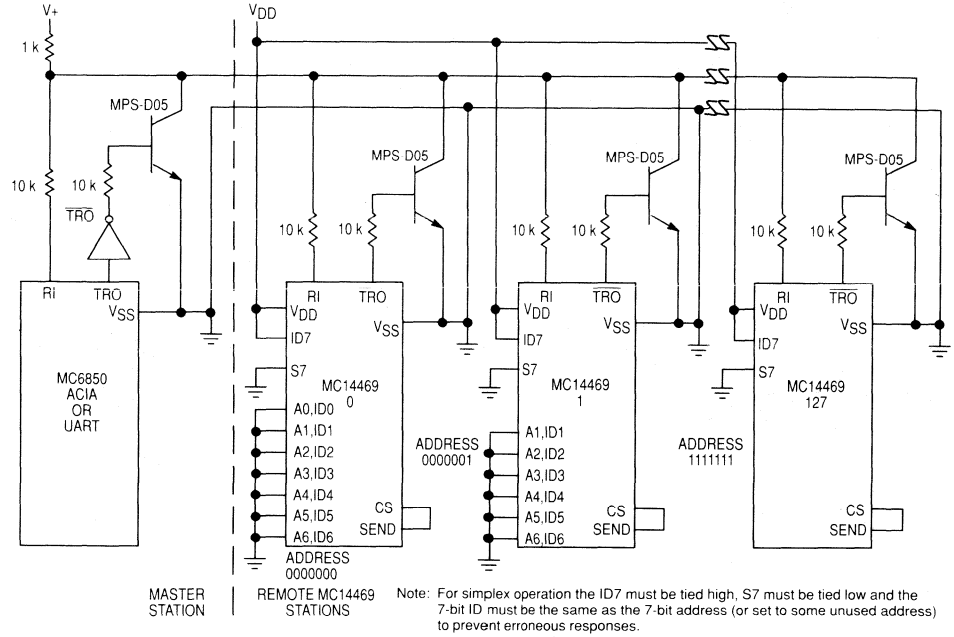


Figure 4. Single Line, Simplex Data Transmission

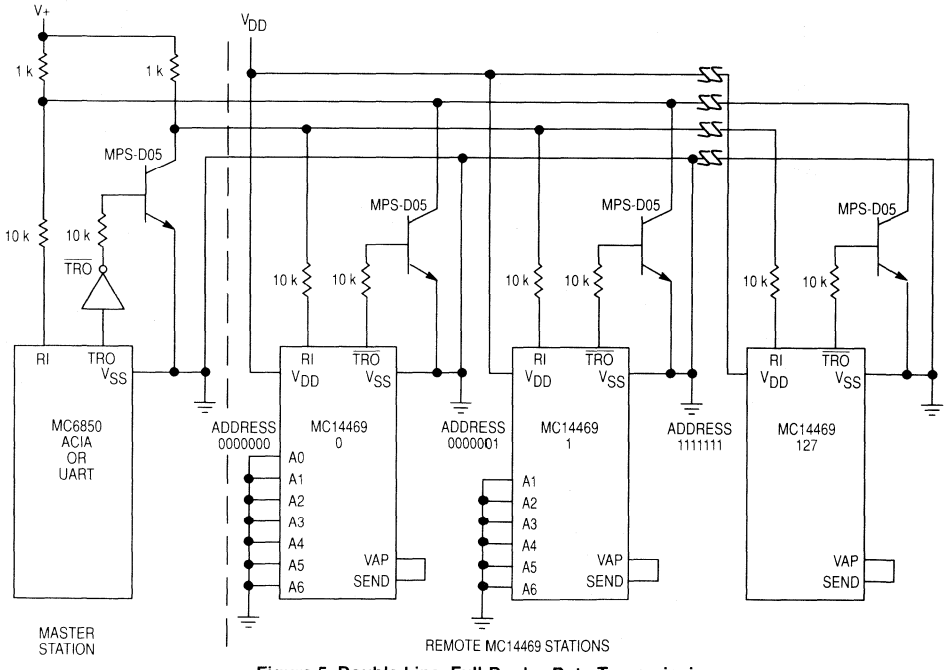


Figure 5. Double Line, Full Duplex Data Transmission

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +15	V
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD}+0.5	V
DC Input Current per Pin	I_{in}	±10	mA
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C; all Voltages Referenced to V_{SS})

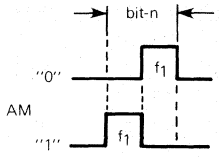
Characteristic		Symbol	Pin	V_{DD}	Min	Max	Unit
Supply Voltage		V_{DD}	18	–	4.0	10.0	V
Supply Current		I_{DD}	18				
Idle				10	–	50	μA
Operation				10	–	5	mA
Output Current – Signal			8				μA
V_{OH} = 3.0 V	Source	I_{OH}		4	−900	–	
V_{OL} = 0.5 V	Sink	I_{OL}		4	120	–	
Output Current – Scanner			4, 5				μA
V_{OH} = 3.0 V	Source	I_{OH}	6, 7	4	−30	–	
V_{OL} = 0.5 V	Sink	I_{OL}		4	245	–	
Output Current – Oscillator			13				μA
V_{OH} = 3.0 V	Source	I_{OH}		4	−300	–	
V_{OL} = 0.5 V	Sink	I_{OL}		4	245	–	
Input Current – Oscillator		I_{in}	12				μA
Operation				10	±2	±80	
Idle, V_{IL} = 0.5 V				4	30	–	
Input Current – Decoder		I_{in}	1, 2, 3, 10				μA
V_{IH} = 9 V			11, 14, 15	10	−15	–	
V_{IL} = 0.5 V			16, 17	4	–	−60	
Input Voltage – Decoder			1, 2, 3, 10				V
		V_{IH}	11, 14, 15	10	9	–	
		V_{IL}	16, 17	10	–	1.2	
		V_{IH}		4	3	–	
		V_{IL}		4	–	1.0	

CIRCUIT OPERATION

The transmitter sends a 6-bit, labelled A (LSB) to F (MSB), binary code giving a total of 64 possible combinations or code words. All of these channels are user selectable, except the last two - where channel 63 is not sent while channel 62 is automatically sent by the transmitter at the end of each transmission as an "End of Transmission" code.

In either mode, FSK or AM, the transmitted signal is in the form of a biphase pulse code modulation (PCM) signal. The AM coding is shown in Figure 2.

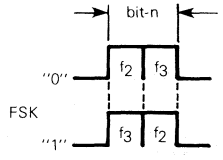
FIGURE 2 — AM CODING



In the AM mode, f_1 is a train of pulses at the modulating frequency of 31.25 kHz for a reference frequency of 500 kHz.

In the FSK mode, two modulating frequencies are used as shown in Figure 3.

FIGURE 3 — FSK CODING



In this mode, f_3 is 50 kHz and f_2 is 41.66 kHz for a reference frequency of 500 kHz.

The keyboard can be a simple switch matrix using no external diodes, connected to the four scanner outputs, A1 to A4, and the eight row inputs, E1 to E8. Under these conditions, only the first 32 code words are available since bit-F is always at logical "0". However, a simple two-pole changeover switch, in the manner of a typewriter "shift" key (switch FK3 in figure 1) can be used to change the polarity of bit-F to give access to the next full set of 32 instructions.

An alternative method of accessing more than 32 instructions is by the use of external diodes between the address inputs (see Figure 4). These have the effect of producing "phantom" address inputs by pulling two inputs low at the same time, which causes bit-F to go high, that is to logical "1". By interconnecting only certain address inputs it is possible to make an intermediate keyboard with between 32 and 64 keys.

The other two switches in Figure 1, FK1 and FK2, change the modulation mode. Closing FK1 changes the modulation from FSK to AM and the start-bit polarity. Closing FK2 changes the start-bit to a logical "0".

The full range of options available is illustrated in the table below:

	Start-bit	Modulation	Bit-F	Channels
E9 = Open	1	FSK	0	0-31
E9 = A1 (FK1)	1	AM	0	0-31
E9 = A2 (FK2)	0	FSK	0	0-31*
E9 = A3 (FK3)	1	FSK	1	32-61
E9 = A1•A2	0	AM	0	0-31
E9 = A1•A3	1	AM	1	32-61
E9 = A2•A3	0	FSK	1	32-61*
E9 = A1•A2•A3	0	AM	1	32-61

*Not allowed.

One of the transmitter's major features is its low power consumption - in the order of 10 μA in the idle state. For this reason the battery is perpetually in circuit. It has in fact been found that a light discharge current is beneficial to battery life.

In its active state, the transmitter efficiency is increased by the use of a low duty cycle which is less than 2.5% for the modulating pulse trains.

While no key is pressed, the circuit is in its idle state and the reference oscillator is stopped. Also, the eight address input lines are held high through internal pull-up resistors.

As soon as a key is pressed, this takes the appropriate address line low, signalling to the circuit that a key has been selected. The oscillator is now enabled. If the key is released *before the code word has been sent, the circuit returns to its* idle state. To account for accidental activation of the transmitter, the circuit has a built-in reaction time of ~20 ms, which also overcomes contact bounce. After this delay the code word will be sent and repeated at 90 ms intervals for as long as the key is pressed. As soon as the key is released, the circuit automatically sends channel 62, the "End of Transmission" (EOT) code. The transmitter then returns to its idle state.

The differences between the two modulation modes are illustrated in figure 5. However, it should be noted that in the AM mode, each transmitted word is preceded by a burst of pulses lasting 512 μs. This is used to set up the AGC loop in the receiver's preamp. In the FSK mode, the first frequency of the first bit is extended by 1.5 ms and the AGC burst is suppressed. In either mode it is assumed that the normal start-bit is present.

TABLE 1 — TRANSMITTED CODES

Channel	Code Word F	E	D	C	B	A	Keyboard In	Out
0	0	0	0	0	0	0	E8	A4
1				0	0	1	E1	A4
2				0	1	0	E2	A4
3				0	1	1	E3	A4
4				1	0	0	E4	A4
5				1	0	1	E5	A4
6				1	1	0	E6	A4
7				1	1	1	E7	A4
8	0	0	1	0	0	0	E8	A1
9				0	0	1	E1	A1
10				0	1	0	E2	A1
11				0	1	1	E3	A1
12				1	0	0	E4	A1
13				1	0	1	E5	A1
14				1	1	0	E6	A1
15				1	1	1	E7	A1
16	0	1	0	0	0	0	E8	A3
17				0	0	1	E1	A3
18				0	1	0	E2	A3
19				0	1	1	E3	A3
20				1	0	0	E4	A3
21				1	0	1	E5	A3
22				1	1	0	E6	A3
23				1	1	1	E7	A3
24	0	1	1	0	0	0	E8	A2
25				0	0	1	E1	A2
26				0	1	0	E2	A2
27				0	1	1	E3	A2
28				1	0	0	E4	A2
29				1	0	1	E5	A2
30				1	1	0	E6	A2
31	0	1	1	1	1	1	E7	A2
32	1	0	0	0	0	0	E8a	A4
33				0	0	1	E1a	A4
34				0	1	0	E2a	A4
35				0	1	1	E3a	A4
36				1	0	0	E4a	A4
37				1	0	1	E5a	A4
38				1	1	0	E6a	A4
39				1	1	1	E7a	A4
40	1	0	1	0	0	0	E8a	A1
41				0	0	1	E1a	A1
42				0	1	0	E2a	A1
43				0	1	1	E3a	A1
44				1	0	0	E4a	A1
45				1	0	1	E5a	A1
46				1	1	0	E6a	A1
47				1	1	1	E7a	A1
48	1	1	0	0	0	0	E8a	A3
49				0	0	1	E1a	A3
50				0	1	0	E2a	A3
51				0	1	1	E3a	A3
52				1	0	0	E4a	A3
53				1	0	1	E5a	A3
54				1	1	0	E6a	A3
55				1	1	1	E7a	A3
56	1	1	1	0	0	0	E8a	A2
57				0	0	1	E1a	A2
58				0	1	0	E2a	A2
59				0	1	1	E3a	A2
60				1	0	0	E4a	A2
61				1	0	1	E5a	A2
62 (EOT)				1	1	0	E6a	A2
Not transmitted	1	1	1	1	1	1	E7a	A2

NOTE: Although the "a" suffix applies to a phantom input when using a keyboard with up to 64 keys, the coding is identical with a 32 key keyboard when switch FK3 is closed.

MC145026
MC145027
MC145028
SC41342
SC41343
SC41344

Encoder and Decoder Pairs
CMOS

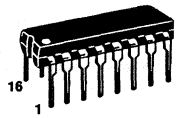
These devices are designed to be used as encoder/decoder pairs in remote control applications.

The MC145026 encodes nine lines of information and serially sends this information upon receipt of a transmit enable ($\overline{TE}$) signal. The nine lines may be encoded with trinary data (low, high, or open) or binary data (low or high). The words are transmitted twice per encoding sequence to increase security.

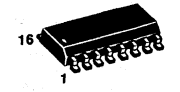
The MC145027 decoder receives the serial stream and interpets five of the trinary digits as an address code. Thus, 243 addresses are possible. If binary data is used at the encoder, 32 addresses are possible. The remaining serial information is interpeted as four bits of binary data. The valid transmission output (VT) goes high on the MC145027 when two conditions are met. First, two addresses must be consecutively received (in one encoding sequence) which both match the local address. Second, the 4-bits of data must match the last valid data received. The active VT indicates that the information at the data output pins has been updated.

The MC145028 decoder treats all nine trinary digits as an address which allows 19,683 codes. If binary data is encoded, 512 codes are possible. The valid transmission output (VT) goes high on the MC145028 when two addresses are consecutively received (in one encoding sequence) which both match the local address.

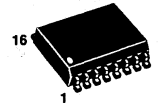
- Operating Temperature Range: –40° to 85°C
- Very-Low Standby Current for the Encoder: 300 nA Maximum @ 25°C
- Interfaces with RF, Ultrasonic, or Infrared Modulators and Demodulators
- RC Oscillator, No Crystal Required
- High External Component Tolerance; Can Use ±5% Components
- Internal Power-On Reset Forces All Decoder Outputs Low
- For Infrared Applications, See Applications Note AN1016
- Operating Voltage Range: 4.5 to 18 V
- Low-Voltage Versions Available —
  SC41342: 2.5 to 18 V Version of the MC145026
  SC41343: 2.8 to 10 V Version of the MC145027
  SC41344: 2.8 to 10 V Version of the MC145028



P SUFFIX
PLASTIC DIP
CASE 648



D SUFFIX
SOG
CASE 751B

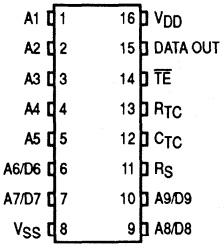


DW SUFFIX
SOG
CASE 751G

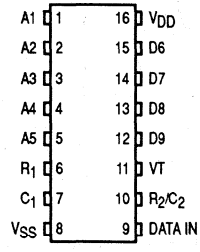
ORDERING INFORMATION

MC145026P, SC41342P	Plastic DIP
MC145026D, SC41342D	SOG Package
MC145027P, SC41343P	Plastic DIP
MC145027DW, SC41343DW	SOG Package
MC145028P, SC41344P	Plastic DIP
MC145028DW, SC41344DW	SOG Package

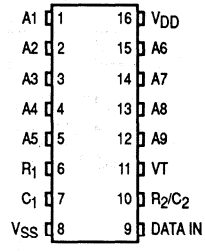
PIN ASSIGNMENTS



MC145026
SC41342
ENCODERS



MC145027
SC41343
DECODERS



MC145028
SC41344
DECODERS

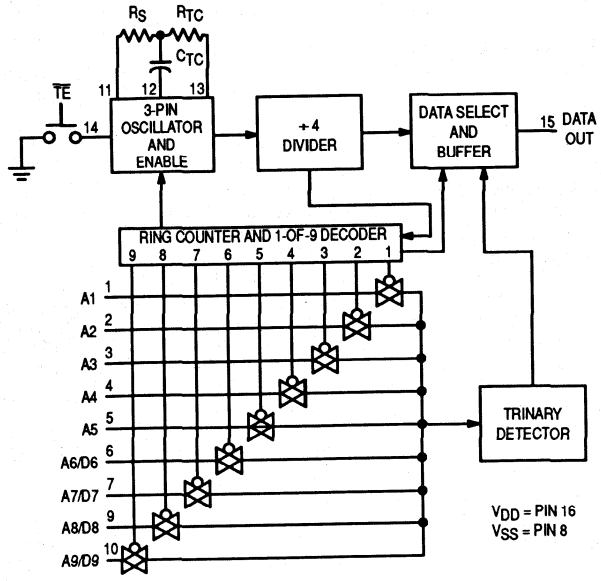


Figure 1. MC145026 Encoder Block Diagram

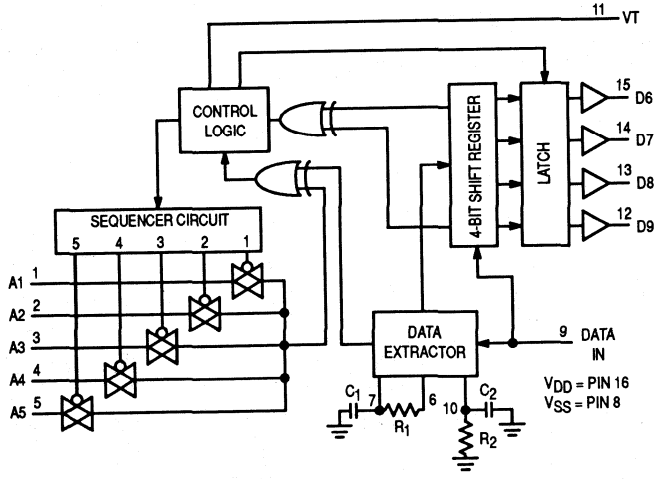


Figure 2. MC145027 Decoder Block Diagram

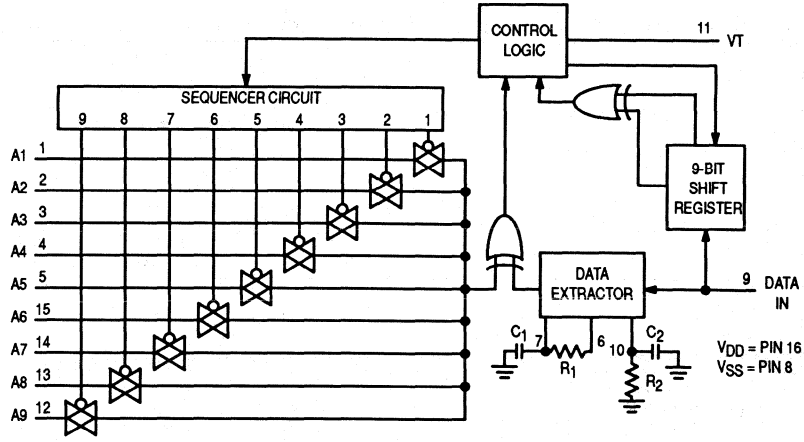


Figure 3. MC145028 Decoder Block Diagram

MAXIMUM RATINGS* (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage (except SC41343, SC41344)	–0.5 to +18	V
V_{DD}	DC Supply Voltage (SC41343, SC41344 only)	–0.5 to +10	V
V_{in}	DC Input Voltage	–0.5 to V_{DD}+0.5	V
V_{out}	DC Output Voltage	–0.5 to V_{DD}+0.5	V
I_{in}	DC Input Current, per Pin	±10	mA
I_{out}	DC Output Current, per Pin	±10	mA
P_D	Power Dissipation, per Package	500	mW
T_{stg}	Storage Temperature	–65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

ELECTRICAL CHARACTERISTICS — MC145026, MC145027, MC145028, and SC41342* (Voltage Referenced to V_{SS})

Symbol	Characteristic	V_{DD} V	Guaranteed Limit						Unit
			−40°C		25°C		+85°C		
			Min	Max	Min	Max	Min	Max	
V_{OL}	Low-Level Output Voltage (V_{in} = V_{DD} or 0)	5.0	—	0.05	—	0.05	—	0.05	V
		10	—	0.05	—	0.05	—	0.05	
		15	—	0.05	—	0.05	—	0.05	
V_{OH}	High-Level Output Voltage (V_{in} = 0 or V_{DD})	5.0	4.95	—	4.95	—	4.95	—	V
		10	9.95	—	9.95	—	9.95	—	
		15	14.95	—	14.95	—	14.95	—	
V_{IL}	Low-Level Input Voltage								V
	(V_{out} = 4.5 or 0.5 V)	5.0	—	1.5	—	1.5	—	1.5	
	(V_{out} = 9.0 or 1.0 V)	10	—	3.0	—	3.0	—	3.0	
	(V_{out} = 13.5 or 1.5 V)	15	—	4.0	—	4.0	—	4.0	
V_{IH}	High-Level Input Voltage								V
	(V_{out} = 0.5 or 4.5 V)	5.0	3.5	—	3.5	—	3.5	—	
	(V_{out} = 1.0 or 9.0 V)	10	7.0	—	7.0	—	7.0	—	
	(V_{out} = 1.5 or 13.5 V)	15	11	—	11	—	11	—	
I_{OH}	High-Level Output Current								mA
	(V_{out} = 2.5 V)	5.0	−2.5	—	−2.1	—	−1.7	—	
	(V_{out} = 4.6 V)	5.0	−0.52	—	−0.44	—	−0.36	—	
	(V_{out} = 9.5 V)	10	−1.3	—	−1.1	—	−0.9	—	
	(V_{out} = 13.5 V)	15	−3.6	—	−3.0	—	−2.4	—	
I_{OL}	Low-Level Output Current								mA
	(V_{out} = 0.4 V)	5.0	0.52	—	0.44	—	0.36	—	
	(V_{out} = 0.5 V)	10	1.3	—	1.1	—	0.9	—	
	(V_{out} = 1.5 V)	15	3.6	—	3.0	—	2.4	—	
I_{in}	Input Current — $\overline{TE}$	5.0	—	—	3.0	11	—	—	µA
	(MC145026 and SC41342, Pullup Device)	10	—	—	16	60	—	—	
		15	—	—	35	120	—	—	
I_{in}	Input Current R_S (MC145026 and SC41342), Data In (MC145027, MC145028)	15	—	±0.3	—	±0.3	—	±1.0	µA
I_{in}	Input Current								µA
	A1-A5, A6/D6–A9/D9 (MC145026 and SC41342),	5.0	—	—	—	±110	—	—	
	A1-A5 (MC145027),	10	—	—	—	±500	—	—	
	A1-A9 (MC145028)	15	—	—	—	+1000	—	—	
C_{in}	Input Capacitance (V_{in} = 0)	—	—	—	—	7.5	—	—	pF
I_{DD}	Quiescent Current — MC145026 and SC41342	5.0	—	—	—	0.1	—	—	µA
		10	—	—	—	0.2	—	—	
		15	—	—	—	0.3	—	—	
I_{DD}	Quiescent Current — MC145027, MC145028	5.0	—	—	—	50	—	—	µA
		10	—	—	—	100	—	—	
		15	—	—	—	150	—	—	
I_{dd}	Dynamic Supply Current — MC145026 and SC41342	5.0	—	—	—	200	—	—	µA
	(f_C = 20 kHz)	10	—	—	—	400	—	—	
		15	—	—	—	600	—	—	
I_{dd}	Dynamic Supply Current — MC145027, MC145028	5.0	—	—	—	400	—	—	µA
	(f_C = 20 kHz)	10	—	—	—	800	—	—	
		15	—	—	—	1200	—	—	

*Also see next Electrical Characteristics table for 2.5 V specifications.

ELECTRICAL CHARACTERISTICS — SC41342 (Voltage Referenced to V_{SS})

Symbol	Characteristic	V_{DD} V	Guaranteed Limit						Unit
			−40°C		25°C		+85°C		
			Min	Max	Min	Max	Min	Max	
V_{OL}	Low-Level Output Voltage (V_{in} = 0 V or V_{DD})	2.5	—	0.05	—	0.05	—	0.05	V
V_{OH}	High-Level Output Voltage (V_{in} = 0 V or V_{DD})	2.5	2.45	—	2.45	—	2.45	—	V
V_{IL}	Low-Level Input Voltage (V_{out} = 0.5 V or 2.0 V)	2.5	—	0.3	—	0.3	—	0.3	V
V_{IH}	High-Level Input Voltage (V_{out} = 0.5 V or 2.0 V)	2.5	2.2	—	2.2	—	2.2	—	V
I_{OH}	High-Level Output Current (V_{out} = 1.25 V)	2.5	0.28	—	0.25	—	0.2	—	mA
I_{OL}	Low-Level Output Current (V_{out} = 0.4 V)	2.5	0.22	—	0.2	—	0.16	—	mA
I_{in}	Input Current ($\overline{TE}$ — Pullup Device)	2.5	—	—	0.09	1.8	—	—	µA
I_{in}	Input Current (A1-A5, A6/D6-A9/D9)	2.5	—	—	—	±25	—	—	µA
I_{DD}	Quiescent Current	2.5	—	—	—	0.05	—	—	µA
I_{dd}	Dynamic Supply Current (f_c = 20 kHz)	2.5	—	—	—	40	—	—	µA

ELECTRICAL CHARACTERISTICS — SC41343 and SC41344 (Voltage Referenced to V_{SS})

Symbol	Characteristic	V_{DD} V	Guaranteed Limit						Unit
			−40°C		25°C		+85°C		
			Min	Max	Min	Max	Min	Max	
V_{OL}	Low-Level Output Voltage (V_{in} = 0 V or V_{DD})	2.8	—	0.05	—	0.05	—	0.05	V
		5.0	—	0.05	—	0.05	—	0.05	
		10	—	0.05	—	0.05	—	0.05	
V_{OH}	High-Level Output Voltage (V_{in} = 0 V or V_{DD})	2.8	2.75	—	2.75	—	2.75	—	V
		5.0	4.95	—	4.95	—	4.95	—	
		10	9.95	—	9.95	—	9.95	—	
V_{IL}	Low-Level Input Voltage								V
	(V_{out} = 2.3 V or 0.5 V)	2.8	—	0.84	—	0.84	—	0.84	
	(V_{out} = 4.5 V or 0.5 V)	5.0	—	1.5	—	1.5	—	1.5	
	(V_{out} = 9.0 V or 1.0 V)	10	—	3.0	—	3.0	—	3.0	
V_{IH}	High-Level Input Voltage								V
	(V_{out} = 0.5 V or 2.3 V)	2.8	1.96	—	1.96	—	1.96	—	
	(V_{out} = 0.5 V or 4.5 V)	5.0	3.5	—	3.5	—	3.5	—	
	(V_{out} = 1.0 V or 9.0 V)	10	7.0	—	7.0	—	7.0	—	
I_{OH}	High-Level Output Current								mA
	(V_{out} = 1.4 V)	2.8	−0.73	—	−0.7	—	−0.55	—	
	(V_{out} = 4.5 V)	5.0	−0.59	—	−0.5	—	−0.41	—	
	(V_{out} = 9.0 V)	10	−1.3	—	−1.1	—	−0.9	—	
I_{OL}	Low-Level Output Current								mA
	(V_{out} = 0.4 V)	2.8	0.35	—	0.3	—	0.24	—	
	(V_{out} = 0.5 V)	5.0	0.8	—	0.6	—	0.4	—	
	(V_{out} = 1.0 V)	10	3.5	—	2.9	—	2.3	—	
I_{in}	Input Current — Data In	10	—	±0.3	—	±0.3	—	±1.0	µA
I_{in}	Input Current	2.8	—	—	—	±30	—	—	µA
	A1-A5 (SC41343),	5.0	—	—	—	±140	—	—	
	A1-A9 (SC41344)	10	—	—	—	±600	—	—	
C_{in}	Input Capacitance (V_{in} = 0)	—	—	—	—	7.5	—	—	pF
I_{DD}	Quiescent Current	2.8	—	—	—	60	—	—	µA
		5.0	—	—	—	75	—	—	
		10	—	—	—	150	—	—	
I_{dd}	Dynamic Supply Current	2.8	—	—	—	300	—	—	µA
	(f_C = 20 kHz)	5.0	—	—	—	500	—	—	
		10	—	—	—	1000	—	—	

SWITCHING CHARACTERISTICS — MC145026, MC145027, MC145028, and SC41342* (C_L = 50 pF, T_A = 25°C)

Symbol	Characteristic	V_{DD}	Guaranteed Limit		Unit
			Min	Max	
t_{TLH}, t_{THL}	Output Transition Time (Figures 4 and 8)	5.0 10 15	— — —	200 100 80	ns
t_r	Data In Rise Time (Decoders) (Figure 5)	5.0 10 15	— — —	15 15 15	µs
t_f	Data In Fall Time (Decoders) (Figure 5)	5.0 10 15	— — —	15 5.0 4.0	µs
f_{osc}	Encoder Clock Frequency (Figure 6)	5.0 10 15	0.001 0.001 0.001	2.0 5.0 10	MHz
f	Decoder Frequency (Referenced to Encoder Clock) (Figure 14)	5.0 10 15	1.0 1.0 1.0	240 410 450	kHz
t_w	$\overline{TE}$ Pulse Width (Encoders) (Figure 7)	5.0 10 15	65 30 20	— — —	ns

*Also see next Switching Characteristics table for 2.5 V specifications.

SWITCHING CHARACTERISTICS — SC41342 (C_L = 50 pF, T_A = 25°C)

Symbol	Characteristic	V_{DD}	Guaranteed Limit		Unit
			Min	Max	
t_{TLH}, t_{THL}	Output Transition Time (Figures 4 and 8)	2.5	—	450	ns
f_{osc}	Encoder Clock Frequency (Figure 6)	2.5	1.0	250	kHz
t_w	$\overline{TE}$ Pulse Width (Figure 7)	2.5	—	—	ns

SWITCHING CHARACTERISTICS — SC41343 and SC41344 (C_L = 50 pF, T_A = 25°C)

Symbol	Characteristic	V_{DD}	Guaranteed Limit		Unit
			Min	Max	
t_{TLH}, t_{THL}	Output Transition Time (Figures 4 and 8)	2.8 5.0 10	— — —	320 200 100	ns
t_r	Data In Rise Time (Figure 5)	2.8 5.0 10	— — —	15 15 15	µs
t_f	Data In Fall Time (Figure 5)	2.8 5.0 10	— — —	15 15 5.0	µs
f	Decoder Frequency (Referenced to Encoder Clock) (Figure 14)	2.8 5.0 10	1.0 1.0 1.0	100 240 410	kHz

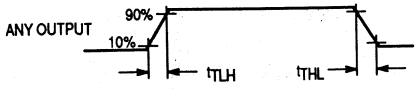


Figure 4.

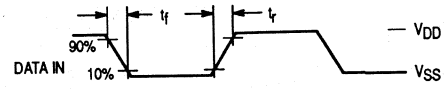


Figure 5.

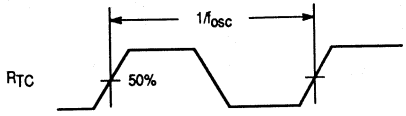


Figure 6.

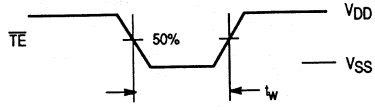
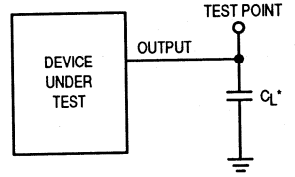


Figure 7.



*INCLUDES ALL PROBE AND JIG CAPACITANCE.

Figure 8. Test Circuit

OPERATING CHARACTERISTICS

MC145026

The encoder serially transmits trinary data as defined by the state of the A1 through A5 and A6/D6 through A9/D9 input pins. These pins may be in either of three states (low, high, or open) allowing 19,683 possible codes. The transmit sequence is initiated by a low level on the $\overline{TE}$ input pin. Each time the $\overline{TE}$ input is forced low, the encoder outputs two identical data words. Between the two data words, no signal is sent for three data periods. If the $\overline{TE}$ input is kept low, the encoder continuously transmits the data word. See Figure 10.

Each transmitted trinary digit is encoded into pulses (See Figure 11). A logic zero (low) is encoded as two consecutive short pulses, a logic one (high) as two consecutive long pulses, and an open (high-impedance) as a long pulse followed by a short pulse. The input state is determined by using a weak "output" device to try to force each input first low, then high. If only a high state results from the two tests, the input is assumed to be hardwired to V_{DD}. If only a low state is obtained, the input is assumed to be hardwired to V_{SS}. If both a high and a low can be forced at an input, an open is assumed and is encoded as such. The "high" and "low" levels are 70% and 30% of the supply voltage as shown in the Electrical Characteristics Table. The weak "output" device sinks/sources up to 110 μA at a 5 V supply level, 500 μA at 10 V, and 1 mA at 15 V.

The $\overline{TE}$ input has an internal pullup device so that a simple switch may be used to force the input low. While $\overline{TE}$ is high, the encoder is completely disabled, the oscillator is inhibited, and the current drain is reduced to quiescent current. When $\overline{TE}$ is brought low, the oscillator is started, and the transmit sequence begins. The inputs are then sequentially selected, and determinations are made as to the input logic states. This information is serially transmitted via the Data Out pin.

MC145027

This decoder receives the serial data from the encoder and outputs the data, if it is valid. The transmitted data, consisting of two identical words, is examined bit by bit during reception. The first five trinary digits are assumed to be the address. If the received address matches the local address, next four (data) bits are internally stored, but are not transferred to the output data latch. As the second encoded word is received, the address must again match. If a match occurs, the new data bits are checked against the previously stored data bits. If the two nibbles of data (four bits each) match, the data is transferred to the output data latch by VT and remains until new data replaces it. At the same time, the VT output pin is brought high and remains high until an error is received or until no input signal is received for four data periods. See Figure 10.

Although the address information may be encoded in trinary, the data information must be either a one or a zero. A trinary (open) data line is decoded as a logic one.

MC145028

This decoder operates in the same manner as the MC145027 except that nine address lines are used and no data output is available. The VT output is used to indicate that a valid address has been received. For transmission security, two identical transmitted words must be consecutively received before a valid transmission output (VT) signal is issued.

The MC145028 allows 19,683 addresses when trinary levels are used. 512 addresses are possible when binary levels are used.

PIN DESCRIPTIONS

MC145026 ENCODER

A1 through A5, A6/D6 through A9/D9 (Pins 1 through 7, 9, and 10)

These address/data inputs are encoded and the data is sent serially from the encoder via the data out pin.

R_S, C_{TC}, R_{TC} (Pins 11, 12, and 13)

These pins are part of the oscillator section of the encoder. See Figure 9.

If an external signal source is used instead of the internal oscillator, it should be connected to the R_S input and the R_{TC} and C_{TC} pins should be left open.

$\overline{TE}$ (Pin 14)

This active-low transmit enable input initiates transmission when forced low. An internal pullup device keeps this input normally high. The pullup current is specified in the Electrical Characteristics table.

Data Out (Pin 15)

This is the output of the encoder that serially presents the encoded data word.

V_{SS} (Pin 8)

The most-negative supply potential. This pin is usually ground.

V_{DD} (Pin 16)

The most-positive power supply pin.

MC145027 AND MC145028 DECODERS

A1 through A5 (Pins 1 through 5) — MC145027
A1 through A9 (Pins 1 through 5, 15, 14, 13, and 12) — MC145028

These are the local address inputs. The states of these pins must match the appropriate encoder inputs for the VT pin to go high. The local address may be encoded with trinary or binary data.

D6 through D9 (Pins 15, 14, 13, and 12) – MC145027 ONLY

These outputs present the binary information that is on encoder inputs A6/D6 through A9/D9. Only binary data is acknowledged; a trinary open at the MC145026 encoder is decoded as a high level (logic 1).

R_1, C_1 (Pins 6, 7)

As shown in Figures 2 and 3, these pins accept a resistor and capacitor that are used to determine whether a narrow pulse or wide pulse has been received. The time constant $R_1 \times C_1$ should be set to 1:72 encoder clock periods:

$R_1 C_1 = 3.95 R_{TC} C_{TC}$.

R_2/C_2 (Pin 10)

As shown in Figures 2 and 3, this pin accepts a resistor and capacitor that are used to detect both the end of a received word and the end of a transmission. The time contant $R_2 \times C_2$ should be 33.5 encoder clock periods (four data periods per Figure 11): $R_2 C_2 = 77 R_{TC} C_{TC}$. This time contant is used to determine whether the data in pin has remained low for four data periods (end of transmission). A separate on-chip comparator looks at the voltage-equivalent two data periods ($0.4 R_2 C_2$) to detect the dead time between received words within a transmission.

VT (Pin 11)

This valid transmission output goes high after the second word of an encoding sequence when the following conditions are satisfied:

(1) the received addresses of both words match the local decoder address, and

(2) the received data bits of both words match.

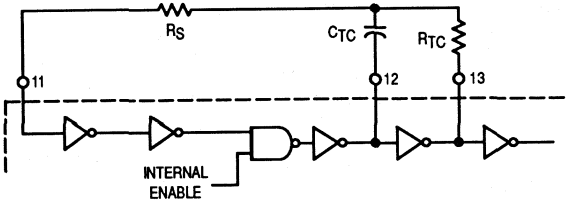
VT remains high until either a mismatch is received or no input signal is received for four data periods.

V_{SS} (Pin 8)

The most-negative supply potential. This pin is usually ground.

V_{DD} (Pin 16)

The most-positive power supply pin.



This oscillator operates at a frequency determined by the external RC network; i.e.,

$$f \approx \frac{1}{2.3\, R_{TC}\, C_{TC}'} \text{ (Hz)}$$

for $1\text{ kHz} \le f \le 400\text{ kHz}$

where: $C_{TC}' = C_{TC} + C_{layout} + 12\text{ pF}$

$R_S \approx 2 R_{TC}$

$R_S \ge 20\text{ k}$

$R_{TC} \ge 10\text{ k}$

$400\text{ pF} < C_{TC} < 15\ \mu\text{F}$

The value for R_S should be chosen to be ≥2 times R_{TC}. This range ensures that current through R_S is insignificant compared to current through R_{TC}. The upper limit for R_S must ensure that R_S x 5 pF (input capacitance) is small compared to $R_{TC} \times C_{TC}$.

For frequencies outside the indicated range, the formula is less accurate. The minimum recommended oscillation frequency of this circuit is 1 kHz. Susceptibility to externally induced noise signals may occur for frequencies below 1 kHz and/or when resistors utilized are greater than 1 MΩ.

Figure 9. Encoder Oscillator Information

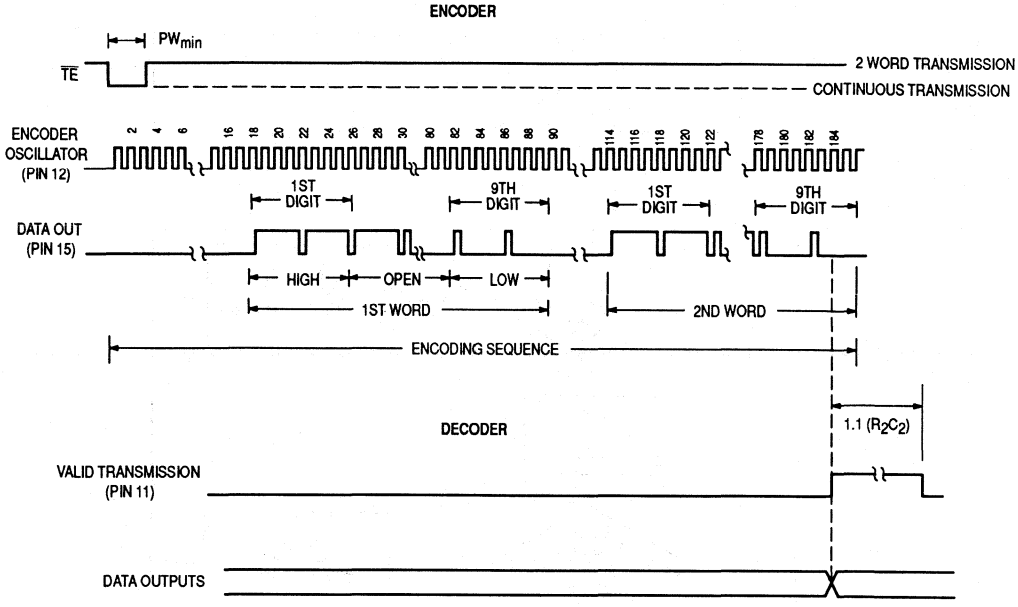


Figure 10. Timing Diagram

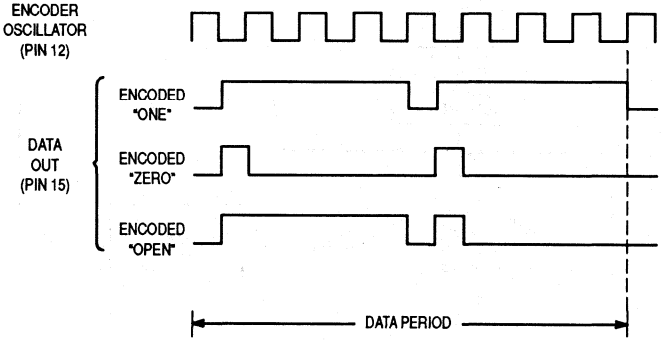


Figure 11. Encoder Data Waveforms

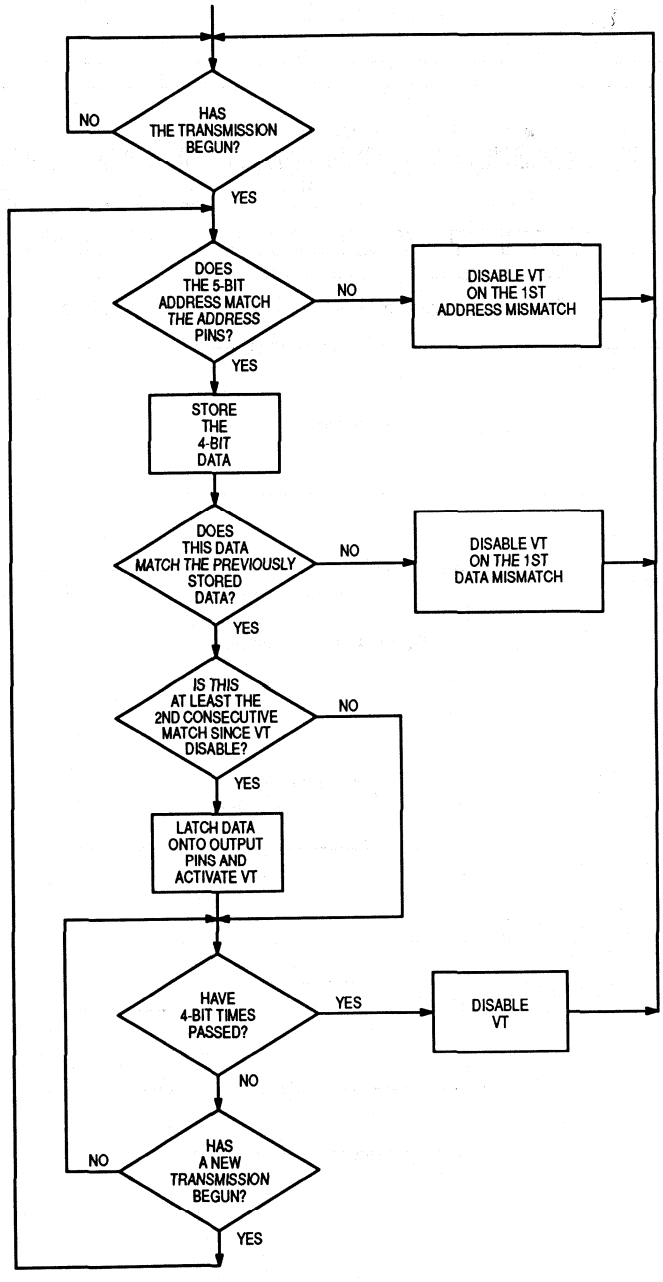


Figure 12. MC145027 Flowchart

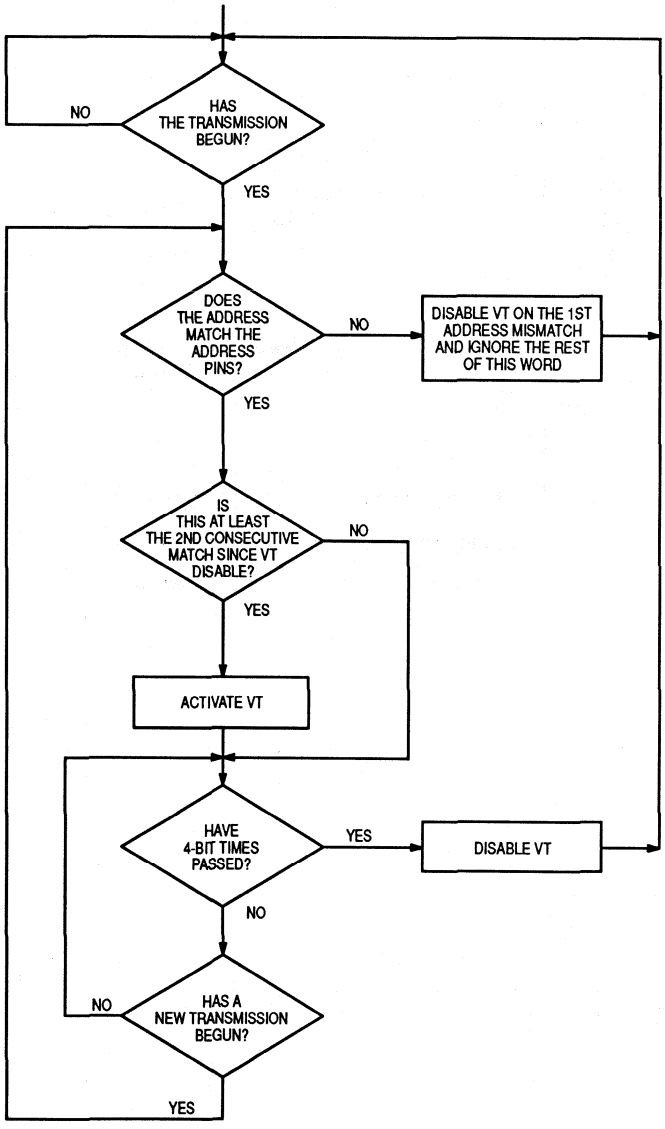


Figure 13. MC145028 Flowchart

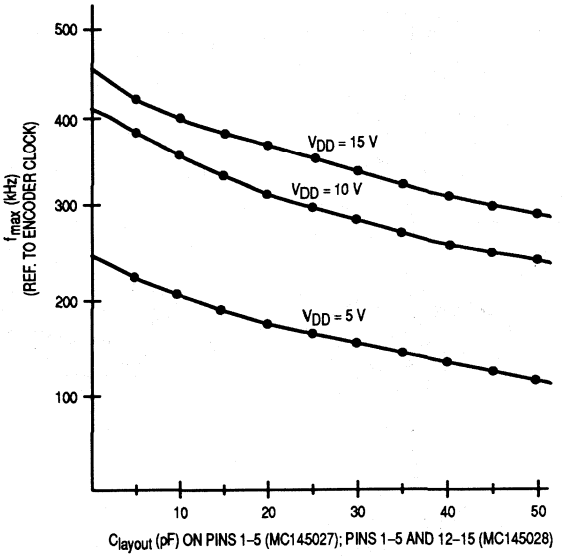
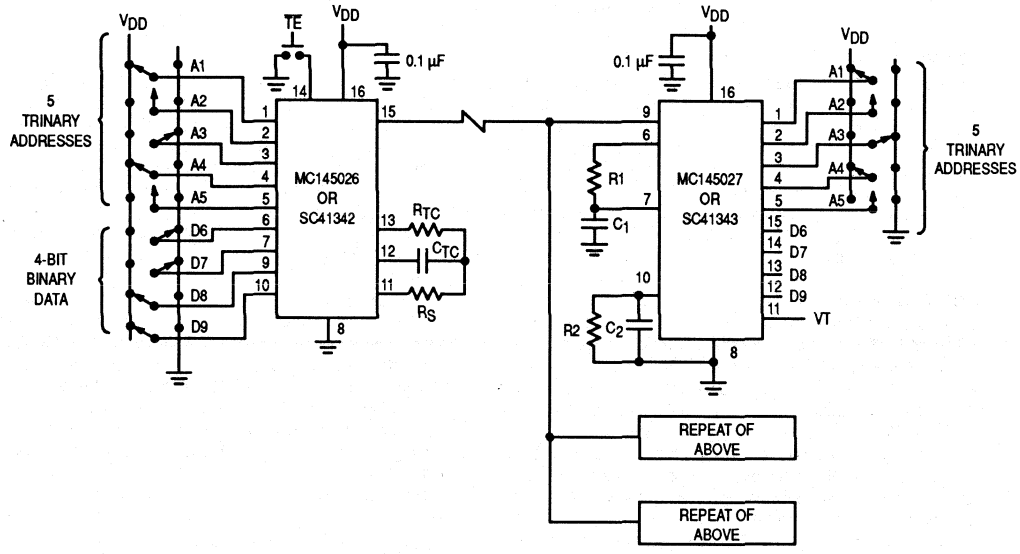


Figure 14. f_{max} vs C_{layout} — Decoders Only



$$f_{osc} = \frac{1}{2.3\,R_{TC}C_{TC}'}$$

$R_1C_1 = 3.95\,R_{TC}C_{TC}$

$R_2C_2 = 77\,R_{TC}C_{TC}$

$C_{TC}' = C_{TC} + C_{layout} + 12$ pF
$100\text{ pF} \le C_{TC} \le 15\ \mu F$
$R_{TC} \ge 10$ k; $R_S \approx 2\,R_{TC}$
$R_1 \ge 10$ k
$C_1 \ge 400$ pF
$R_2 \ge 100$ k
$C_2 \ge 700$ pF

Example R/C Values
(All Resistors and Capacitors are ±5%)

($C_{TC}' = C_{TC} + 20$ pF)

f_{osc} (kHz)	R_{TC}	C_{TC}'	R_S	R_1	C_1	R_2	C_2
362	10 k	120 pF	20 k	10 k	470 pF	100 k	910 pF
181	10 k	240 pF	20 k	10 k	910 pF	100 k	1800 pF
88.7	10 k	490 pF	20 k	10 k	2000 pF	100 k	3900 pF
42.6	10 k	1020 pF	20 k	10 k	3900 pF	100 k	7500 pF
21.5	10 k	2020 pF	20 k	10 k	8200 pF	100 k	0.015 µF
8.53	10 k	5100 pF	20 k	10 k	0.02 µF	200 k	0.02 µF
1.71	50 k	5100 pF	100 k	50 k	0.02 µF	200 k	0.1 µF

Figure 15. Typical Application

APPLICATIONS INFORMATION

Infrared Transmitter

In Figure 16, the MC145026 encoder is set to run at an oscillator frequency of about 4 kHz to 9 kHz. Thus, the time required for a complete two-word encoding sequence is about 20 ms to 40 ms. The data output from the encoder gates an RC oscillator running at 50 kHz; the oscillator shown starts rapidly enough to be used in this application. When the "send" button is not depressed, both the MC145026 and oscillator are in a low-power standby state. The RC oscillator has to be trimmed for 50 kHz and has some drawbacks for frequency stability. A superior system uses a ceramic resonator oscillator running at 400 kHz. This oscillator feeds a divider as shown in Figure 17. The unused inputs of the MC14011UB must be grounded.

The MLED81 IRED is driven with the 50 kHz square wave at about 200 mA to 300 mA to generate the carrier. If desired, 2 IREDs wired in series can be used. (See Application Note AN1016 for more information.) The bipolar IRED switch shown in Figure 16 offers two advantages over a FET. First, a logic FET has too much gate capacitance for the MC14011UB to drive without waveform distortion. Second, the bipolar drive permits lower supply voltages, which are an advantage in portable battery-powered applications.

The configuration shown in Figure 16 operates over a supply range of 4.5 V to 18 V. A low-voltage system which operates down to 2.5 V could be realized if the SC41342 (the low-voltage version of the MC145026) is used in lieu of the MC145026. The oscillator section of a MC74HC4060 is used in place of the MC14011UB. The data output of the SC41342 is inverted and fed to the reset pin of the MC74HC4060. Alternately, the MC74HCU04 could be used for the oscillator.

Information on the MC14011UB is in book number DL131/D. The MC74HCU04 and MC74HC4060 are found in book number DL129/D.

Infrared Receiver

The receiver in Figure 18 couples an IR-sensitive diode to input preamp A1, followed by bandpass amplifier A2 with a gain of about 10. Limiting stage A3 follows, with an output of about 800 mVp-p. The limited 50 kHz burst is detected by comparator A4 that passes only positive pulses, and peak-detected and filtered by a diode/RC network to extract the data envelope from the burst. Comparator A5 boosts the signal to logic levels compatible with the MC145027/8 data input. The data in pin of these decoders is a standard CMOS high-impedance input which must NOT be allowed to float. Therefore, direct coupling from A5 to the decoder input is utilized.

Shielding should be used on at least A1 and A2, with good ground and high-sensitivity circuit layout techniques applied.

For operation with supplies higher than +5 V, limiter A4's positive output swing needs to be limited to 3 V to 5 V. This is accomplished via adding a zener diode in the negative feedback path, thus avoiding excessive system noise. The biasing resistor stack should be adjusted such that V3 is 1.25 V to 1.5 V.

This system works up to a range of about 10 meters. The gains of the system may be adjusted to suit the individual design needs. The 100 Ω resistor in the emitter of the first 2N5088 and the 1 kΩ resistor feeding A2 may be altered if different gain is required. In general, more gain does not necessarily result in increased range. This is due to noise floor limitations. The designer should increase transmitter power and/or increase receiver aperature with fresnal lensing to greatly improve range. See applications note AN1016 for additional information.

Information on the MC34074 is in data book DL128/D.

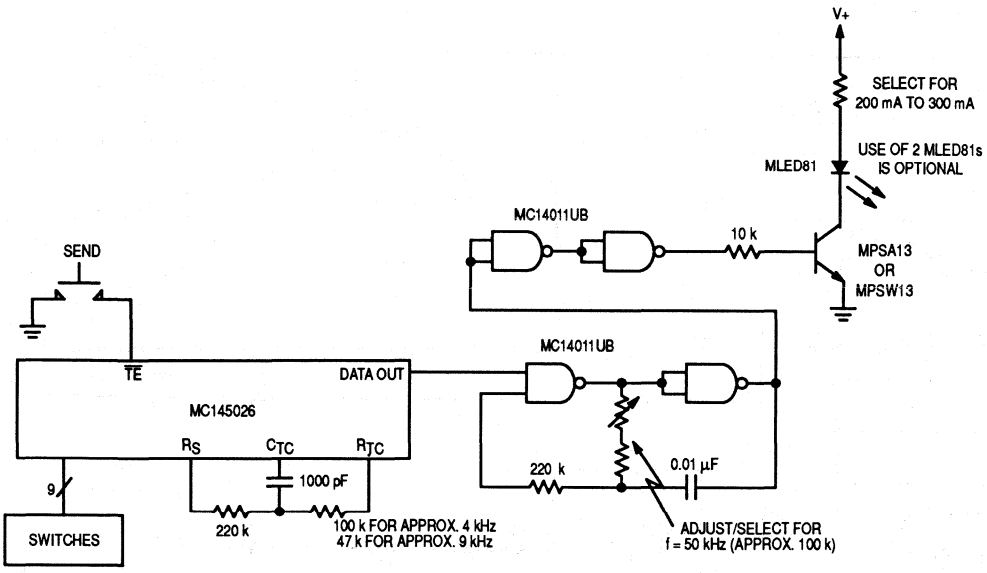


Figure 16. IRED Transmitter Using RC Oscillator to Generate Carrier Frequency

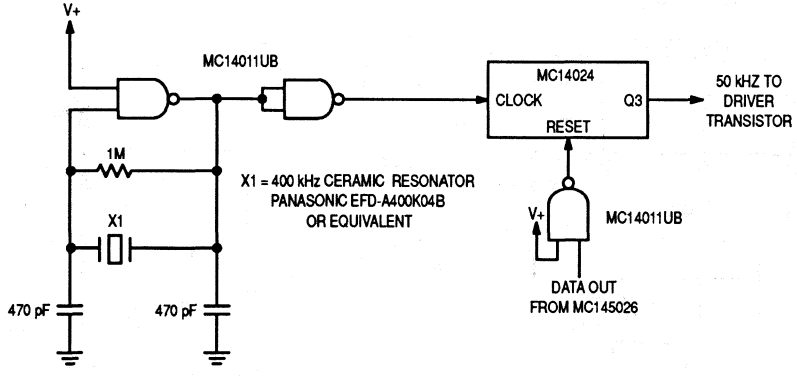


Figure 17. Using a Ceramic Resonator to Generate Carrier Frequency

MAXIMUM RATINGS* (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +7.0	V
V_{in}	DC Input Voltage	−0.5 to V_{DD}+0.5	V
V_{out}	DC Output Voltage	−0.5 to V_{DD}+0.5	V
I_{in}	DC Input Current, per Pin	±10	mA
I_{out}	DC Output Current, per Pin	±10	mA
I_{DD}	DC Supply Current, V_{DD} and V_{SS} Pins	±30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating: −12 mW/°C from 65°C to 85°C.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Except for the Address inputs, unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). The Address inputs may be left open; see Pin Descriptions. Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, Voltages Referenced to V_{SS})

Symbol	Parameter	Test Condition	V_{DD} V	Guaranteed Limit	Unit
V_{DD}	Power Supply Voltage Range		—	2.0 to 6.0	V
V_{IL}	Maximum Low-Level Input Voltage — Except Decoder In		2.5 6.0	0.3 1.2	V
V_{IH}	Minimum High-Level Input Voltage — Except Decoder In		2.5 6.0	1.9 4.5	V
V_{sig}	Minimum Output Voltage of Signal Source Driving Decoder In	Square-Wave Source See Figure 1	2.5 6.0	200 200	mVp-p
V_{OL}	Maximum Low-Level Output Voltage	I_{out} = 0 μA I_{out} = 0.4 mA	2.5	0.15 0.4	V
		I_{out} = 0 μA I_{out} = 1.0 mA	6.0	0.15 0.4	
V_{OH}	Minimum High-Level Output Voltage	I_{out} = 0 μA I_{out} = −0.4 mA	2.5	2.35 2.0	V
		I_{out} = 0 μA I_{out} = −1.0 mA	6.0	5.85 5.5	
I_{in}	Maximum Input Current — Decoder In Encode Enable, Decoder Reset, Osc In	V_{in} = V_{DD} or V_{SS}	6.0	±60 ±0.3	μA
I_{IH}	Maximum High-Level Input Leakage Current — A0-A8	V_{in} = V_{DD}	6.0	0.3	μA
I_{IL}	Maximum Low-Level Pull-Up Current — A0-A8	V_{in} = V_{SS}	6.0	−100	μA
I_{OZ}	Maximum 3-State Leakage Current — Encoder Out	V_{out} = V_{DD} or V_{SS}	6.0	±500	nA
I_{DD}	Maximum Quiescent Supply Current (per Package)	Device in Standby Mode V_{in} = V_{SS} or V_{DD} for Encode Enable, Decoder In, Decoder Reset, Osc In V_{in} = V_{SS}, V_{DD}, or Open for A0-A8 I_{out} = 0 μA	2.0 6.0	20 100	μA
I_{dd}	Maximum RMS Operating Supply Current (per Package)	Oscillator Frequency = 500 kHz V_{in} = V_{SS} or V_{DD} for Encode Enable, Decoder In, Decoder Reset, Osc In V_{in} = V_{SS}, V_{DD}, or Open for A0-A8 I_{out} = 0 μA	2.5 6.0	700 2500	μA

AC ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $C_L = 50$ pF, $V_{DD} = 2.5$ to 6 V unless otherwise stated)

Symbol	Parameter	V_{DD} V	Guaranteed Limit	Unit
f_{osc}	Maximum Oscillator Frequency (~50% Duty Cycle) (Figure 2)*	–	500	kHz
t_{PLH}, t_{PHL}	System Propagation Delay, Encode Enable (of an encoding device) to Decoder Out (of a decoding device) Figures 3 and 5	–	384 to 608	Osc Cycles
t_d	Debounce Time, Encode Enable (guarantees 1 encoding sequence)	–	608	Osc Cycles
t_w	Minimum Input Pulse Width, Encode Enable or Decoder Reset (Figure 4)	2.5 6.0	200 80	ns
C_{in}	Maximum Input Capacitance	–	10	pF

*See Pin Descriptions and Application Example for component tolerances.

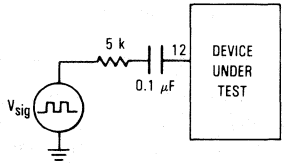


Figure 1. Decoder In Sensitivity Test

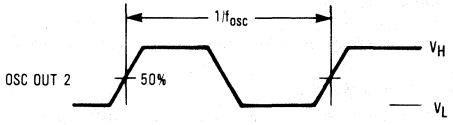


Figure 2. Switching Waveform

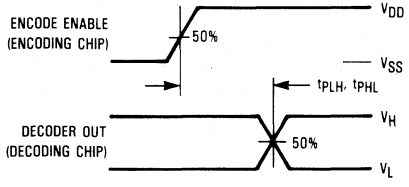


Figure 3. Switching Waveforms

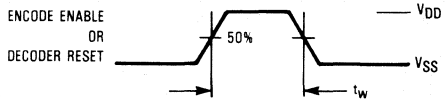
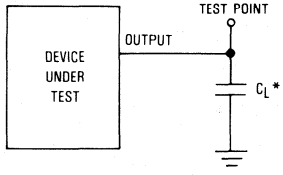


Figure 4. Switching Waveform



*Includes all probe and jig capacitance.

Figure 5. Test Circuit

PIN DESCRIPTIONS

INPUTS

A0 through A8 (Pins 1, 3-9, 2)

Local Address Inputs. These binary inputs provide the address for both the encoder and decoder; 512 addresses are possible. The local address is sent serially from Encoder Out with 2 sync bits appearing first, followed by A0. The decoder compares the local address with the received address stream.

On-chip pullup devices are provided on the address inputs to facilitate interface to SPST switches or jumpers to V_{SS}. During standby, A0 through A8 are in the high-impedance state. That is, the pullup devices are inactive to minimize standby power consumption.

The inputs are left open (or tied to V_{DD}) for a high level and tied to V_{SS} for a low level.

Encode Enable (Pin 10)

Edge-Sensitive Encode Enable. A low-to-high transition on this pin aborts any decoding sequence in progress and initiates an encoding sequence. This input is debounced 608 oscillator cycles. See Figures 8 and 9.

Decoder In (Pin 12)

Decoder In is the input to the on-chip amplifier. The incoming signal is usually capacitively-coupled to this pin. Direct coupling may be used if the signal level is rail-to-rail (V_{SS} to V_{DD}).

Decoder Reset (Pin 13)

Level-Sensitive Decoder Reset. When this input is taken high, Decoder Out is cleared to a low level. This pin may be used to override a response from a Decoder In data stream.

OUTPUTS

Status (Pin 11)

Encode/Decode Status. This pin is high during the encoding sequence and low during decoding or idle.

When Status is low, the Encoder Out pin is in the high-impedance state.

Decoder Out (Pin 15)

Toggle Flip-Flop Decoder Output. The encoder sends the same address twice to complete a sequence. If one or both of the decoded addresses matches the local address, Decoder Out toggles once per sequence (unless overridden by Decoder Reset). See Figures 6 and 7.

Encoder Out (Pin 16)

Three-State Encoder Output. This is the serial output of the Manchester-encoded local address. A0 appears before A8 in the bit stream. The local address is sent twice to complete a sequence which is initialized by Encode Enable. When a sequence is complete, Encoder Out returns to the high-impedance state. See Figures 8 and 9.

OSCILLATOR

Osc In, Osc Out 1, Osc Out 2 (Pins 20, 19, 18)

As shown in Figure 10, these pins are used in conjunction with external resistors and a capacitor to form an oscillator. Polystyrene or mylar capacitors are recommended. Susceptibility to externally induced noise signals may occur if resistors utilized are greater than 1 megohm. See Figure 10 for component tolerances.

When the on-chip oscillator is used, the frequency may be up to 500 kHz. The oscillator is active only during encoding or decoding.

When an external frequency source is used to drive Osc In, Osc Out 1, and Osc Out 2 may be left floating. The signal applied to Osc In should swing rail-to-rail and may be dc to 500 kHz.

POWER

V_{SS} (Pin 17)

This pin is the negative supply potential and is usually ground.

V_{DD} (Pin 14)

This pin is the positive supply potential and may range from +2 to +6 volts with respect to V_{SS}.

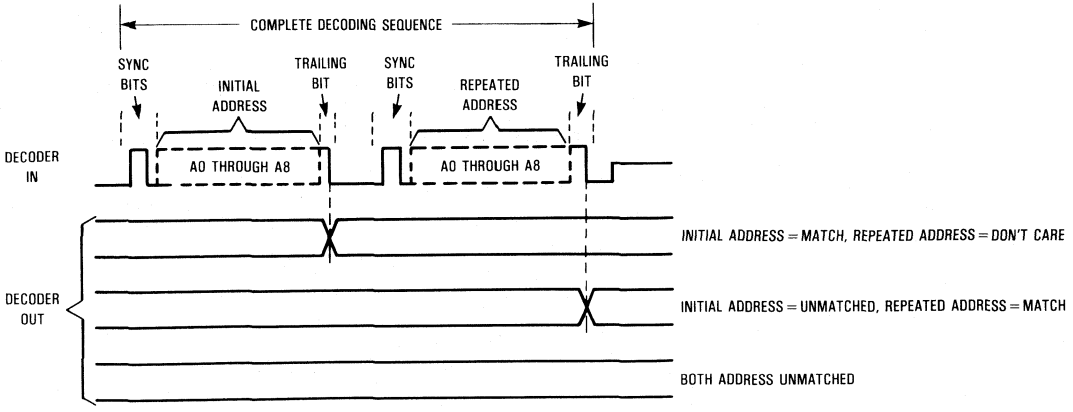


Figure 6. Decoder Timing Diagram

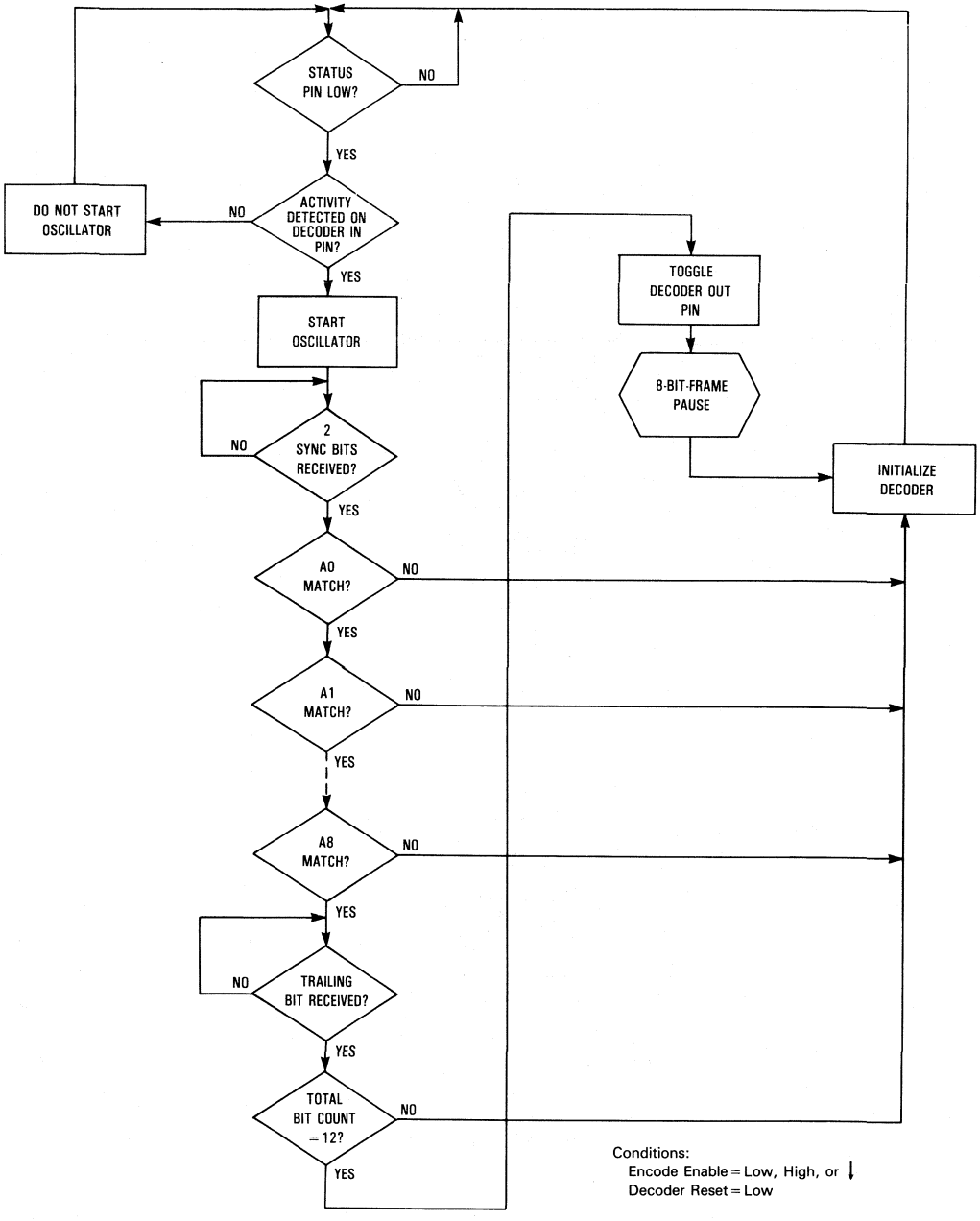


Figure 7. Decoder Flowchart

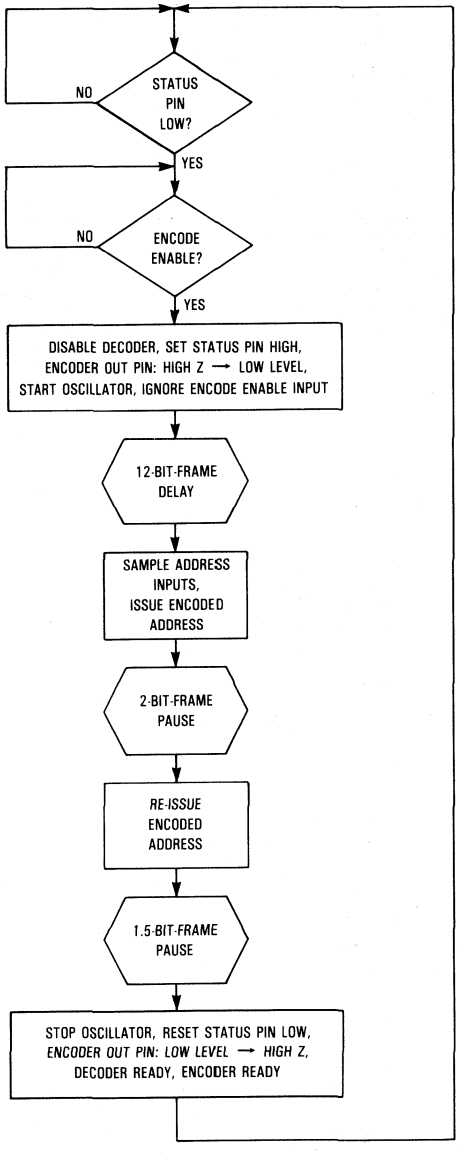


Figure 8. Encoder Flowchart

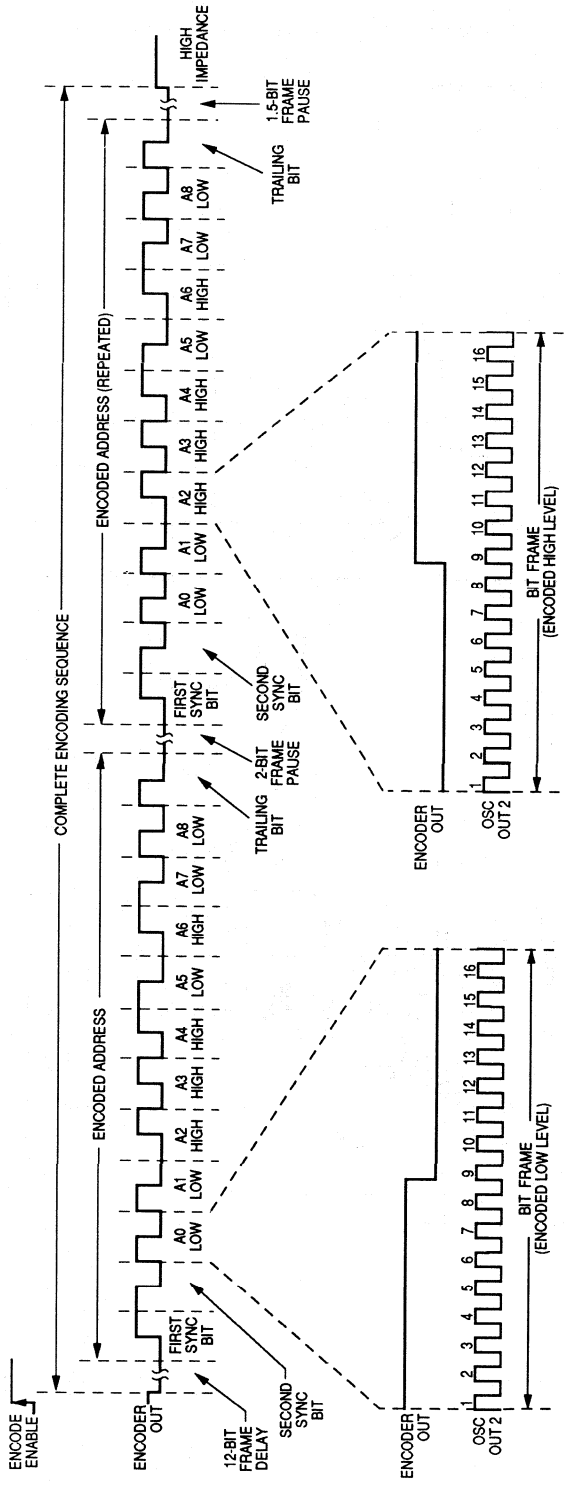
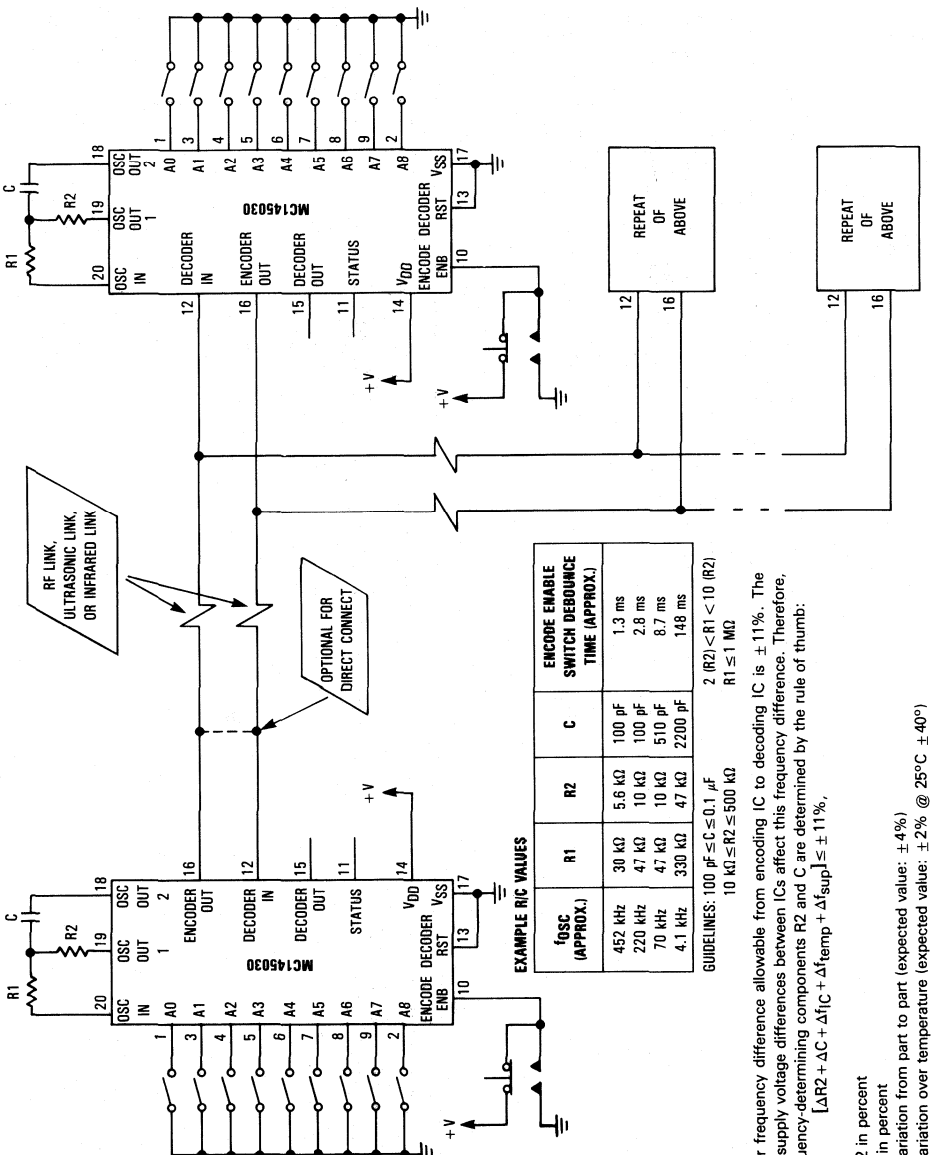


Figure 9. Encoder Timing Diagram



EXAMPLE R/C VALUES

f_{OSC} (APPROX.)	R1	R2	C	ENCODE ENABLE SWITCH DEBOUNCE TIME (APPROX.)
452 kHz	30 kΩ	5.6 kΩ	100 pF	1.3 ms
220 kHz	47 kΩ	10 kΩ	100 pF	2.8 ms
70 kHz	47 kΩ	10 kΩ	510 pF	8.7 ms
4.1 kHz	330 kΩ	47 kΩ	2200 pF	148 ms

GUIDELINES: 100 pF ≤ C ≤ 0.1 μF; 2 (R2) < R1 < 10 (R2)
10 kΩ ≤ R2 ≤ 500 kΩ; R1 ≤ 1 MΩ

The maximum oscillator frequency difference allowable from encoding IC to decoding IC is ±11%. The ambient temperature and supply voltage differences between ICs affect this frequency difference. Therefore, the tolerances of the frequency-determining components R2 and C are determined by the rule of thumb:

$$[\Delta R2 + \Delta C + \Delta f_{IC} + \Delta f_{temp} + \Delta f_{sup}] \leq \pm 11\%,$$

where

R2 = tolerance of R2 in percent
C = tolerance of C in percent
f_{IC} = IC frequency variation from part to part (expected value: ±4%)
f_{temp} = IC frequency variation over temperature (expected value: ±2% @ 25°C, ±40°)
f_{sup} = IC frequency variation with supply (expected value: ±2% @ 5 V ±0.5 V)

From the above variances: $[\Delta R2 + \Delta C + (\pm 4\%) + (\pm 2\%) + (\pm 2\%)] \leq \pm 11\%$

$$[\Delta R2 + \Delta C] \leq \pm 3\%$$

Choose R2 with a ±1% tolerance and C2 with a ±2% tolerance. R1 may be ±5%.

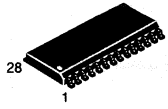
Figure 10. Application Example

Advance Information

MC145031 Encoder
MC145032 Decoder
MC145033 Encoder/Decoder
MC145034 Encoder
MC145035 Decoder

CMOS

MC145031
MC145032
MC145033
MC145034
MC145035



DW SUFFIX
SOG PACKAGE
CASE 751F

ORDERING INFORMATION
MC14503xDW SOG Package

The encoders convert parallel address and data inputs into the Manchester code format and output the information serially via a data out pin.

The decoders revert the serial Manchester-coded input back into binary and compare the incoming address with local one. If both addresses match, an output valid signal (VD) is asserted and the proper data appears at the data out pins.

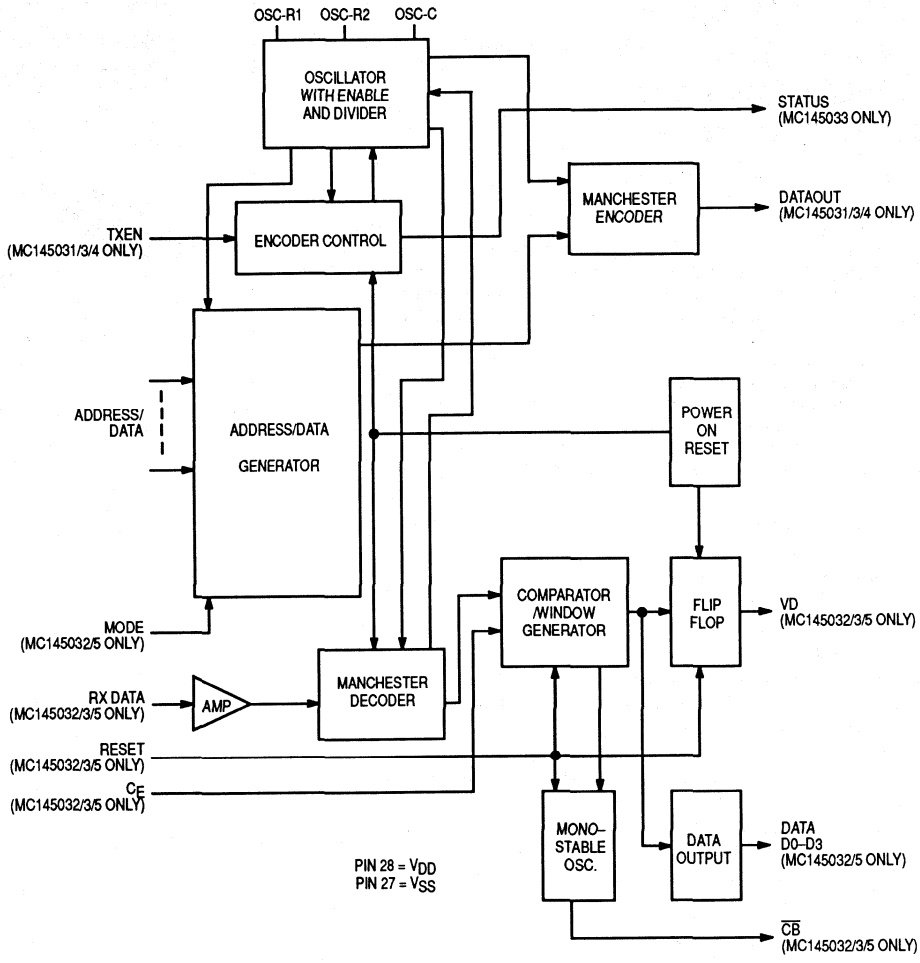
The difference between the MC145031/2 and MC145034/5 is the valid output pin, VD. The valid output of the MC145031/2 is a toggle function while the MC145034/5 is a "one shot" valid address output pulse if a correct data sequence and matched address is received.

The MC145033 encoder/decoder has a status output. The status pin, when high, indicates the device is encoding. During decoding or standby, status is low.

- Typical Applications: Remote Control, Security Systems, and Keyless Entry
- Manchester Coding
- RC Oscillator, No Crystal Required
- Binary Address and Data Inputs
- Two-Word Transmit Sequence
- Built-In Input Data Amplifier
- Schmitt-Trigger Serial Input for Excellent Noise Immunity
- Code Break Output with Adjustable Error Code Transmission Time Window
- Operating Voltage Range: 2 to 6 V
- Operating Temperature Range: –40° to 85°C
- MC145031 Encoder/MC145032 Decoder Pair: 13 Address and 4 Data Lines or 17 Address Lines
- MC145033 Encoder/Decoder: 15 Address Lines
- MC145034 Encoder/MC145035 Decoder Pair: 13 Address and 4 Data Lines or 17 Address Lines

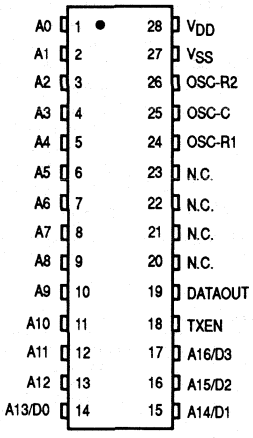
This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM OF MC145031/2/3/4/5

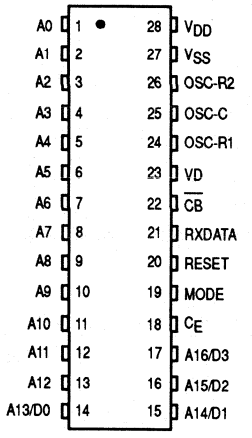


PIN ASSIGNMENTS

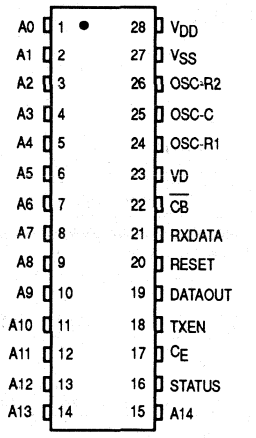
MC145031 ENCODER



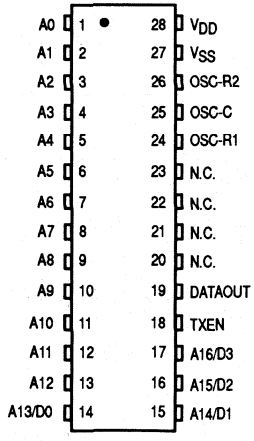
MC145032 DECODER



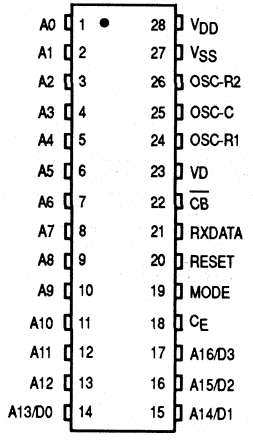
MC145033 ENCODER/DECODER



MC145034 ENCODER



MC145035 DECODER



MAXIMUM RATING* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	–0.5 to +0.7	V
V_{in}	DC Input Voltage	–0.5 to V_{DD}+0.5	V
V_{out}	DC Output Voltage	–0.5 to V_{DD}+0.5	V
I_{in}	DC Input Current, per Pin	±10	mA
I_{out}	DC Output Current, per Pin	±10	mA
I_{DD}	DC Supply Current, V_{DD} and V_{SS} Pins	±30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	–65 to +150	°C
T_L	Lead Temperature (10-second soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Power Dissipation Temperature Derating

–12 mW/°C from 65°C to 85°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$.

Except for the Address inputs, unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). The Address inputs may be left open, see Pin Descriptions. Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (T_A=–40° to 85°C, C_L=50 pF, V_{DD}=2.5 to 6 V unless otherwise stated)

Symbol	Parameter	Test Condition	V_{DD} V	Guaranteed Limit	Unit
V_{DD}	Power Supply Voltage Range		—	2.0 to 6.0	V
V_{IL}	Maximum Low-Level Input Voltage Except RXDATA		2.5 6.0	0.3 1.2	V
V_{IH}	Minimum High-Level Input Voltage Except RXDATA		2.5 6.0	1.9 4.5	V
V_{OL}	Maximum Low-Level Output Voltage	I_{out}=0 µA I_{out}=0.4 mA	2.5	0.15 0.4	V
		I_{out}=0 µA I_{out}=1.0 mA	6.0	0.15 0.4	
V_{OH}	Minimum High-Level Output Voltage	I_{out}=0 µA I_{out}=–0.4 mA	2.5	2.35 2.0	V
		I_{out}=0 µA I_{out}=–1.0 mA	6.0	5.85 5.5	
I_{in}	Maximum Input Current RXDATA TXEN, Reset, OSC-R2	V_{in}=V_{DD} or V_{SS}	6.0	±80 ±0.3	µA
I_{IH}	Maximum High-Level Input Leakage Current A0–A16	V_{in}=V_{DD}	6.0	0.3	µA
I_{IL}	Maximum Low-Level Pull–Up Current A0–A16	V_{in}=V_{SS}	6.0	–100	µA
I_{OZ}	Maximum 3–State Leakage Current Data Out	V_{out}=V_{DD} or V_{SS}	6.0	±500	nA
I_{DD}	Maximum Quiescent Supply Current (per Package)	Device in standby mode, V_{in}=V_{DD} or V_{SS} for TXEN, Decoder in, Reset, OSC-R2. V_{in}=V_{SS}, V_{DD}, or open for A0–A16. I_{out}=0 µA	2.5 6.0	25 100	µA
I_{dd}	Maximum RMS Operating Supply Current (per Package)	Oscillator Frequency =500 kHz. V_{in}=V_{SS} or V_{DD} for TXEN, Reset, OSC-R2. V_{in}=V_{SS}, V_{DD}, or open for A0–A16. I_{out}=0 µA	2.5 6.0	700 2500	µA
I_{OL}	Code Break Sink Current $\overline{CB}$			5	mA
V_{in}	Minimum RXDATA Input Level For Decoder	Square wave, see Figure 1	6.0	200	mV pp

AC ELECTRICAL CHARACTERISTICS (T_A=25°C, C_L=50 pF, V_{DD}=2.5 to 6 V unless otherwise stated)

Symbol	Parameter	V_{DD} V	Guaranteed Limit	Unit
f_{OSC}	Maximum Oscillator Frequency (50% Duty Cycle) (Figure 2)	—	500	kHz
t_d	Debounce Time, TXEN (guarantees 1 encoding sequence)	—	500	OSC cycles
t_w	Minimum Input Pulse Width, TXEN or Reset (Figure 3)	2.5 6.0	200 80	ns
C_{in}	Maximum Input Capacitance	—	10	pF

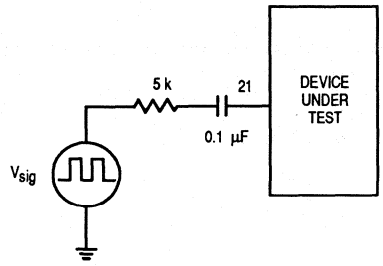


Figure 1. Decoder In Sensitivity Test

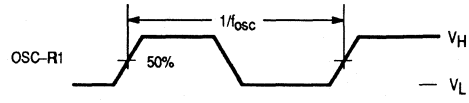


Figure 2. Switching Waveform

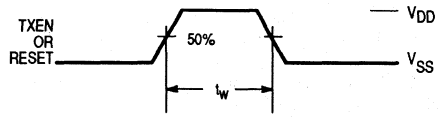


Figure 3. Switching Waveform

GENERAL DESCRIPTION

ENCODER

The encoder circuit encodes the parallel binary input address/data into manchester code and outputs the information serially.

Each transmitted word is preceded by a two-bit dead time interval. Once the TXEN (transmit enable) pin is triggered by a high level, a two-word transmit sequence following a 12-bit preamble is serially output at the DATAOUT terminal. The transmit sequences repeat continuously if the TXEN remains high. The minimum is one complete sequence; if TXEN goes low, the transmission continues until the end of the current transmit sequence.

The data rate is set at one eighth of the system clock, which is a RC oscillator.

One transmission cycle comprises:

1. 12-bit preamble
2. 2-bit dead time interval
3. First word
4. 2-bit dead time interval
5. Second word

One transmitted word consists of:

1. 2 start bits
2. The address/data bits
3. 2 stop bits

DECODER

The decoder circuit accepts a serial manchester-coded input at the RXDATA pin. The data stream is then decoded and compared with the local address set by the parallel address inputs. When a correct transmit sequence (two identical words) is received and the incoming address matches the local one, the VD output on the MC145035 goes high and the decoded data may then be read at the data outputs D0–D3 if the mode pin is high. See the mode pin discription. The valid output VD remains high unless an erroneous address/data is detected or the transmit sequence is terminated.

For the MC145032 and MC145033, the valid data output (VD) is a toggle function. That is, VD changes state once each time a valid sequence of bits is received. If needed, VD can be reset to a low level via the reset pin.

If the decoder detects an error in the incoming transmit sequence, a time window is opened at the end of that sequence. If two consecutive erroneous transmit sequences are received within that window, the code break output $\overline{CB}$ goes low until the window's duration is over. During the opened window, the $\overline{CB}$ output can be reset by either the reset input or a correct transmit sequence that follows. The window duration is controlled by an external capacitor connected to pin C_E. The duration of the code break output is equal to TB which is half of error window time constant TE.

PIN DESCRIPTIONS

V_{DD} (Pin 28)

Power supply. This pin may range from +2 to+ 6 V with respect to V_{SS}.

V_{SS} (Pin 27)

Power supply ground.

TXEN (Pin 18)—MC145031, MC145033, and MC145034 Only

Transmit enable. A low to high transition on this pin initiates a transmit sequence. Transmission is continuous if TXEN remains high.

DATA OUT (Pin 19)—MC145031, MC145033, and MC145034 Only

Three-state encoder output. It serially outputs the manchester-coded transmit data, when initiated by TXEN.

VD (Pin 23)—MC145032 and MC145033 Only

Decoder valid address output. This "toggle" output changes state whenever correct transmit sequence is received and the address matches the local one. See Figure 4. A high level on VD can be cleared by either a correct transmit sequence that follows or the reset input.

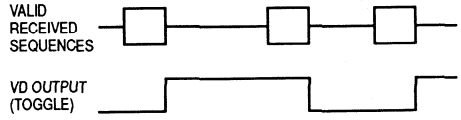


Figure 4. Valid Address Output Timing (MC145032 and MC145033)

VD (Pin 23)—MC145035 Only

Decoder valid address output. This pin goes high if and only if a correct transmit sequence is received and the address matches the local one. The valid output remains high unless an erroneous address/data is detected or the transmit sequence is terminated. The minimum duration of VD is guaranteed by an external RC. See Figures 5 and 6.

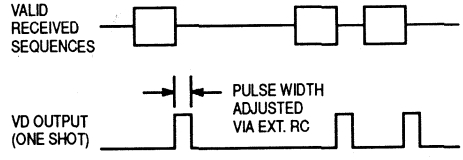


Figure 5. Valid Address Output Timing (MC145035)

RESET (Pin 20)—MC145032 and MC145033 Only

A positive pulse on this pin resets the code break output $\overline{CB}$ and valid address output VD.

RESET (Pin 20)—MC145035 Only

A positive pulse on this pin resets the code break output $\overline{CB}$ and the valid output VD. Its resets VD only when there is no RXDATA received. See Figure 6.

$\overline{CB}$ (Pin 22)—MC145032, MC145033, and MC145035 Only

Decoder code-break open-drain output. It goes low if two additional consecutive erroneous transmit sequences following the 1st error have been received within the window set by

external capacitor C_E. While in active state, it can be cleared by the reset input.

An external PNP transistor may be utilized to charge up the C_E (timing capacitor) to disable the low frequency oscillator. As a result, the TB counter stops. In this case, the $\overline{CB}$ output remains activated until a "reset" signal is applied to reset the C_E flip flop. See Figures 7 and 8.

A0 THROUGH A12 AND A13/D0 THROUGH A16/D3 (Pins 1 Through 17)—MC145031, MC145032, MC145034, and MC145035

Bidirectional address/data pins. These pins form a binary input port during encoding. The pins become a three-state data output port during decoding if the mode pin is tied to V_{DD}.

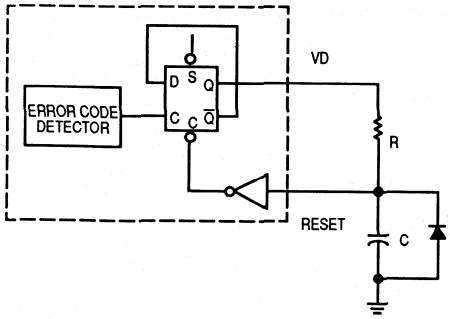


Figure 6. One Shot VD Output Circuit (MC145035)

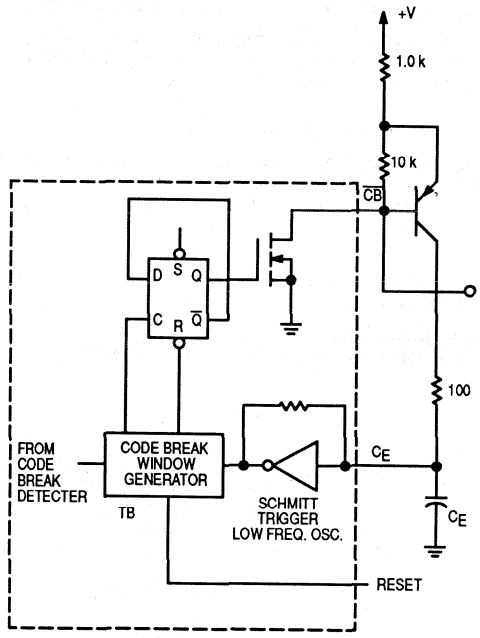


Figure 7. Code Break Window Control

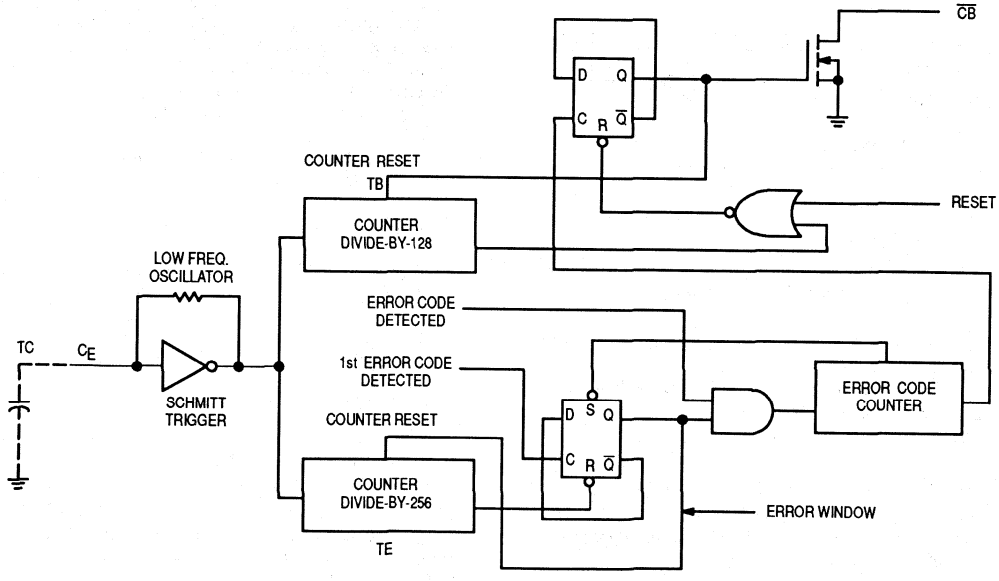


Figure 8. Error Window TE and Code Break Window Generator TB

A0 Through A14 (Pins 1 through 15)—MC145033 Only

Binary address inputs. These pins form a binary input port during the encoding sequence. These inputs become the local address during the decoding sequence.

STATUS (Pin 16)—MC145033 Only

Encode/Decode Status. This pin is high during the encoding sequence and low during decoding or idle.

When Status is low, the DATAOUT pin is in the high-impedance state.

RXDATA (Pin 21)—MC145032, MC145033, and MC145035 Only

Serial data input to the Manchester decoder. Minimum encoded data signal level is 200 mV pp. See Figure 9.

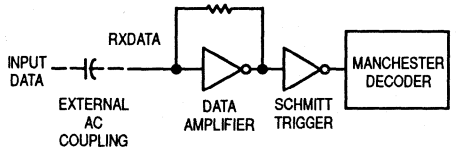
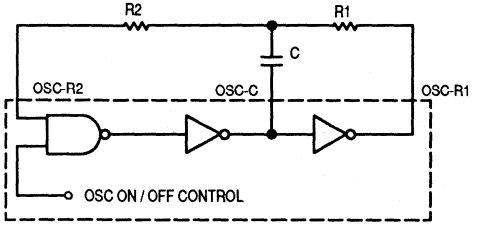


Figure 9. RXDATA Pin Coupling

OSC-R2, OSC-R1, OSC-C (Pins 26, 24, and 25)

Oscillator pins. The oscillator frequency is determined by the external RC network. See Figure 10.



$$f = \frac{0.38}{R1C} \text{ (Hz)}$$

for f ≤ 150 kHz where R2=2R1
The system oscillating frequency is eight times the Encoded Data Rate.

Figure 10. RC Oscillator

There is only 4% change in system oscillating frequency as the supply voltage varies from 2.0 volts to 6.0 volts.

The Encoder System Oscillating frequency can be varied ±10% with reference to Decoder system oscillator frequency for valid detection.

MODE (Pin 19)—MC145032 and MC145035

Mode select input. This pin defines the A13/D0–A16/D3 lines to be address or data lines. It is internally pulled high.

L=Address Lines
H=Data Lines

C_E (Pin 18—MC145032 and MC145035, Pin 17—MC145033)

Error window duration control input. The built-in schmitt trigger oscillator frequency is controlled by external capacitor C_E. The error window TE is equal to 256 times the internal oscillator cycle.

If an unmatched data word (error code) is detected, an internal error window TE is generated. If two or more errors are detected within the TE period, a code break signal $\overline{CB}$ is activated, signalling that an outsider is trying to break the code of this system. (Noise cannot activate the code break output.)

If only one error code is detected within the window, the window period is automatically extended from the last invalid word to check if there are two or more error codes. If so, the code break signal is activated; if not, TE is closed after a defined period. See Figures 8 and 11.

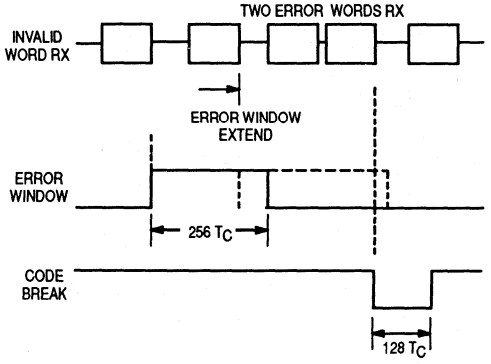


Figure 11. Error Window and Code Break Output Timing

TE and TB are generated from a schmitt-trigger low frequency oscillator of which the period (TC) is controlled by the timing capacitor C_E. The period of this low frequency oscillator is defined as TC as indicated in Figure 8.

TE is generated by an 8-stage counter.

TB is generated by an 7-stage counter.

TE=256 TC and TB=128 TC.

The relation between TC and the timing capacitor C_E is listed below with a 5.0-volt supply.

Timing Capacitor	Cycle Time TC
4.7 µF	1430 ms
1.0 µF	330 ms
0.1 µF	26 ms
0.047 µF	12 ms
0.022 µF	5.6 ms
0.01 µF	2.5 ms
0.0047 µF	1.0 ms
0.001 µF	0.3 ms

In order to minimize false $\overline{CB}$ triggers, one Error Code is allowed for every Error Window period (256 TC).

Suppose C_E = 4.7 µF, TC = 1430 ms, TE = 256 TC. On an average, it takes 2 to the power of 10 trials in order to succeed in breaking the system coding. Total time taken in breaking the system coding = # of trials x TC x 256.

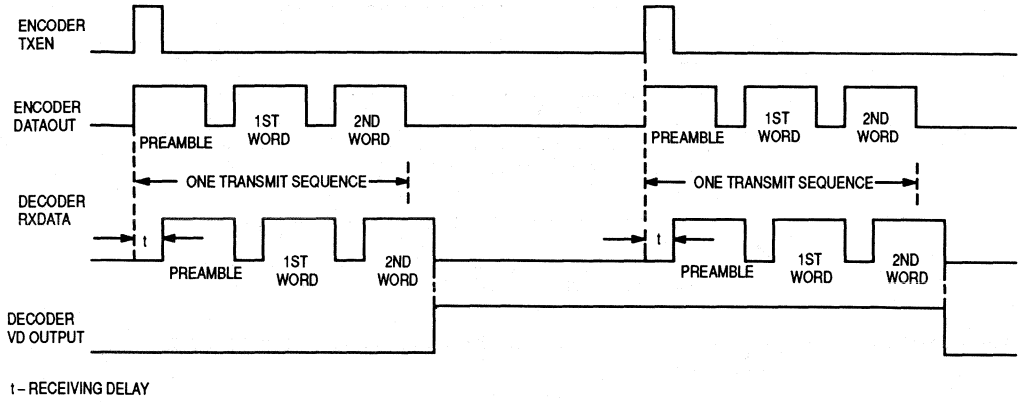


Figure 12. MC145031/2/3 Encoding and Decoding Timing Diagram

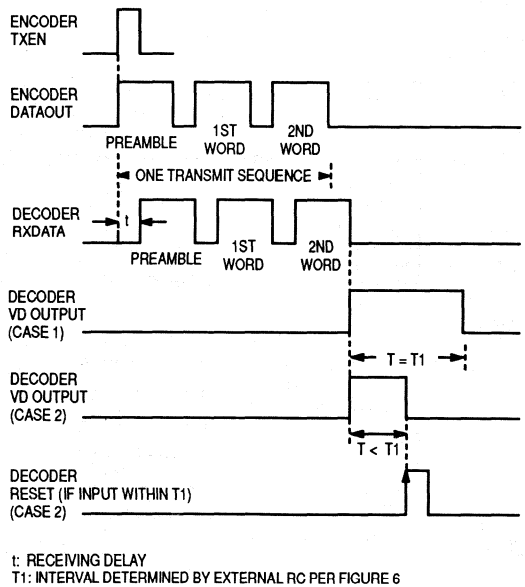


Figure 13. MC145034/5 Encoding and Decoding Timing Diagram — Single Transmission

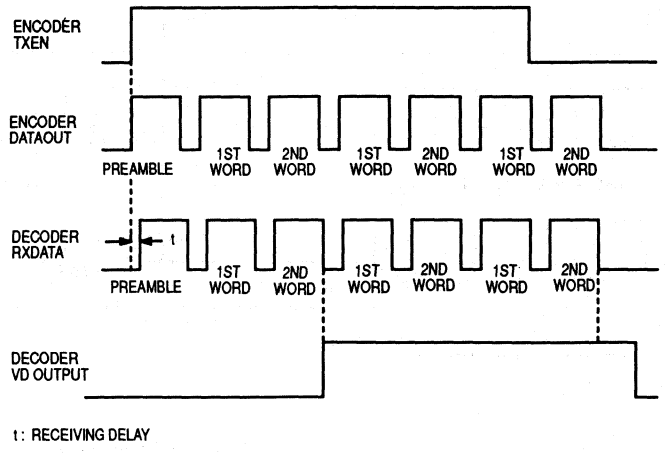


Figure 14. MC145034/5 Encoding and Decoding Timing Diagram — Continuous Transmissions

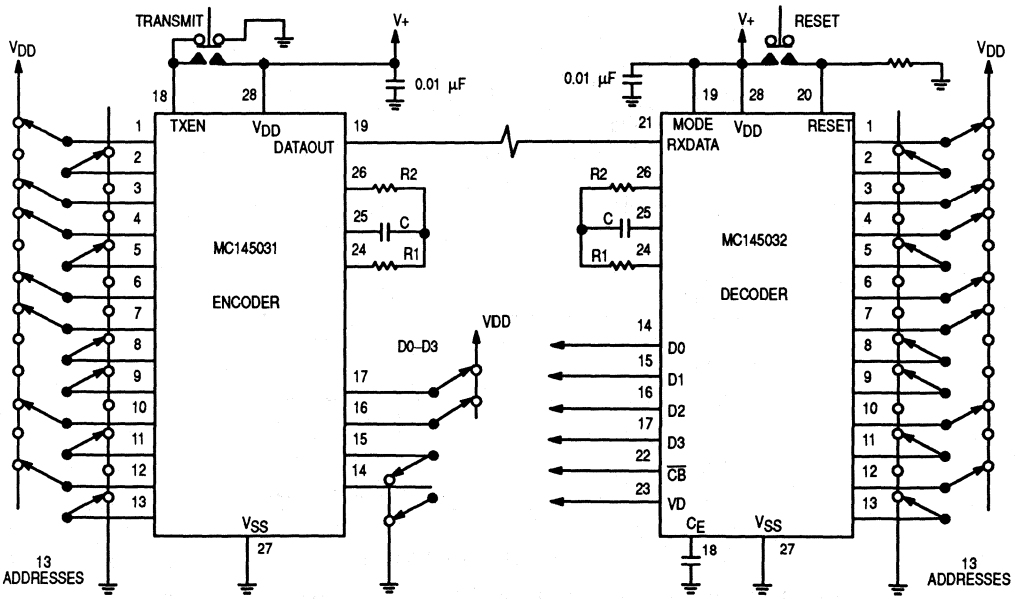


Figure 15. Typical Application

Smoke Detectors

MAXIMUM RATINGS* (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +15	V
Input Voltage, All Inputs Except Pin 8	V_{in}	−0.25 to V_{DD} +0.25	V
DC Current Drain per Input Pin, Except Pin 15 = 1 mA	I	10	mA
DC Current Drain per Output Pin	I	30	mA
Operating Temperature Range	T_A	−10 to +60	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Reverse Battery Time	t_{RB}	5.0	s

*Maximum Ratings are those values beyond which damage to the device may occur.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS})

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	9.0	V
Timing Capacitor	–	0.1	μF
Timing Resistor	–	8.2	MΩ
Battery Load (Resistor or LED)	–	10	mA

ELECTRICAL CHARACTERISTICS (Voltages referenced to V_{SS}, T_A = 25°C)

Characteristic		Symbol	V_{DD} V_{dc}	Min	Typ#	Max	Unit
Operating Voltage		V_{DD}	–	6.0	–	12	V
Output Voltage		V_{OH}					V
Piezoelectric Horn Drivers (I_{OH} = −16 mA)			7.2	6.3	–	–	
Comparators (I_{OH} = −30 μA)			9.0	8.5	8.8	–	
Piezoelectric Horn Drivers (I_{OL} = +16 mA)		V_{OL}	7.2	–	–	0.9	V
Comparators (I_{OL} = +30 μA)			9.0	–	0.1	0.5	
Output Voltage – LED Driver, I_{OL} = 10 mA		V_{OL}	7.2	–	–	3.0	V
Output Impedance, Active Guard	Pin 14	Lo-Z	9.0	–	–	10	kΩ
	Pin 16	Hi-Z	9.0	–	–	1000	
Operating Current (R_{bias} = 8.2 MΩ)		I_{DD}	9.0	–	5.0	9.0	μA
			12.0	–	–	12.0	
Input Current – Detect (40% R.H.)		I_{in}	9.0	–	–	±1.0	pA
Internal Set Voltage							
Low Battery		V_{low}	9.0	7.2	–	7.8	V
Sensitivity		V_{set}	–	47	50	53	%V_{DD}
Hysteresis		V_{hys}	9.0	75	100	150	mV
Offset Voltage (measured at $V_{in} = V_{DD}/2$)		V_{OS}					mV
Active Guard			9.0	–	–	±100	
Detect Comparator			9.0	–	–	±50	
Input Voltage Range, Pin 8		V_{in}	–	−10	–	V_{DD} + 10	V
Input Capacitance		C_{in}	–	–	5.0	–	pF
Common Mode Voltage Range, Pin 15		V_{cm}	–	0.6	–	V_{DD} − 2	V

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that except for pin 8, V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$. For pin 8, refer to the Electrical Characteristics.

TIMING PARAMETERS ($C = 0.1\ \mu F$, $R_{bias} = 8.2\ M\Omega$, $V_{DD} = 9.0\ V$, $T_A = 25°C$, See Figure 5)

Characteristics		Symbol	Min	Typ#	Max	Units
Oscillator Period	No Smoke	t_{Cl}	1.34	1.67	2.0	s
	Smoke		32	40	48	ms
Oscillator Rise Time		t_r	8	10	12	ms
Horn Output	On Time	PW_{on}	120	160	208	ms
(During Smoke)	Off Time	PW_{off}	60	80	104	ms
LED Output	Between Pulses	t_{LED}	32	40	48	s
	On Time	PW_{on}	8	10	12	ms
Horn Output	On Time	t_{on}	8	10	12	ms
(During Low Battery)	Between Pulses	t_{off}	32	40	48	s

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 2 — TYPICAL LED OUTPUT I-V CHARACTERISTIC

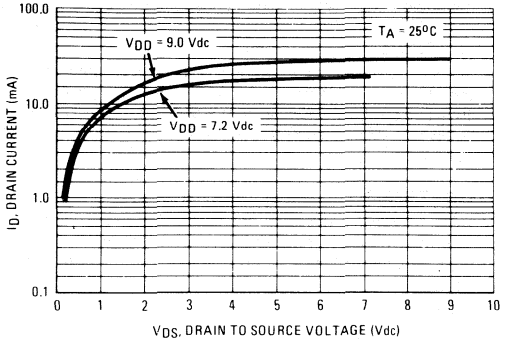


FIGURE 3 — TYPICAL COMPARATOR OUTPUT I-V CHARACTERISTIC

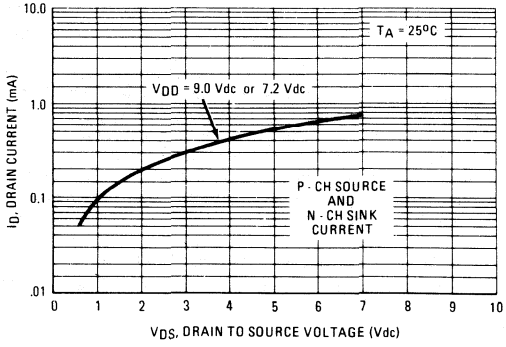
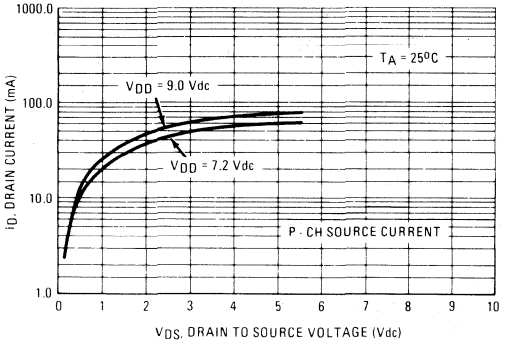
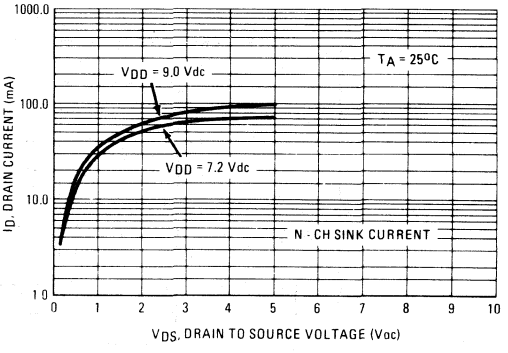


FIGURE 4 — TYPICAL P HORN DRIVER OUTPUT I-V CHARACTERISTIC





MC14468

IONIZATION SMOKE DETECTOR WITH INTERCONNECT

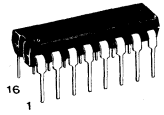
The MC14468, when used with an ionization chamber and a small number of external components, will detect smoke. When smoke is sensed, an alarm is sounded via an external piezoelectric transducer and internal drivers. This circuit is designed to comply with the UL217 and UL268 specifications.

- Ionization Type with On-Chip FET Input Comparator
- Piezoelectric Horn Driver
- Guard Outputs on Both Sides of Detect Input
- Input-Protection Diodes on the Detect Input
- Low-Battery Trip Point, Internally Set, Can Be Altered Via External Resistor
- Detect Threshold, Internally Set, Can Be Altered Via External Resistor
- Pulse Testing for Low Battery Uses LED for Battery Loading
- Comparator Output for Detect
- Internal Reverse Battery Protection
- Strobe Output for External Trim Resistors
- I/O Pin Allows Up to 40 Units to be Connected for Common Signaling
- Power-On Reset Prevents False Alarms on Battery Change

CMOS MSI

(LOW POWER COMPLEMENTARY MOS)

IONIZATION SMOKE DETECTOR WITH INTERCONNECT

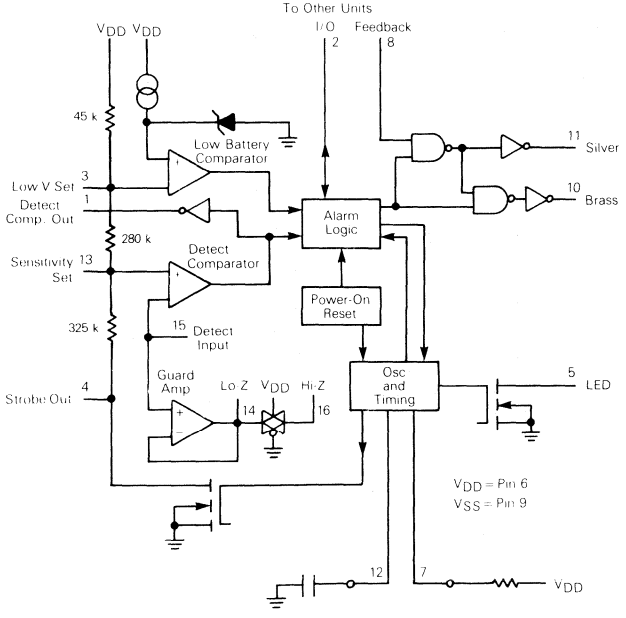


P SUFFIX
PLASTIC DIP
CASE 648

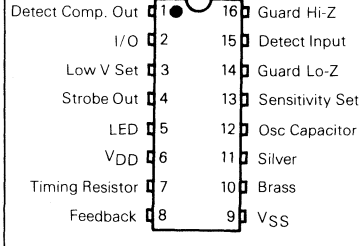
ORDERING INFORMATION

MC14468P	Plastic DIP

BLOCK DIAGRAM



PIN ASSIGNMENT



MAXIMUM RATINGS* (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +15	V
Input Voltage, All Inputs Except Pin 8	V_{in}	−0.25 to V_{DD} +0.25	V
DC Current Drain per Input Pin, Except Pin 15 = 1 mA	I	10	mA
DC Current Drain per Output Pin	I	30	mA
Operating Temperature Range	T_A	−10 to +60	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Reverse Battery Time	t_{RB}	5.0	s

*Maximum Ratings are those values beyond which damage to the device may occur.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS})

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	9.0	V
Timing Capacitor	–	0.1	μF
Timing Resistor	–	8.2	MΩ
Battery Load (Resistor or LED)	–	10	mA

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic		Symbol	V_{DD} V_{dc}	Min	Typ#	Max	Unit
Operating Voltage		V_{DD}	–	6.0	–	12	V
Output Voltage		V_{OH}					V
Piezoelectric Horn Drivers (I_{OH} = −16 mA)			7.2	6.3	–	–	
Comparators (I_{OH} = −30 μA)			9.0	8.5	8.8		
Piezoelectric Horn Drivers (I_{OL} = +16 mA)		V_{OL}	7.2	–	–	0.9	V
Comparators (I_{OL} = +30 μA)			9.0	–	0.1	0.5	
Output Voltage – LED Driver, I_{OL} = 10 mA		V_{OL}	7.2	–	–	3.0	V
Output Impedance, Active Guard	Pin 14	Lo-Z	9.0	–	–	10	kΩ
	Pin 16	Hi-Z	9.0	–	–	1000	
Operating Current (R_{bias} = 8.2 MΩ)		I_{DD}	9.0	–	5.0	9.0	μA
			12.0	–	–	12.0	
Input Current – Detect (40% R.H.)		I_{in}	9.0	–	–	±1.0	pA
Input Current, Pin 8		I_{in}	9.0	–	–	±0.1	μA
Input Current @ 50°C, Pin 15		I_{in}	–	–	–	±6.0	pA
Internal Set Voltage							
Low Battery		V_{low}	9.0	7.2	–	7.8	V
Sensitivity		V_{set}	–	47	50	53	%V_{DD}
Hysteresis		V_{hys}	9.0	75	100	150	mV
Offset Voltage (measured at V_{in} = V_{DD}/2)		V_{OS}					mV
Active Guard			9.0	–	–	±100	
Detect Comparator			9.0	–	–	±50	
Input Voltage Range, Pin 8		V_{in}	–	−10	–	V_{DD} + 10	V
Input Capacitance		C_{in}	–	–	5.0	–	pF
Common Mode Voltage Range, Pin 15		V_{cm}	–	0.6	–	V_{DD} − 2	V
I/O Current, Pin 2							
Input, V_{IH} = V_{DD} − 2		I_{IH}	–	25	–	100	μA
Output, V_{OH} = V_{DD} − 2		I_{OH}	–	−4.0	–	−16	mA

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

TIMING PARAMETERS ($C = 0.1\ \mu F$, $R_{Bias} = 8.2\ M\Omega$, $V_{DD} = 9.0\ V$, $T_A = 25°C$, See Figure 5)

Characteristics		Symbol	Min	Typ#	Max	Units
Oscillator Period	No Smoke	t_{Cl}	1.34	1.67	2.0	s
	Smoke		32	40	48	ms
Oscillator Rise Time		t_r	8	10	12	ms
Horn Output	On Time	PW_{on}	120	160	208	ms
(During Smoke)	Off Time	PW_{off}	60	80	104	ms
LED Output	Between Pulses	t_{LED}	32	40	48	s
	On Time	PW_{on}	8	10	12	ms
Horn Output	On Time	t_{on}	8	10	12	ms
(During Low Battery)	Between Pulses	t_{off}	32	40	48	s

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 — TYPICAL LED OUTPUT I-V CHARACTERISTIC

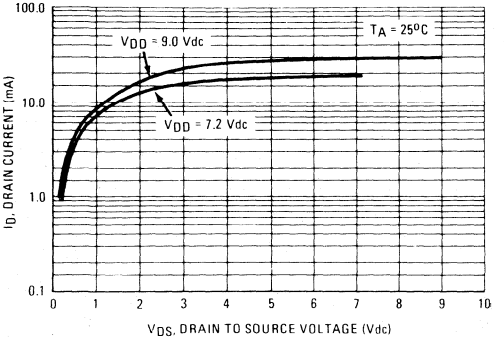
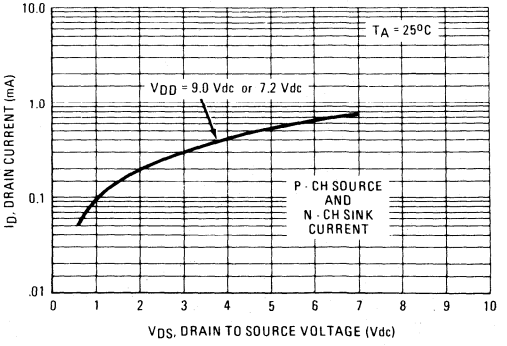
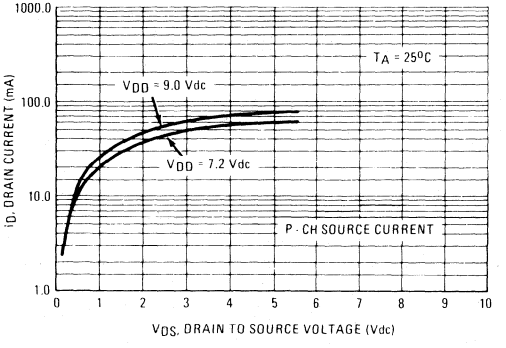


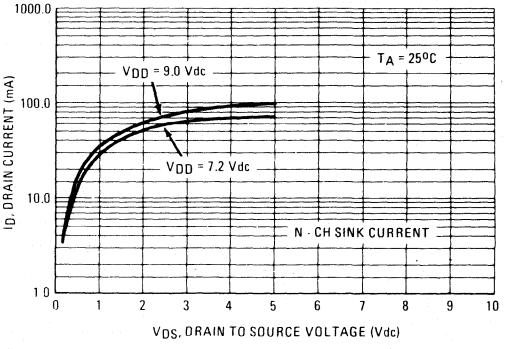
FIGURE 2 — TYPICAL COMPARATOR OUTPUT I-V CHARACTERISTIC



7

FIGURE 3 — TYPICAL P HORN DRIVER OUTPUT I-V CHARACTERISTIC





DEVICE OPERATION

TIMING

The internal oscillator of the MC14468 operates with a period of 1.67 seconds during no-smoke conditions. Each 1.67 seconds, internal power is applied to the entire IC and a check is made for smoke, except during LED pulse, Low Battery Alarm Chirp, or Horn Modulation (in smoke). Every 24 clock cycles a check is made for low battery by comparing V_{DD} to an internal zener voltage. Since very small currents are used in the oscillator, the oscillator capacitor should be of a low leakage type.

DETECT CIRCUITRY

If smoke is detected, the oscillator period becomes 40 ms and the piezoelectric horn oscillator circuit is enabled. The horn output is modulated 160 ms on, 80 ms off. During the off time, smoke is again checked and will inhibit further horn output if no smoke is sensed. During local smoke conditions the low battery alarm is inhibited, but the LED pulses at a 1.0 Hz rate. In remote smoke, the LED is inhibited as well.

An active guard is provided on both pins adjacent to the detect input. The voltage at these pins will be within 100 mV of the input signal. This will keep surface leakage currents to a minimum and provide a method of measuring the input voltage without loading the ionization chamber. The active guard op amp is not power strobed and thus gives constant protection from surface leakage currents. Pin 15 (the Detect input) has internal diode protection against static damage.

INTERCONNECT

The I/O (Pin 2), in combination with V_{SS}, is used to interconnect up to 40 remote units for common signaling. A Local Smoke condition activates a current limited output driver, thereby signaling Remote Smoke to interconnected units. A small current sink improves noise immunity during non-smoke conditions. Remote units at lower voltages do not draw excessive current from a sending unit at a higher voltage. The I/O is disabled for three oscillator cycles after power up, to eliminate false alarming of remote units when the battery is changed.

SENSITIVITY/LOW BATTERY THRESHOLDS

Both the sensitivity threshold and the low battery voltage levels are set internally by a common voltage divider connected between V_{DD} and V_{SS}. These voltages can be altered by external resistors connected from pins 3 or 13 to either V_{DD} or V_{SS}. There will be a slight interaction here due to the common voltage divider network. The sensitivity threshold can also be set by adjusting the smoke chamber ionization source.

TEST MODE

Since the internal op amps and comparators are power strobed, adjustments for sensitivity or low battery level could be difficult and/or time-consuming. By forcing Pin 12 to V_{SS}, the power strobing is bypassed and the output, Pin 1, constantly shows smoke/no smoke. Pin 1 = V_{DD} for smoke. In this mode and during the 10 ms power strobe, chip current rises to approximately 50 μA.

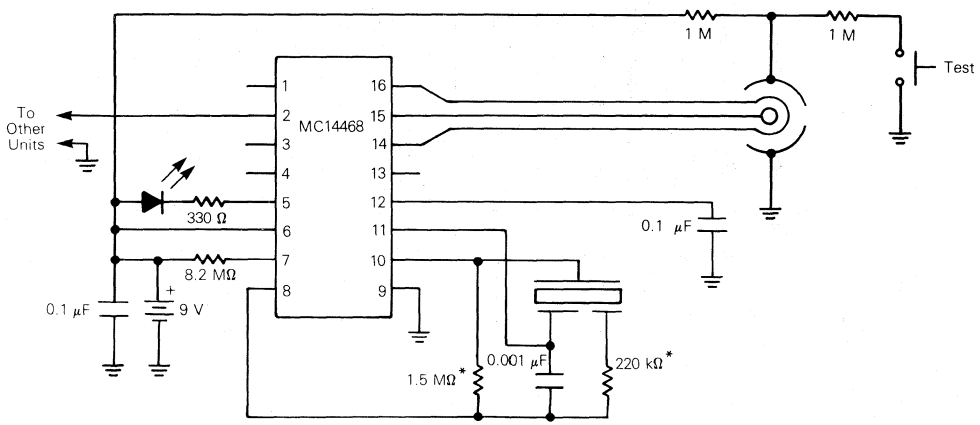
LED PULSE

The 9-volt battery level is checked every 40 seconds during the LED pulse. The battery is loaded via a 10 mA pulse for 10 ms. If the LED is not used, it should be replaced with an equivalent resistor such that the battery loading remains at 10 mA.

HYSTERESIS

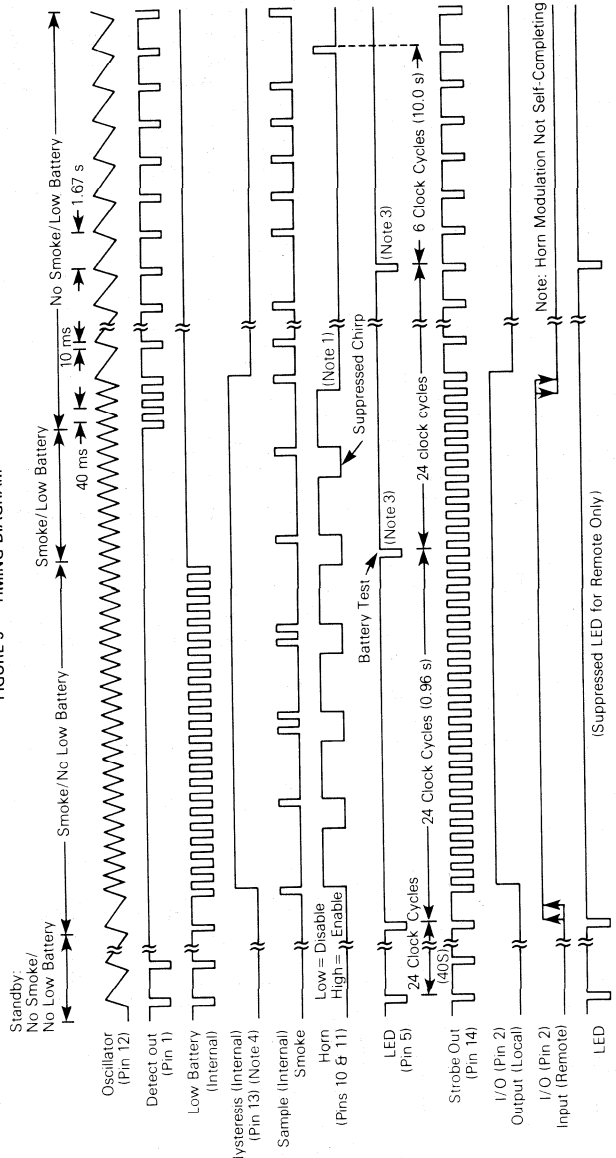
When smoke is detected, the resistor/divider network that sets sensitivity is altered to increase sensitivity. This yields approximately 100 mV of hysteresis and reduces false triggering.

FIGURE 4 — TYPICAL APPLICATION AS IONIZATION SMOKE DETECTOR



*NOTE: Component values may change depending on type of piezoelectric horn used.

FIGURE 5 — TIMING DIAGRAM

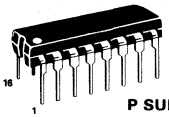


NOTES: 1. Horn modulation is self-completing. When going from smoke to no smoke, the alarm condition will terminate only when horn is off.
2. Comparators are strobed on once per clock cycle (1.67 s for no smoke, 40 ms for smoke).
3. Low battery comparator information is latched only during LED pulse.
4. ~ 100 mV p-p swing.

MC14470

Advance Information

Ionization Smoke Detector with I/O
For Line-Powered Applications



P SUFFIX
PLASTIC DIP
CASE 648

ORDERING INFORMATION

MC14470P	Plastic DIP

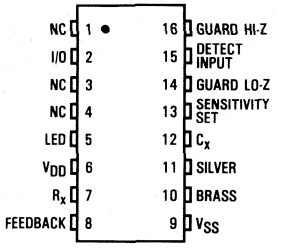
The CMOS MC14470 is a smoke detector component containing both analog and digital circuitry. The IC is used with an ionization chamber. When detection occurs, a pulsating alarm is sounded via on-chip push-pull drivers and an external piezoelectric transducer.

An on-chip driver causes an external LED lamp to be illuminated when the MC14470 is receiving power in the standby mode. The lamp remains illuminated if a remote smoke condition is sensed at the I/O pin. During a local smoke condition, the lamp is extinguished.

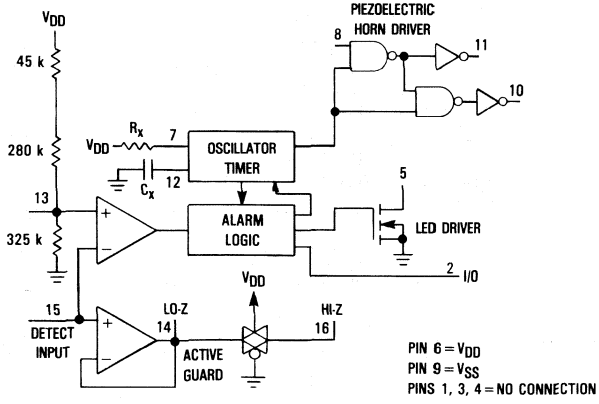
The I/O pin, in combination with V_{SS}, can be used to interconnect up to 40 units for common signaling. An on-chip current sink provides noise immunity when the I/O is an input. A local-smoke condition activates the short-circuit-protected I/O driver, thereby signaling remote smoke to the interconnected units. Additionally, the I/O pin can be used to activate escape lights, enable auxiliary or remote alarms, and/or initiate auto-dialers.

- Complies with the UL217 and UL268 Specifications
- Operating Voltage Range: 6 to 12 V
- Direct Interface to Ionization Chamber
- Electrostatic Discharge (ESD) and Latch Up Protection Circuitry on All Pins
- Detect Threshold is Internally Set
- Power-On Reset (POR) Prevents False Alarms on Power Up

PIN ASSIGNMENT



BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +15	V
V_{in}	DC Input Voltage, All Inputs Except Pin 8	−0.25 to V_{DD}+0.25	V
I_{in}	DC Input Current, per Pin, Except Pin 15 = 1 mA	±10	mA
I_{out}	DC Output Current, per Pin	±30	mA
T_{stg}	Storage Temperature	−55 to +125	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$ except for pin 8, which can exceed V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	7.2 to 12	V
C_x	Timing Capacitor (Can Use Up to ±20% Tolerance)	0.1	μF
R_x	Timing Resistor (Can Use Up to ±20% Tolerance)	8.2	MΩ
T_A	Operating Temperature	−10 to +60	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, Voltages Referenced to V_{SS})

Symbol	Parameter		Test Condition	V_{DD} V	Min	Max	Unit
V_{DD}	Power Supply Voltage Range			—	6.0	12	V
I_{DD}	Average Operating Supply Current		R_x = 8.20 MΩ	9.0 12.0	— —	9.0 12.0	μA
V_{in}	Input Voltage Range	Feedback		—	−10	V_{DD}+10	V
V_{ref}	Smoke Comparator Reference Voltage			—	47	53	%V_{DD}
V_{hys}	Hysteresis Voltage		Alarm Condition, Pin 13	9.0	75	150	mV
V_{CM}	Common Mode Voltage Range	Detect Input		—	0.6	V_{DD}−2	V
V_{OS}	Offset Voltage	Active Guard Detect Comparator	$V_{in} = V_{DD}/2$	9.0 9.0	— —	±100 ±50	mV
I_{in}	Input Leakage Current	Feedback	$V_{in} = V_{DD}$ or V_{SS}	9.0	—	±0.1	μA
		Detect Input Detect Input @ 50°C	$V_{in} = V_{DD}$ or V_{SS}	9.0	— —	±1 ±5	pA
C_{in}	Input Capacitance			—	—	TBD	pF
V_{IL}	Input Voltage	I/O	No Remote Smoke	—	—	1.5	V
V_{IH}			Remote Smoke		3.0	—	
I_{IH}	Pull-Down Current	I/O	No Local Smoke $V_{in} = V_{DD}$−2 V	—	25	100	μA
I_{OH}	Output Current	I/O	Local Smoke $V_{out} = V_{DD}$−2 V	—	−4.0	−16	mA
V_{OH}	High-Level Output Voltage	Piezoelectric Horn Drivers	I_{out} = −16 mA	7.2	6.3	—	V
V_{OL}	Low-Level Output Voltage	Piezoelectric Horn Drivers	I_{out} = 16 mA	7.2	—	0.9	V
V_{OL}	Low-Level Output Voltage	LED Driver	I_{out} = 10 mA	7.2	—	3.0	V
Z_{out}	Output Impedance, Active Guard	Lo-Z, Pin 14 Hi-Z, Pin 16		9.0 9.0	— —	10 1000	kΩ

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{DD} = 9.0 V, C_x = 0.10 μF, R_x = 8.20 MΩ, See Figure 4)

Symbol	Parameter	Test Condition		Min	Max	Unit
$1/f_{osc}$	Oscillator Period	Free-Running Sawtooth Measured at Pin 12	No Alarm	1.34	2.0	s
			Alarm	32	48	ms
t_r	Oscillator Rise Time			8	12	ms
$t_{w(Horn)}$	Horn Pulse Width	During Alarm Condition	On	120	208	ms
			Off	60	104	

DEVICE OPERATION

TIMING

The internal oscillator of the MC14470 operates with a nominal period of 1.67 seconds during non-alarm conditions. Each 1.67 seconds, internal power is applied to the entire IC and a check is made for an alarm state, except during horn modulation (in alarm condition).

The oscillator capacitor should be of a low-leakage type because of the low-current oscillator employed. Lastly, the tolerance of the external timing components must be no greater than ±20%.

DETECT CIRCUITRY

If smoke is detected, the oscillator period becomes approximately 40 ms and the piezoelectric horn oscillator circuit is enabled. The horn output is modulated approximately 160 ms on, 80 ms off. During the off time, the smoke condition is again checked and further horn output is inhibited if a smoke condition is not sensed.

The LED tied to pin 5 is normally on to indicate that the device is receiving power. When a remote smoke condition is sensed by the I/O pin, the LED remains lit. During a local smoke condition, the LED is extinguished.

An active guard is provided on both pins adjacent to the detect input. The voltage at these pins is within 100 mV of the input signal. This keeps surface leakage currents to a minimum and provides a method of measuring the input voltage without loading the detect input pin. The active guard op amp is not power strobed and thus gives constant protection from surface leakage currents. The Detect Input has internal diode protection against static damage.

SENSITIVITY THRESHOLD

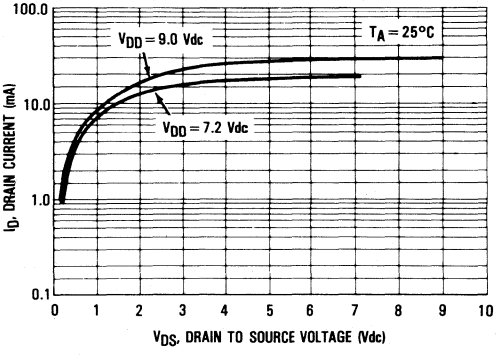
The sensitivity threshold is set internally by a voltage divider connected between V_{DD} and V_{SS}. The voltage can be altered by an external resistor connected from pin 13 to either V_{DD} or V_{SS}. The sensitivity threshold can also be set by adjusting the smoke chamber ionization source.

INTERCONNECT

The I/O (Pin 2), in combination with V_{SS}, is used to interconnect up to 40 remote units for common signaling. A Local Smoke condition activates a current limited output driver, thereby signaling Remote Smoke to interconnected units. A small current sink improves noise immunity during non-smoke conditions. Remote units at lower voltages do not draw excessive current from a sending unit at a higher voltage. The I/O is disabled for three oscillator cycles after power up, to eliminate false alarming of remote units.

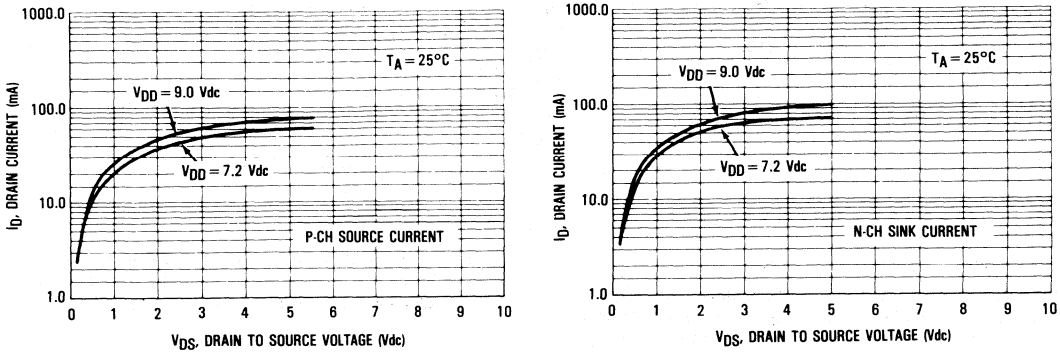
HYSTERESIS

When an alarm is detected, the resistor/divider network that sets sensitivity is altered to increase sensitivity. This yields approximately 100 mV of hysteresis and reduces intermittent triggering.



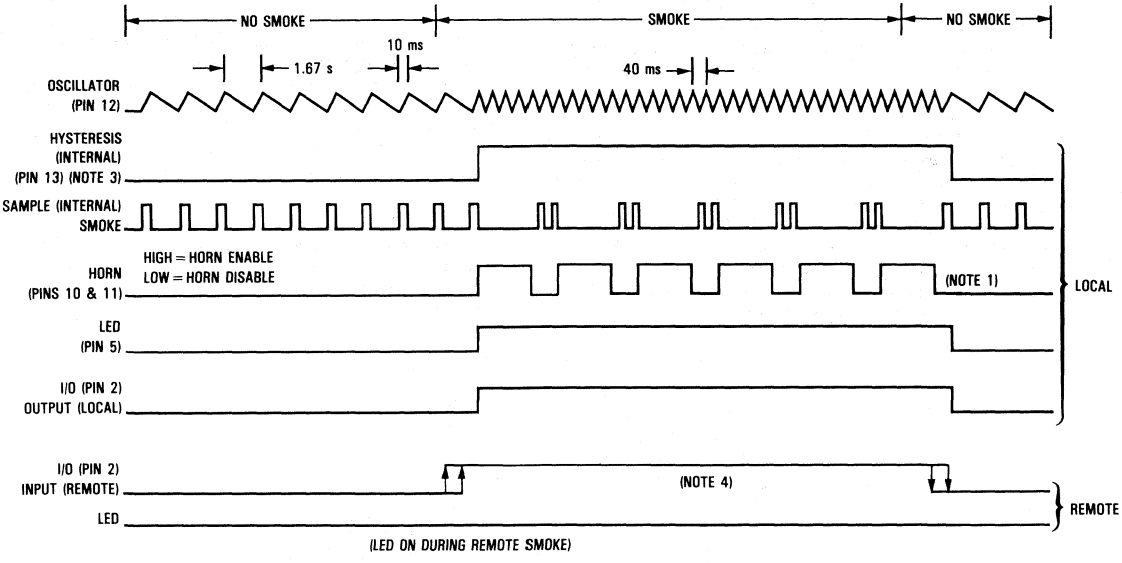
NOTE: This "typical" graph is not to be used for design purposes but is intended as an indication of the IC's potential performance.

Figure 1. Typical LED Output I-V Characteristic



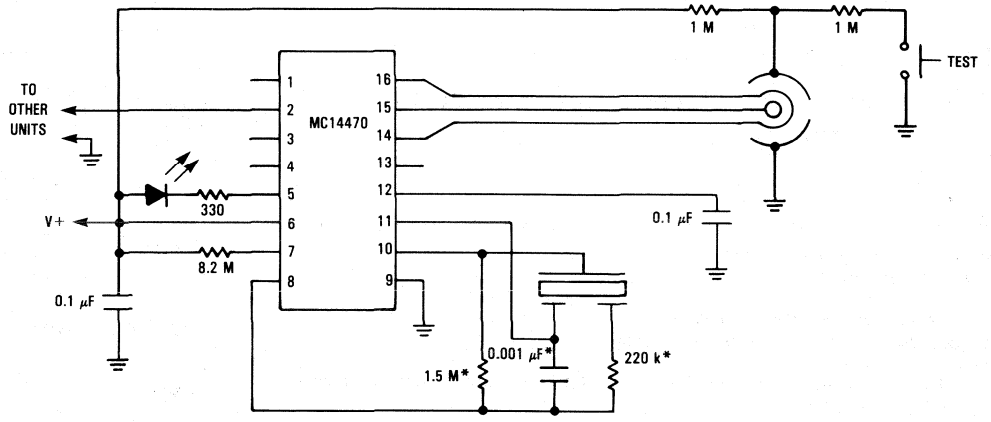
NOTE: These "typical" graphs are not to be used for design purposes but are intended as indications of the IC's potential performance.

Figure 2. Typical P Horn Driver Output I-V Characteristic



NOTES:
1. Horn modulation is self-completing. When going from smoke to no smoke, the alarm condition will terminate only when horn is off.
2. Comparators are strobed on once per clock cycle (1.67 s for no smoke, 40 ms for smoke).
3. ~100 mVp-p swing.
4. Horn modulation is not self-completing when going from remote smoke to no smoke.

Figure 3. Timing Diagram



*NOTE: Component values may change depending on type of piezoelectric horn used.

Figure 4. Typical Application as Ionization Smoke Detector

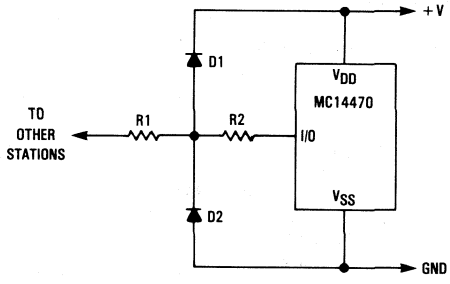


Figure 5. Protection Circuit

LINE-POWERED MC14470 PROTECTION CIRCUIT

During system installation of stations powered from the ac line, the MC14470 can be damaged if the live hot conductor and I/O conductor come in contact before the neutral conductor. The circuit of Figure 5 prevents such damage, while enhancing the ESD (electrostatic discharge) immunity of the system.

The following values may be used for the components:

D1 = D2 = 1N5393 (1.5 A, 200 V)

R1 = 1000 ohms ± 10% = 900 to 1100 ohms

R2 = 47 ohms ± 10% = 42.3 to 51.7 ohms

Assuming a 9.0 V supply, the supporting calculations (all worst case) are:

AC line voltage = 130 V_{rms} = 184 V_{peak}

Therefore,

$I_{diode} = V_{peak}/R1 = 184/900 = 204$ mA

$I_{latchup} = (V_{diode} - V_{IC})/R2 = (1.0 - 0.55)/42.3 = 11$ mA

Fanout:

$V_{remote} = IR = 100\ \mu A \times (51.7 + 1100) = 0.12$ V

Therefore,

Logic High = 3.0 + 0.12 = 3.12 V minimum

At 4 mA drive, MC14470 provides $V_{DD} - 2 = 7$ V output

Max drop allowable = V_R local = 7 − 3.12 = 3.88 V

Under ideal conditions,

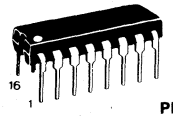
Fanout = 3.88 V/[(1100 + 51.7) 100 μA] = 33 stations

NOTE: Interconnect wiring losses and noise reduces fanout.

MC14578

Advance Information

Micro-Power Comparator plus Voltage Follower
CMOS



P SUFFIX
PLASTIC DIP
CASE 648

D SUFFIX
SOG
CASE 751B

ORDERING INFORMATION

MC14578P	Plastic DIP
MC14578D	SOG Package

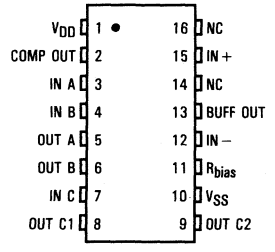
The MC14578 is an analog building block consisting of a very-high input impedance comparator. The voltage follower allows monitoring the noninverting input of the comparator without loading.

Four enhancement-mode MOSFETs are also included on chip. These FETs can be externally configured as open-drain or totem-pole outputs. The drains have on-chip static-protecting diodes. Therefore, the output voltage must be maintained between V_{SS} and V_{DD}.

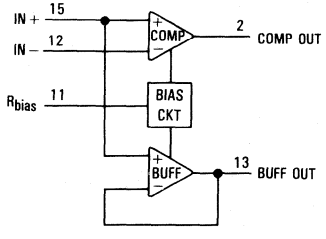
The chip requires one external component. A 3.9 MΩ ± 10% resistor must be connected from the R_{bias} pin to V_{DD}.

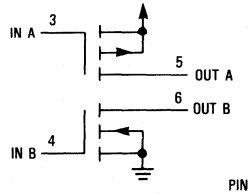
- Applications:
  - Pulse Shapers
  - Threshold Detectors
  - Low-Battery Detectors
  - Line-Powered Smoke Detectors
  - Liquid/Moisture Sensors
- DIP Complies with the UL217 and UL268 Specifications
- Operating Voltage Range: 3.5 to 14 V
- Operating Temperature Range: −30° to 70°C
- Input Current (IN+ Pin): ±1 pA @ 25°C (DIP Only)
- Quiescent Current: 10 μA @ 25°C
- Electrostatic Discharge (ESD) Protection Circuitry on All Pins
- Chip Complexity: 26 FETs

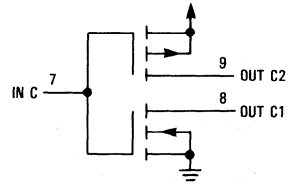
PIN ASSIGNMENT



LOGIC DETAIL







PIN 1 = V_{DD}
PIN 10 = V_{SS}
PINS 14, 16 = NO CONNECTION

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS* (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +14.0	V
V_{in}	DC Input Voltage	−0.5 to V_{DD}+0.5	V
V_{out}	DC Output Voltage	−0.5 to V_{DD}+0.5	V
I_{in}	DC Input Current, Except IN+	±10	mA
I_{in}	DC Input Current, IN+	±1	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{DD}	DC Supply Current, V_{DD} and V_{SS} Pins	±50	mA
P_D	Power Dissipation, per Package	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

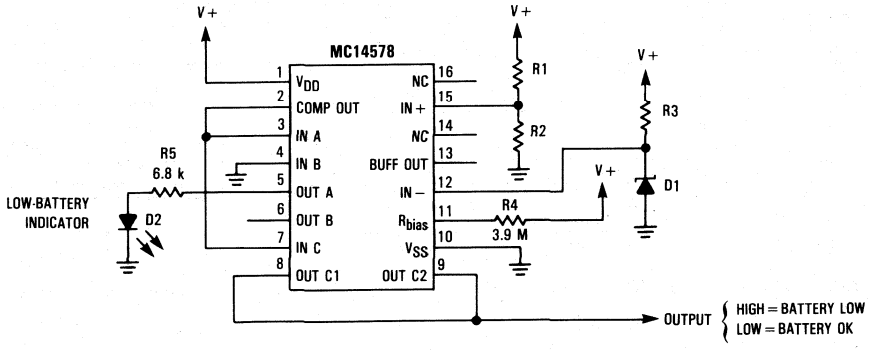
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, R_{bias} = 3.9 MΩ to V_{DD}, T_A = −30° to 70°C Unless Otherwise Indicated)

Symbol	Parameter	Test Condition	V_{DD} V	Guaranteed Limit	Unit
V_{DD}	Power Supply Voltage Range		—	3.5 to 14.0	V
V_{IL}	Maximum Low-Level Input Voltage, MOSFETs Wired as Inverters; i.e., IN A tied to IN B, OUT A to OUT B, OUT C1 to OUT C2	V_{out} = 9.0 V, $\|I_{out}\| < 1$ μA	10.0	2.0	V
V_{IH}	Minimum High-Level Input Voltage, MOSFETs Wired as Inverters; i.e., IN A tied to IN B, OUT A to OUT B, OUT C1 to OUT C2	V_{out} = 1.0 V, $\|I_{out}\| < 1$ μA	10.0	8.0	V
V_{IO}	Comparator Input Offset Voltage	T_A = 25°C, Over Common Mode Range	10.0	±50	mV
		T_A = 0° to 50°C, Over Common Mode Range	3.5 to 14.0	±75	
V_{CM}	Comparator Common Mode Voltage Range		3.5 to 14.0	0.7 to V_{DD} − 1.5	V
V_{OL}	Maximum Low-Level Comparator Output Voltage	IN+: $V_{in} = V_{SS}$, IN−: $V_{in} = V_{DD}$, I_{out} = 30 μA	10.0	0.5	V
V_{OH}	Minimum High-Level Comparator Output Voltage	IN+: $V_{in} = V_{DD}$, IN−: $V_{in} = V_{SS}$, I_{out} = −30 μA	10.0	9.5	V
V_{OO}	Buffer Amp Output Offset Voltage	R_{load} = 10 MΩ to V_{DD} or V_{SS}, Over Common Mode Range	—	±100	mV
V_{OL}	Maximum Low-Level Output Voltage, MOSFETs Wired as Inverters; i.e., IN A tied to IN B, OUT A to OUT B, OUT C1 to OUT C2	OUT C1, OUT C2: I_{out} = 1.1 mA	10.0	0.5	V
		OUT A, OUT B: I_{out} = 270 μA	10.0	0.5	
V_{OH}	Minimum High-Level Output Voltage, MOSFETs Wired as Inverters; i.e., IN A tied to IN B, OUT A to OUT B, OUT C1 to OUT C2	OUT C1, OUT C2: I_{out} = −1.1 mA	10.0	9.5	V
		OUT A, OUT B: I_{out} = −270 μA	10.0	9.5	
I_{in}	Maximum Input Leakage Current — IN+ (DIP Only)	T_A = 25°C, 40% R.H., $V_{in} = V_{SS}$ or V_{DD}	10.0	±1	pA
	IN+ (DIP Only)	T_A = 50°C, $V_{in} = V_{SS}$ or V_{DD}	10.0	±6	
	IN+ (SOG), IN A, IN B, IN C, IN−	$V_{in} = V_{SS}$ or V_{DD}	10.0	±40	nA
I_{OZ}	Maximum Off-State MOSFET Leakage Current	IN A, IN C: $V_{in} = V_{DD}$, OUT A, OUT C2: $V_{out} = V_{SS}$ or V_{DD}	10.0	±100	nA
		IN B, IN C: $V_{in} = V_{SS}$, OUT B, OUT C1: $V_{out} = V_{SS}$ or V_{DD}	10.0	±100	
I_{DD}	Maximum Quiescent Current	T_A = 25°C, IN A, IN B, IN C: $V_{in} = V_{SS}$ or V_{DD}, $\|V_{IN+} - V_{IN-}\|$ = 100 mV, I_{out} = 0 μA	10.0	10	μA
C_{in}	Maximum Input Capacitance — IN+	f = 1 kHz	—	5	pF
	Other Inputs		—	15	

APPLICATIONS INFORMATION



NOTE: IN+ and IN− have very-high input impedance. Interconnect to these pins should be as short as possible.

Figure 1. Low-Battery Detector

EXAMPLE VALUES

D1: 1N4683 Zener Diode (Available From Motorola)

D2: HLMP-D150, HLMP-K150, or HLMP-Q150 Low-Current LED (Hewlett-Packard Part Number or Equivalent)

R1	R2	R3	Nominal Trip Point
470 kΩ	1.3 MΩ	20 kΩ	4.08 V
820 kΩ	1.2 MΩ	39 kΩ	5.05 V
1.2 MΩ	1.2 MΩ	62 kΩ	6.00 V

Near the switchpoint, the comparator output in the circuit of Figure 1 may chatter or oscillate. This oscillation appears on the signal labelled OUTPUT. In come cases, the oscillation in the transition region will not cause problems. For example, an MPU reading OUTPUT could sample the signal two or three times to ensure a solid level is attained. But, in a low battery detector, this probably is not necessary.

To eliminate comparator chatter, hysteresis can be added as shown in Figure 2. The circuit of Figure 2 requires slightly more operating current than the Figure 1 arrangement.

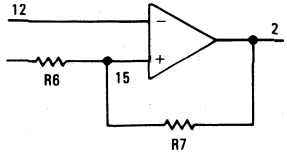


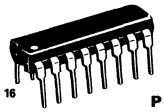
Figure 2. Adding Hysteresis

MC145010

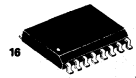
Advance Information

Photoelectric Smoke Detector with I/O

For Battery-Powered Applications



P SUFFIX
PLASTIC DIP
CASE 648



DW SUFFIX
SOG
CASE 751G

ORDERING INFORMATION

MC145010P	Plastic DIP
MC145010DW	SOG Package

The CMOS MC145010 is an advanced smoke detector component containing sophisticated very-low-power analog and digital circuitry. The IC is used with an infrared photoelectric chamber. Detection is accomplished by sensing scattered light from minute smoke particles or other aerosols. When detection occurs, a pulsating alarm is sounded via on-chip push-pull drivers and an external piezoelectric transducer.

The variable-gain photo amplifier allows direct interface to IR detectors (photodiodes). Two external capacitors C1 and C2, C1 being the larger, determine the gain settings. Low gain is selected by the IC during most of the standby state. Medium gain is selected during a local-smoke condition. High gain is used during pushbutton test. During standby, the special monitor circuit which periodically checks for degraded chamber sensitivity uses high gain, also.

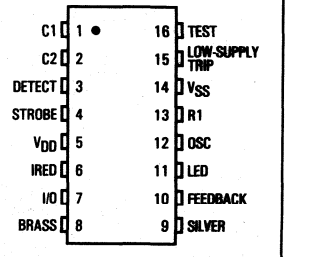
The I/O pin, in combination with V_{SS}, can be used to interconnect up to 40 units for common signaling. An on-chip current sink provides noise immunity when the I/O is an input. A local-smoke condition activates the short-circuit-protected I/O driver, thereby signaling remote smoke to the interconnected units. Additionally, the I/O pin can be used to activate escape lights, enable auxiliary or remote alarms, and/or initiate auto-dialers.

While in standby, the low-supply detection circuitry conducts periodic checks using a pulsed load current from the LED pin. The trip point is set using two external resistors. The supply for the MC145010 can be a 9 V battery.

A visible LED flash accompanying a pulsating audible alarm indicates a local-smoke condition. A pulsating audible alarm with no LED flash indicates a remote-smoke condition. A beep or chirp occurring virtually simultaneously with an LED flash indicates a low-supply condition. A beep occurring half-way between LED flashes indicates degraded chamber sensitivity. A low-supply condition does not affect the smoke detection capability if $V_{DD} \geq 6$ V. Therefore, the low-supply condition and degraded chamber sensitivity can be further distinguished by performing a pushbutton (chamber) test.

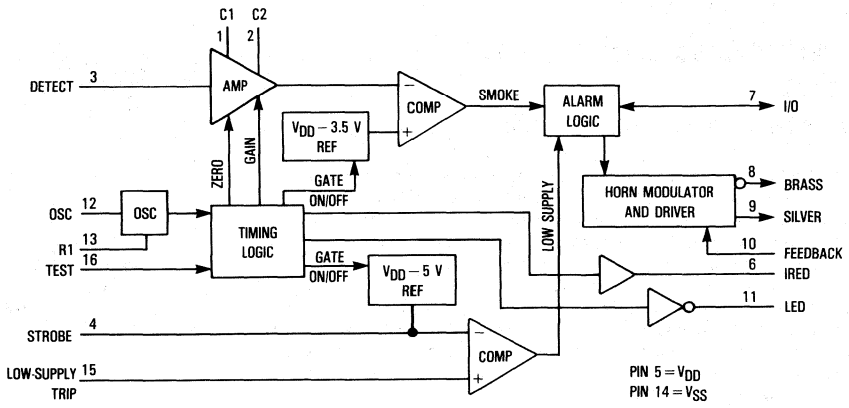
- Complies with the UL217 and UL268 Specifications
- Operating Voltage Range: 6 to 12 V
- Operating Temperature Range: − 10 to 60°C
- Average Supply Current: 12 μA
- Power-On Reset Places IC in Standby Mode (Non-Alarm State)
- Electrostatic Discharge (ESD) and Latch Up Protection Circuitry on All Pins
- Chip Complexity: 2000 FETs, 12 NPNs, 16 Resistors, and 10 Capacitors

PIN ASSIGNMENT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +12.0	V
V_{in}	DC Input Voltage C1, C2, Detect Osc, Low-Supply Trip I/O Feedback Test	−0.25 to V_{DD} + 0.25 −0.25 to V_{DD} + 0.25 −0.25 to V_{DD} + 10 −15 to +25 −1.0 to V_{DD} + 0.25	V
I_{in}	DC Input Current, per Pin	±10	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{DD}	DC Supply Current, V_{DD} and V_{SS} Pins	+25/−150	mA
P_D	Power Dissipation in Still Air, 5 seconds Continuous	1200† 350★	mW
T_{stg}	Storage Temperature	−55 to +125	°C
T_L	Lead Temperature, 1 mm from Case for 10 seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables.

†Derating: −12 mW/°C from 25° to 60°C.

★Derating: −3.5 mW/°C from 25° to 60°C.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$ except for the I/O, which can exceed V_{DD}, and the Test input, which can go below V_{SS}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs and/or an unused I/O must be left open.

ELECTRICAL CHARACTERISTICS (T_A = −10 to 60°C Unless Otherwise Indicated, Voltages Referenced to V_{SS})

Symbol	Parameter		Test Condition	V_{DD} V	Min	Max	Unit
V_{DD}	Power Supply Voltage Range			—	6	12	V
V_{TH}	Supply Threshold Voltage, Low-Supply Alarm		Low-Supply Trip: $V_{in} = V_{DD}/3$	—	6.5	7.8	V
I_{DD}	Average Operating Supply Current (per Package)		Standby Configured per Fig. 5	12.0	—	12	μA
i_{DD}	Peak Supply Current (per Package)		During Strobe On, IRED Off Configured per Fig. 5	12.0	—	2.0	mA
			During Strobe On, IRED On Configured per Fig. 5	12.0	—	3.0	
V_{IL}	Low-Level Input Voltage	I/O		9.0	—	1.5	V
		Feedback		9.0	—	2.7	
		Test		9.0	—	7.0	
V_{IH}	High-Level Input Voltage	I/O		9.0	3.2	—	V
		Feedback		9.0	6.3	—	
		Test		9.0	8.5	—	
I_{in}	Input Current	Osc, Detect	$V_{in} = V_{SS}$ or V_{DD}	12.0	—	±100	nA
		Low-Supply Trip	$V_{in} = V_{SS}$ or V_{DD}	12.0	—	±100	
		Feedback	$V_{in} = V_{SS}$ or V_{DD}	12.0	—	±100	
I_{IL}	Low-Level Input Current	Test	$V_{in} = V_{SS}$	12.0	—	−1	μA
I_{IH}	Pull-Down Current	Test	$V_{in} = V_{DD}$	9.0	0.5	10	μA
		I/O	No Local Smoke, $V_{in} = V_{DD}$	9.0	25	100	
			No Local Smoke, V_{in} = 17 V	12.0	—	140	
V_{OL}	Low-Level Output Voltage	LED	I_{out} = 10 mA	6.5	—	0.6	V
		Silver, Brass	I_{out} = 16 mA	6.5	—	1.0	
V_{OH}	High-Level Output Voltage	Silver, Brass	I_{out} = −16 mA	6.5	5.5	—	V
V_{out}	Output Voltage (For Line Regulation, see Pin Descriptions)	Strobe	Inactive, I_{out} = −1 μA	—	$V_{DD}-0.1$	—	V
			Active, I_{out} = 100 μA to 500 μA (Load Regulation)	9.0	$V_{DD}-4.4$	$V_{DD}-5.6$	
		IRED	Inactive, I_{out} = 1 μA	—	—	0.1	
			Active, I_{out} = 6 mA (Load Regulation)	9.0	2.25*	3.75*	
I_{OH}	High-Level Output Current	I/O	Local Smoke, $V_{out} = 4.5$ V	6.5	−4	—	mA
			Local Smoke, $V_{out} = V_{SS}$ (Short Circuit Current)	12.0	—	−16	
I_{OZ}	Off-State Output Leakage Current	LED	$V_{out} = V_{SS}$ or V_{DD}	12.0	—	±1	μA
V_{IC}	Common Mode Voltage Range	C1, C2, Detect	Local Smoke, Pushbutton Test, or Chamber Sensitivity Test	—	$V_{DD}-4$	$V_{DD}-2$	V
V_{ref}	Smoke Comparator Reference Voltage	Internal	Local Smoke, Pushbutton Test, or Chamber Sensitivity Test	—	$V_{DD}-3.08$	$V_{DD}-3.92$	V

*T_A = 25°C only.

AC ELECTRICAL CHARACTERISTICS (Reference Timing Diagram Figures 3 and 4)
($T_A = 25°C, V_{DD} = 9.0$ V, Component Values from Figure 5: R1 = 100.0 KΩ, C3 = 1500.0 pF, R2 = 10.0 MΩ)

No.	Symbol	Parameter	Test Condition	Min	Max	Unit
1	$1/f_{osc}$	Oscillator Period	Free-Running Sawtooth Measured at Pin 12	9.5	11.5	ms
2	t_{LED}	LED Pulse Period	No Local Smoke, and No Remote Smoke	38.9	47.1	s
3			Remote Smoke, but No Local Smoke	None		
4			Local Smoke or Pushbutton Test	0.60	0.74	
5	$t_{w(LED)}$, $t_{w(stb)}$	LED Pulse Width and Strobe Pulse Width		9.5	11.5	ms
6	t_{IRED}	IRED Pulse Period	Smoke Test	9.67	11.83	s
7			Chamber Sensitivity Test, without Local Smoke	38.9	47.1	
8			Pushbutton Test	0.302	0.370	
9	$t_{w(IRED)}$	IRED Pulse Width		94	116	μs
10	t_r	IRED Rise Time		–	30	μs
	t_f	IRED Fall Time		–	200	
11	t_{mod}	Silver and Brass Modulation Period	Local or Remote Smoke	297	363	ms
11, 12	t_{on}/t_{mod}	Silver and Brass Duty Cycle	Local or Remote Smoke	73	77	%
13	t_{CH}	Silver and Brass Chirp Pulse Period	Low Supply or Degraded Chamber Sensitivity	38.9	47.1	s
14	$t_{w(CH)}$	Silver and Brass Chirp Pulse Width	Low Supply or Degraded Chamber Sensitivity	9.5	11.5	ms
15	t_{RR}	Rising Edge on I/O to Smoke Alarm Response Time	Remote Smoke, No Local Smoke	–	800	ms
16	t_{stb}	Strobe Pulse Period	Smoke Test	9.67	11.83	s
17			Chamber Sensitivity Test, without Local Smoke	38.9	47.1	
18			Low Supply Test, without Local Smoke	38.9	47.1	
19			Pushbutton Test	0.302	0.370	

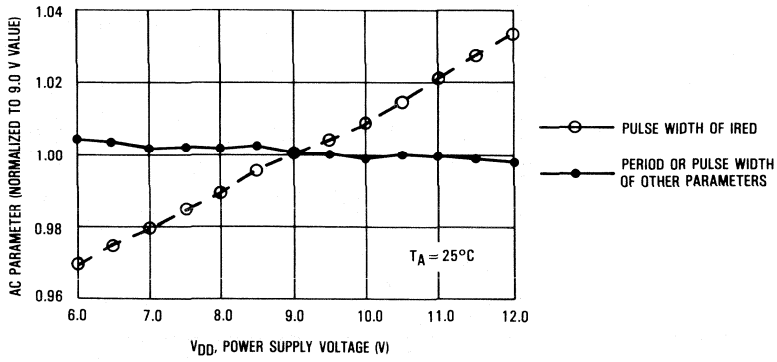
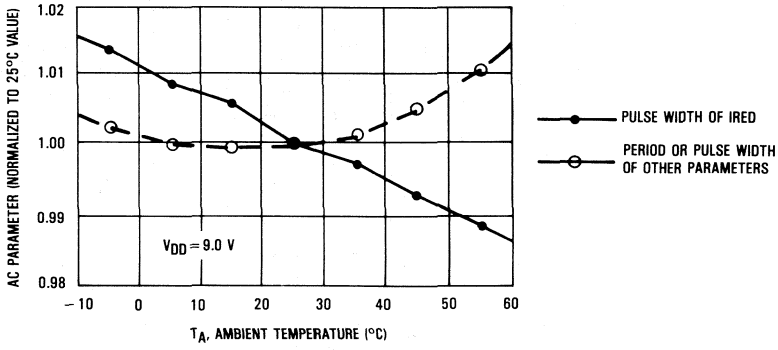
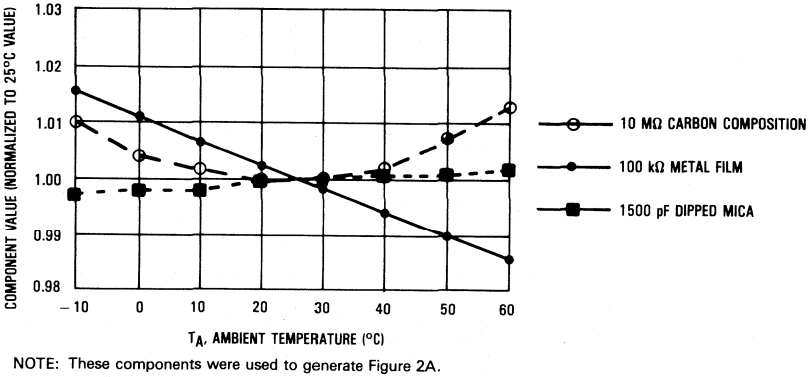


Figure 1. AC Characteristics versus Supply



NOTE: Includes external component variations. See Figure 2B.

Figure 2A. AC Characteristics versus Temperature



NOTE: These components were used to generate Figure 2A.

Figure 2B. RC Component Variation Over Temperature

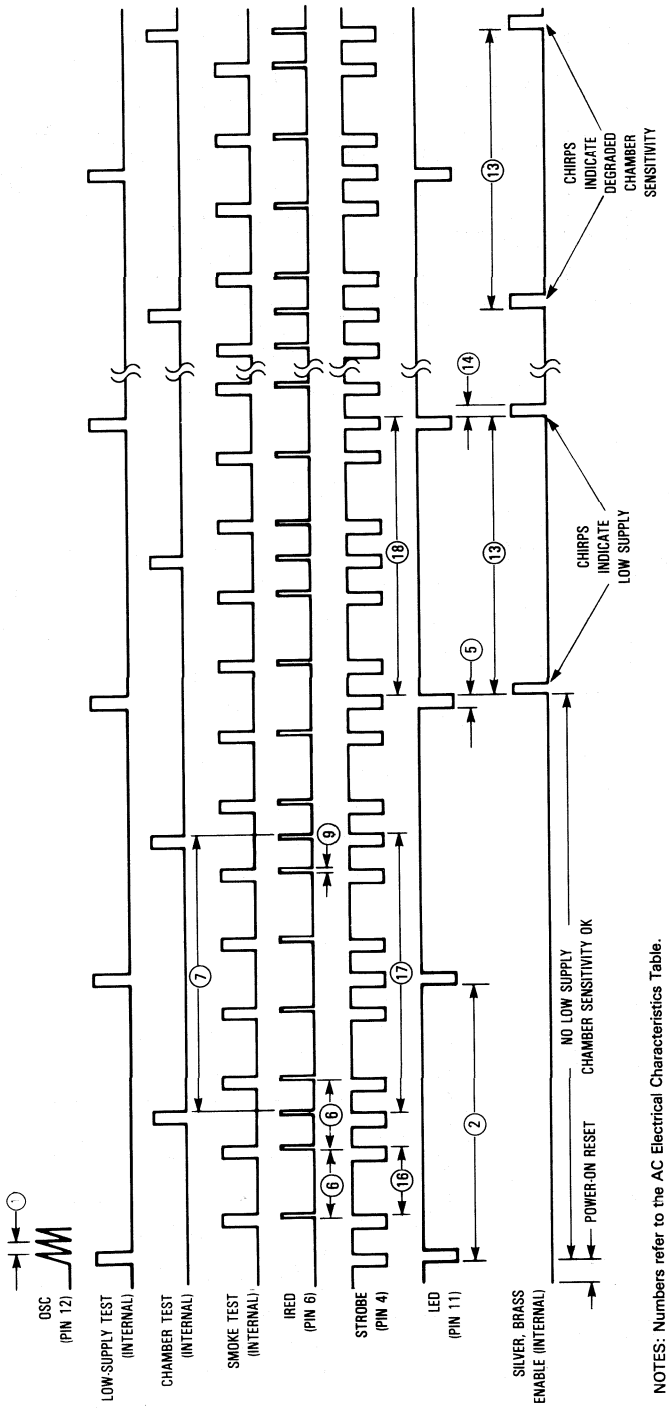
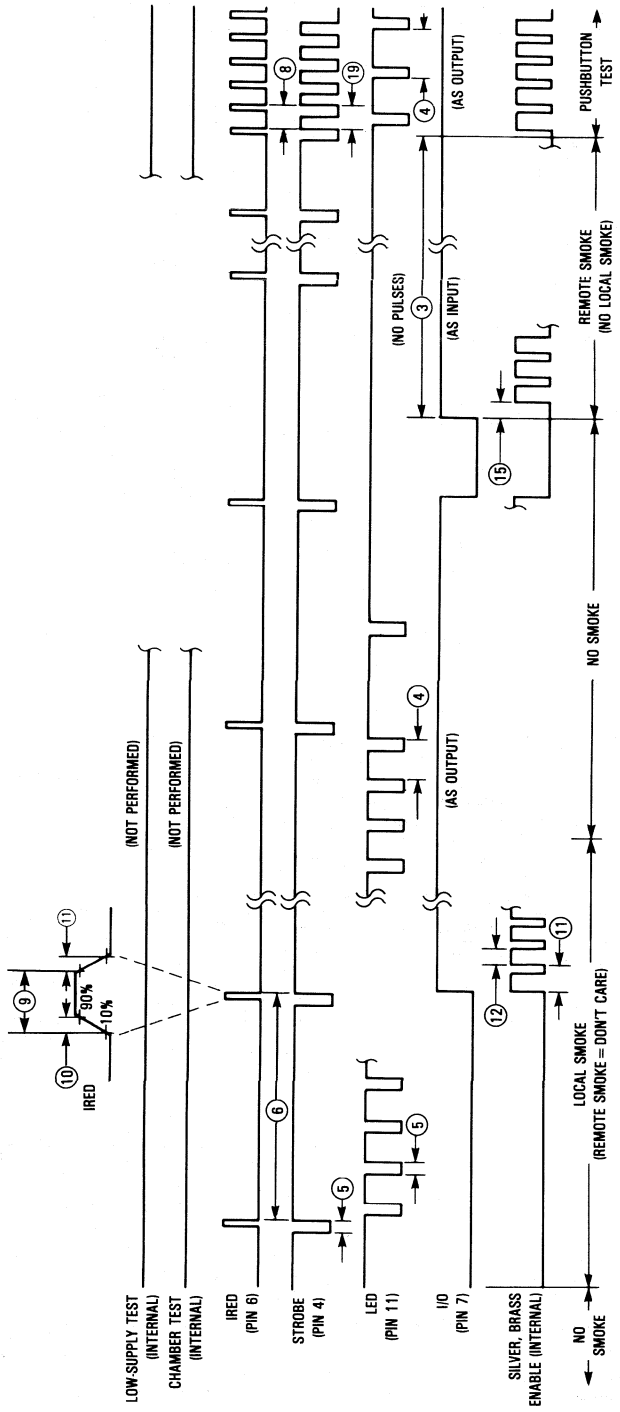


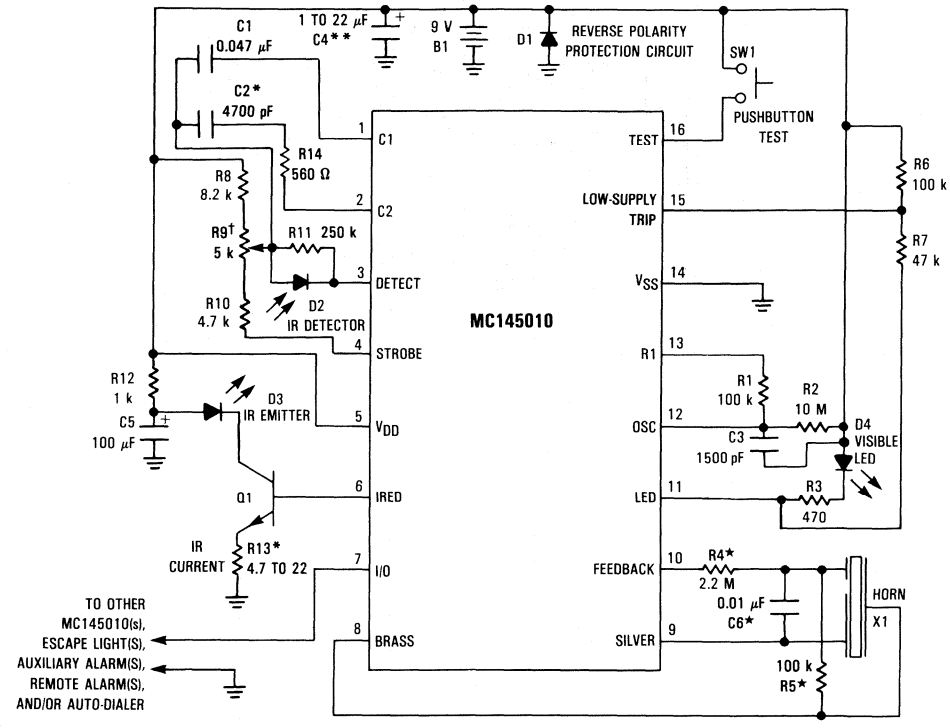
Figure 3. Standby Timing Diagram

NOTES: Numbers refer to the AC Electrical Characteristics Table.
Illustration is not to scale.



NOTES: Numbers refer to the AC Electrical Characteristics Table.
Illustration is not to scale.

Figure 4. Smoke Timing Diagram



*Values for R4, R5, and C6 may differ depending on type of piezoelectric horn used.

*C2 and R13 are used for coarse sensitivity adjustment. Typical values are shown.

†R9 is for fine sensitivity adjustment (optional). If fixed resistors are used, R8 = 12 k, R10 is 5.6 k to 10 k, and R9 is eliminated. When R9 is used, noise pickup is increased due to antenna effects. Shielding may be required.

**C4 should be 22 μF if B1 is a carbon battery. C4 could be reduced to 1 μF when an alkaline battery is used.

Figure 5. Battery-Powered Application

Table 1. Suppliers of Ancillary Components

Reference	Part Number	Description	Supplier	Contact Information
D1	MR500	Low-Leakage Power Rectifier	Motorola Semiconductor Products Sector	Phone: 1-800-521-6274 or contact your local Motorola Semiconductor Sales Office
D2	MRD821	Photodiode Detector	Motorola Semiconductor Products Sector	
D3	MLED81	Infrared Emitting Diode (IRED)	Motorola Semiconductor Products Sector	
D4	—	Light Emitting Diode (LED)	General Instruments, Optoelectronics Div.*	Phone: (415) 493-0400 TWX/TLX: 470208 FAX: (415) 493-7055
			Hewlett-Packard, Components Group*	Contact your local H-P Components Sales Office
			Wilbrecht Electronics, LEDCO Div.*	Phone: (612) 222-2791 TWX: (910) 563-3679 FAX: (612) 222-7639
Q1	MPS2222 MMBT2222	TO-92 Plastic SOT-23 Surface Mount	NPN Transistor, $\beta \geq 100$	Motorola Semiconductor Products Sector	(see above)
X1	—	Piezoelectric Audio Transducer	Motorola Components Div.	Phone: (505) 822-8801 TLX: 4999100 FAX: (505) 822-8801, x265

*Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of LED suppliers.

PIN DESCRIPTIONS

C1 (PIN 1)

A capacitor connected to this pin as shown in Figure 5 determines the gain of the on-chip photo amplifier during pushbutton test and chamber sensitivity test (high gain). The capacitor value is chosen such that the alarm is tripped from background reflections in the chamber during pushbutton test.

$A_V \approx 1 + (C1/10)$ where C1 is in pF. CAUTION: The value of the closed-loop gain should not exceed 10,000.

C2 (PIN 2)

A capacitor connected to this pin as shown in Figure 5 determines the gain of the on-chip photo amplifier except during pushbutton or chamber sensitivity tests.

$A_V \approx 1 + (C2/10)$ where C2 is in pF. This gain increases about 10% during the IRED pulse, after two consecutive local smoke detections.

Resistor R14 must be installed in series with C2. $R14 \approx [1/(12\sqrt{C2})] - 680$ where R14 is in ohms and C2 is in farads.

DETECT (PIN 3)

This input to the high-gain pulse amplifier is tied to the cathode of an external photodiode. The photodiode should have low capacitance and low dark leakage current. The diode must be shunted by a load resistor and is operated at zero bias.

The Detect input must be ac/dc decoupled from all other signals, V_{DD}, and V_{SS}. Lead length and/or foil traces to this pin must be minimized, also. See Figure 6.

STROBE (PIN 4)

This output provides a strobed, regulated voltage referenced to V_{DD}. The temperature coefficient of this voltage is ±0.2%/°C maximum from −10° to 60°C. The supply-voltage coefficient (line regulation) is ±0.2%/V maximum from 6 to 12 V. Strobe is tied to external resistor string R8, R9, and R10.

V_{DD} (PIN 5)

This pin is connected to the positive supply potential and may range from +6 to +12 V with respect to V_{SS}. CAUTION: In battery-powered applications, reverse-polarity protection must be provided externally.

IRED (PIN 6)

This output provides pulsed base current for external NPN transistor Q1 used as the infrared emitter driver. Q1 must have $\beta \geq 100$. At 10 mA, the temperature coefficient of the output voltage is typically +0.5%/°C from −10° to 60°C. The supply-voltage coefficient (line regulation) is ±0.2%/V maximum from 6 to 12 V. The IRED pulse width (active-high) is determined by external components R1 and C3. With a 100 kΩ/1500 pF combination, the nominal width is 105 μs.

To minimize noise impact, IRED is not active when the visible LED and horn outputs are active. IRED is active near the end of Strobe pulses for Smoke Tests, Chamber Sensitivity Test, and Pushbutton Test.

I/O (PIN 7)

This pin can be used to connect up to 40 units together in a wired-OR configuration for common signaling. V_{SS} is used as the return. An on-chip current sink minimizes noise pick up during non-smoke conditions and eliminates the need for an external pull-down resistor to complete the wired-OR. Remote units at lower supply voltages do not draw excessive current from a sending unit at a higher supply voltage.

I/O can also be used to activate escape lights, auxiliary alarms, remote alarms, and/or auto-dialers.

As an input, this pin feeds a positive-edge-triggered flip-flop whose output is sampled nominally every 625 ms during standby (using the recommended component values). A local-smoke condition or the pushbutton-test mode forces this current-limited output to source current. All input signals are ignored when I/O is sourcing current.

I/O is disabled by the on-chip power-on reset to eliminate nuisance signaling during battery changes or system power up.

If unused, I/O must be left unconnected.

BRASS (PIN 8)

This half of the push-pull driver output is connected to the metal support electrode of a piezoelectric audio transducer and to the horn-starting resistor. A continuous modulated tone from the transducer is a smoke alarm indicating either local or remote smoke. A short beep or chirp is a trouble alarm indicating a low supply or degraded chamber sensitivity.

SILVER (PIN 9)

This half of the push-pull driver output is connected to the ceramic electrode of a piezoelectric transducer and to the horn-starting capacitor.

FEEDBACK (PIN 10)

This input is connected to both the feedback electrode of a self-resonating piezoelectric transducer and the horn-starting resistor and capacitor through current-limiting resistor R4. If unused, this pin must be tied to V_{SS} or V_{DD}.

LED (PIN 11)

This active-low open-drain output directly drives an external visible LED at the pulse rates indicated below. The pulse width is equal to the OSC period.

The load for the low-supply test is applied by this output. This low-supply test is non-coincident with the smoke tests, chamber sensitivity test, pushbutton test, or any alarm signals.

The LED also provides a visual indication of the detector status as follows, assuming the component values shown in Figure 5:

Standby (includes low-supply and chamber sensitivity tests)—Pulses every 43 seconds (nominal)

Local Smoke—Pulses every 0.67 seconds (nominal)

Remote Smoke—No pulses

Pushbutton Test—Pulses every 0.67 seconds (nominal)

OSC (PIN 12)

This pin is used in conjunction with external resistor R2 (10 MΩ) to V_{DD} and external capacitor C3 (1500 pF) to V_{DD} to form an oscillator with a nominal period of 10.5 ms.

R1 (PIN 13)

This pin is used in conjunction with resistor R1 (100 kΩ) to pin 12 and C3 (1500 pF, see pin 12 description) to determine the IRED pulse width. With this RC combination, the nominal pulse width is 105 μs.

V_{SS} (PIN 14)

This pin is the negative supply potential and the return for the I/O pin. Pin 14 is usually tied to ground.

LOW-SUPPLY TRIP (PIN 15)

This pin is connected to an external voltage which determines the low-supply alarm threshold. The trip voltage is obtained through a resistor divider connected between the V_{DD} and LED pins. The low-supply alarm threshold voltage (in volts) $\approx (5R7/R6) + 5$ where R6 and R7 are in the same units.

TEST (PIN 16)

This input has an on-chip pull-down device and is used to manually invoke a test mode.

The *Pushbutton Test* mode is initiated by a high level at pin 16 (usually depression of a S.P.S.T. normally-open pushbutton switch to V_{DD}). After one oscillator cycle, IRED pulses approximately every 336 ms, regardless of the presence of smoke. Additionally, the amplifier gain is increased by automatic selection of C1. Therefore, the background reflections in the smoke chamber may be interpreted as smoke, generating a simulated-smoke condition. After the second IRED pulse, a successful test activates the horn-driver and I/O circuits. The active I/O allows remote signaling for system testing. When the Pushbutton Test switch is released, the Test input returns to V_{SS} due to the on-chip pull-down device. After one oscillator cycle, the amplifier gain returns to normal, thereby removing the simulated-smoke condition. After two additional IRED pulses, less than a second, the IC exits the alarm mode and returns to standby timing.

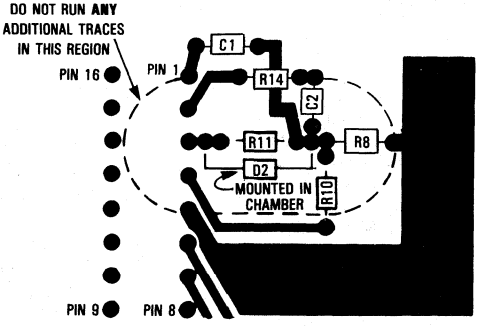
CALIBRATION

To facilitate checking the sensitivity and calibrating smoke detectors, the MC145010 can be placed in a calibration mode. In this mode, certain device pins are controlled/reconfigured as shown in Table 2. To place the part in the calibration mode, pin 16 (Test) must be pulled below the V_{SS} pin with 100 μA continuously drawn out of the pin for at least one cycle on the OSC pin. To exit this mode, the Test pin is floated for at least one OSC cycle.

In the calibration mode, the IRED pulse rate is increased to one for every OSC cycle. Also, Strobe is always active low.

Table 2. Configuration of Pins in the Calibration Mode

Description	Pin	Comment
I/O	7	Disabled as an output. Forcing this pin high places the photo amp output on pin 1 or 2, as determined by Low-Supply Trip. The amp's output appears as pulses.
Low-Supply Trip	15	If the I/O pin is high, pin 15 controls which gain capacitor is used. Low: normal gain, amp output on pin 1. High: supervisory gain, amp output on pin 2.
Feedback	10	Driving this input high enables hysteresis (10% gain increase) in the photo amp; pin 15 must be low.
OSC	12	Driving this input high brings the internal clock high. Driving the input low brings the internal clock low. If desired, the RC network for the oscillator may be left intact; this allows the oscillator to run similar to the normal mode of operation.
Silver	9	This pin becomes the smoke comparator output. A high level indicates that smoke has been detected.
Brass	8	This pin becomes the smoke integrator output. That is, two consecutive smoke detections are required for "on" (high level) and two consecutive no-detections for "off" (low level).



NOTES: Illustration is bottom view of layout using a DIP. Top view for SOIC layout is mirror image.
Optional potentiometer R9 is not included.
Drawing is not to scale.
Leads on D2, R11, R8, and R10 and their associated traces must be kept as short as possible. This practice minimizes noise pick up.
Pin 3 must be decoupled from all other traces.

Figure 6. Recommended PCB Layout

MC145011

Advance Information

Photoelectric Smoke Detector with I/O

For Line-Powered Applications

The CMOS MC145011 is an advanced smoke detector component containing sophisticated very-low-power analog and digital circuitry. The IC is used with an infrared photoelectric chamber. Detection is accomplished by sensing scattered light from minute smoke particles or other aerosols. When detection occurs, a pulsating alarm is sounded via on-chip push-pull drivers and an external piezoelectric transducer.

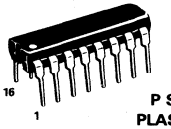
The variable-gain photo amplifier allows direct interface to IR detectors (photodiodes). Two external capacitors C1 and C2, C1 being the larger, determine the gain settings. Low gain is selected by the IC during most of the standby state. Medium gain is selected during a local-smoke condition. High gain is used during pushbutton test. During standby, the special monitor circuit which periodically checks for degraded chamber sensitivity uses high gain, also.

The I/O pin, in combination with V_{SS}, can be used to interconnect up to 40 units for common signaling. An on-chip current sink provides noise immunity when the I/O is an input. A local-smoke condition activates the short-circuit-protected I/O driver, thereby signaling remote smoke to the interconnected units. Additionally, the I/O pin can be used to activate escape lights, enable auxiliary or remote alarms, and/or initiate auto-dialers.

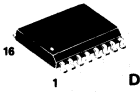
While in standby, the low-supply detection circuitry conducts periodic checks using a load current from the LED pin. The trip point is set using two external resistors. The supply for the MC145011 must be a dc power source capable of supplying 35 mA continuously and 45 mA peak. When the MC145011 is in standby, an external LED is continuously illuminated to indicate that the device is receiving power.

An extinguished LED accompanied by a pulsating audible alarm indicates a local-smoke condition. A pulsating audible alarm with the LED illuminated indicates a remote-smoke condition. A beep or chirp indicates a low-supply condition or degraded chamber sensitivity. A low-supply condition does not affect the smoke detection capability if $V_{DD} \geq 6$ V. Therefore, the low-supply condition and degraded chamber sensitivity can be distinguished by performing a pushbutton (chamber) test.

- Complies with the UL217 and UL268 Specifications
- Operating Voltage Range: 6 to 12 V
- Operating Temperature Range: −10 to 60°C
- Average Standby Supply Current (Visible LED Illuminated): 20 mA
- Power-On Reset Places IC in Standby Mode (Non-Alarm State)
- Electrostatic Discharge (ESD) and Latch Up Protection Circuitry on All Pins
- Chip Complexity: 2000 FETs, 12 NPNs, 16 Resistors, and 10 Capacitors



P SUFFIX
PLASTIC DIP
CASE 648

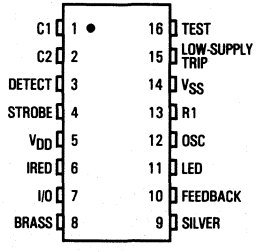


DW SUFFIX
PLASTIC SOG
CASE 751G

ORDERING INFORMATION

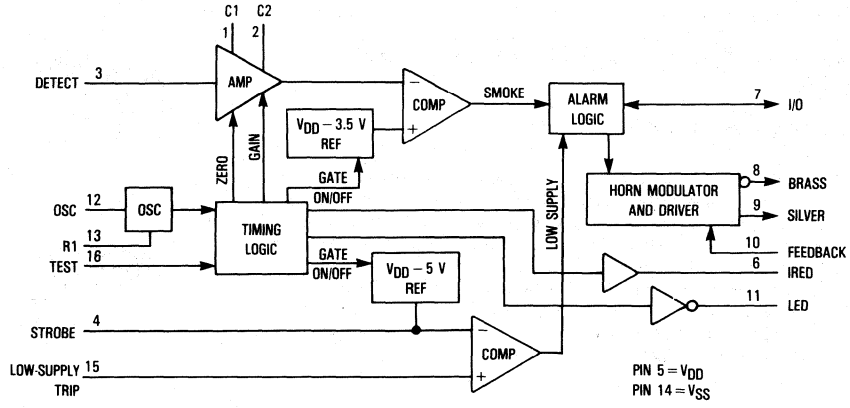
MC145011P	Plastic DIP
MC145011DW	SOG Package

PIN ASSIGNMENT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +12.0	V
V_{in}	DC Input Voltage C1, C2, Detect Osc, Low-Supply Trip I/O Feedback Test	−0.25 to V_{DD} + 0.25 −0.25 to V_{DD} + 0.25 −0.25 to V_{DD} + 10 −15 to +25 −1.0 to V_{DD} + 0.25	V
I_{in}	DC Input Current, per Pin	±10	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{DD}	DC Supply Current, V_{DD} and V_{SS} Pins	+25/−150	mA
P_D	Power Dissipation in Still Air, 5 seconds Continuous	1200† 350★	mW
T_{stg}	Storage Temperature	−55 to +125	°C
T_L	Lead Temperature, 1 mm from Case for 10 seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables.

†Derating: −12 mW/°C from 25° to 60°C.

★Derating: −3.5 mW/°C from 25° to 60°C.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$ except for the I/O, which can exceed V_{DD}, and the Test input, which can go below V_{SS}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs and/or an unused I/O must be left open.

ELECTRICAL CHARACTERISTICS (T_A = −10 to 60°C Unless Otherwise Indicated, Voltages Referenced to V_{SS})

Symbol	Parameter		Test Condition	V_{DD} V	Min	Max	Unit
V_{DD}	Power Supply Voltage Range			—	6	12	V
V_{TH}	Supply Threshold Voltage, Low-Supply Alarm		Low-Supply Trip: $V_{in} = V_{DD}/3$	—	6.5	7.8	V
I_{DD}	Average Operating Supply Current, Excluding the Visible LED Current (per Package)		Standby Configured per Fig. 5	12.0	—	12	μA
i_{DD}	Peak Supply Current, Excluding the Visible LED Current (per Package)		During Strobe On, IRED Off Configured per Fig. 5	12.0	—	2.0	mA
			During Strobe On, IRED On Configured per Fig. 5	12.0	—	3.0	
V_{IL}	Low-Level Input Voltage	I/O		9.0	—	1.5	V
		Feedback		9.0	—	2.7	
		Test		9.0	—	7.0	
V_{IH}	High-Level Input Voltage	I/O		9.0	3.2	—	V
		Feedback		9.0	6.3	—	
		Test		9.0	8.5	—	
I_{in}	Input Current	Osc, Detect	$V_{in} = V_{SS}$ or V_{DD}	12.0	—	±100	nA
		Low-Supply Trip	$V_{in} = V_{SS}$ or V_{DD}	12.0	—	±100	
		Feedback	$V_{in} = V_{SS}$ or V_{DD}	12.0	—	±100	
I_{IL}	Low-Level Input Current	Test	$V_{in} = V_{SS}$	12.0	—	−1	μA
I_{IH}	Pull-Down Current	Test	$V_{in} = V_{DD}$	9.0	0.5	10	μA
		I/O	No Local Smoke, $V_{in} = V_{DD}$	9.0	25	100	
			No Local Smoke, V_{in} = 17 V	12.0	—	140	
V_{OL}	Low-Level Output Voltage	LED	I_{out} = 10 mA	6.5	—	0.6	V
		Silver, Brass	I_{out} = 16 mA	6.5	—	1.0	
V_{OH}	High-Level Output Voltage	Silver, Brass	I_{out} = −16 mA	6.5	5.5	—	V
V_{out}	Output Voltage (For Line Regulation, see Pin Descriptions)	Strobe	Inactive, I_{out} = −1 μA	—	V_{DD} − 0.1	—	V
			Active, I_{out} = 100 μA to 500 μA (Load Regulation)	9.0	V_{DD} − 4.4	V_{DD} − 5.6	
		IRED	Inactive, I_{out} = 1 μA	—	—	0.1	
			Active, I_{out} = 6 mA (Load Regulation)	9.0	2.25*	3.75*	
I_{OH}	High-Level Output Current	I/O	Local Smoke, V_{out} = 4.5 V	6.5	−4	—	mA
			Local Smoke, $V_{out} = V_{SS}$ (Short Circuit Current)	12.0	—	−16	
I_{OZ}	Off-State Output Leakage Current	LED	$V_{out} = V_{SS}$ or V_{DD}	12.0	—	±1	μA
V_{IC}	Common Mode Voltage Range	C1, C2, Detect	Local Smoke, Pushbutton Test, or Chamber Sensitivity Test	—	V_{DD} − 4	V_{DD} − 2	V
V_{ref}	Smoke Comparator Reference Voltage	Internal	Local Smoke, Pushbutton Test, or Chamber Sensitivity Test	—	V_{DD} − 3.08	V_{DD} − 3.92	V

*T_A = 25°C only.

AC ELECTRICAL CHARACTERISTICS (Reference Timing Diagram Figures 3 and 4)
($T_A = 25°C, V_{DD} = 9.0$ V, Component Values from Figure 5: R1 = 100.0 KΩ, C3 = 1500.0 pF, R2 = 10.0 MΩ)

No.	Symbol	Parameter	Test Condition	Min	Max	Unit
1	$1/f_{osc}$	Oscillator Period	Free-Running Sawtooth Measured at Pin 12	9.5	11.5	ms
2	t_{LED}	LED Status	No Local Smoke, and No Remote Smoke	Illuminated		
3			Remote Smoke, but No Local Smoke	Illuminated		
4			Local Smoke or Pushbutton Test	Extinguished		
5	$t_{w(stb)}$	Strobe Pulse Width		9.5	11.5	ms
6	t_{IRED}	IRED Pulse Period	Smoke Test	9.67	11.83	s
7			Chamber Sensitivity Test, without Local Smoke	38.9	47.1	
8			Pushbutton Test	0.302	0.370	
9	$t_{w(IRED)}$	IRED Pulse Width		94	116	μs
10	t_r	IRED Rise Time		—	30	μs
	t_f	IRED Fall Time		—	200	
11	t_{mod}	Silver and Brass Modulation Period	Local or Remote Smoke	297	363	ms
11, 12	t_{on}/t_{mod}	Silver and Brass Duty Cycle	Local or Remote Smoke	73	77	%
13	t_{CH}	Silver and Brass Chirp Pulse Period	Low Supply or Degraded Chamber Sensitivity	38.9	47.1	s
14	$t_{w(CH)}$	Silver and Brass Chirp Pulse Width	Low Supply or Degraded Chamber Sensitivity	9.5	11.5	ms
15	t_{RR}	Rising Edge on I/O to Smoke Alarm Response Time	Remote Smoke, No Local Smoke	—	800	ms
16	t_{stb}	Strobe Pulse Period	Smoke Test	9.67	11.83	s
17			Chamber Sensitivity Test, without Local Smoke	38.9	47.1	
18			Low Supply Test, without Local Smoke	38.9	47.1	
19			Pushbutton Test	0.302	0.370	

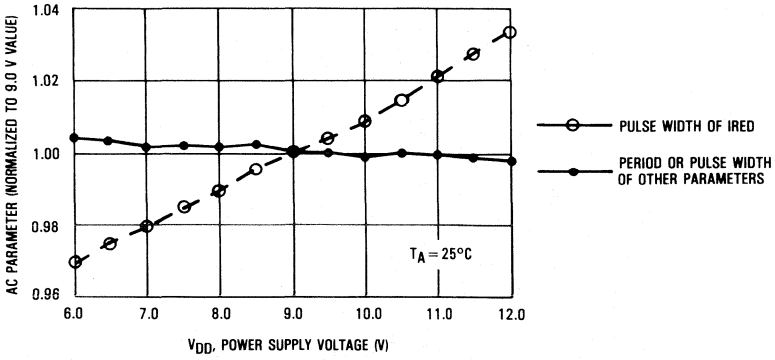
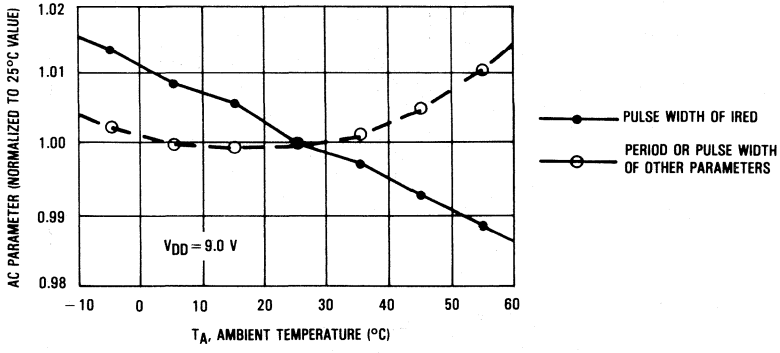
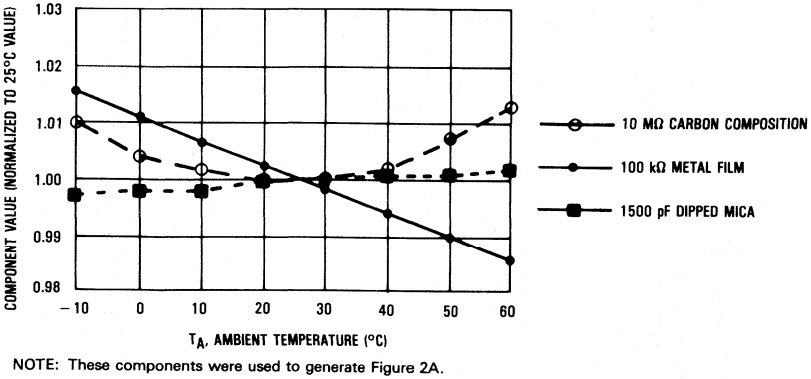


Figure 1. AC Characteristics versus Supply



NOTE: Includes external component variations. See Figure 2B.

Figure 2A. AC Characteristics versus Temperature



NOTE: These components were used to generate Figure 2A.

Figure 2B. RC Component Variation Over Temperature

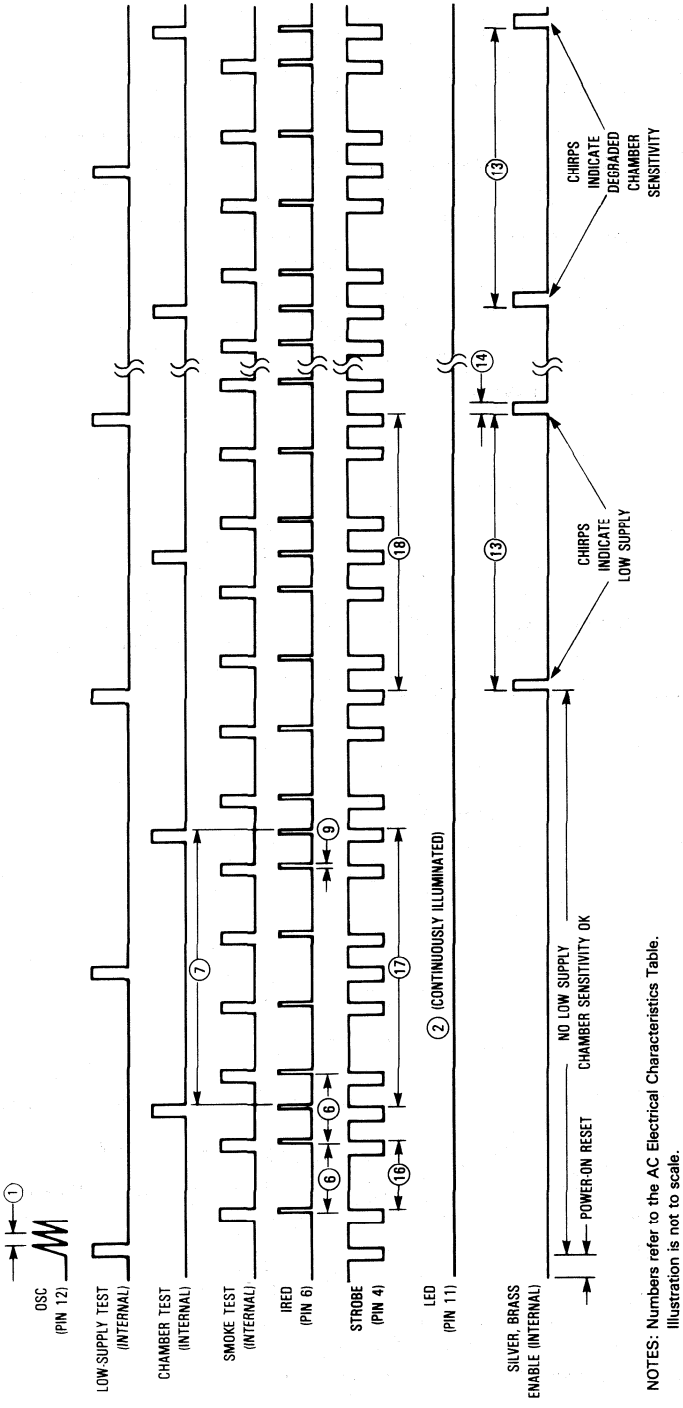


Figure 3. Standby Timing Diagram

NOTES: Numbers refer to the AC Electrical Characteristics Table.
Illustration is not to scale.

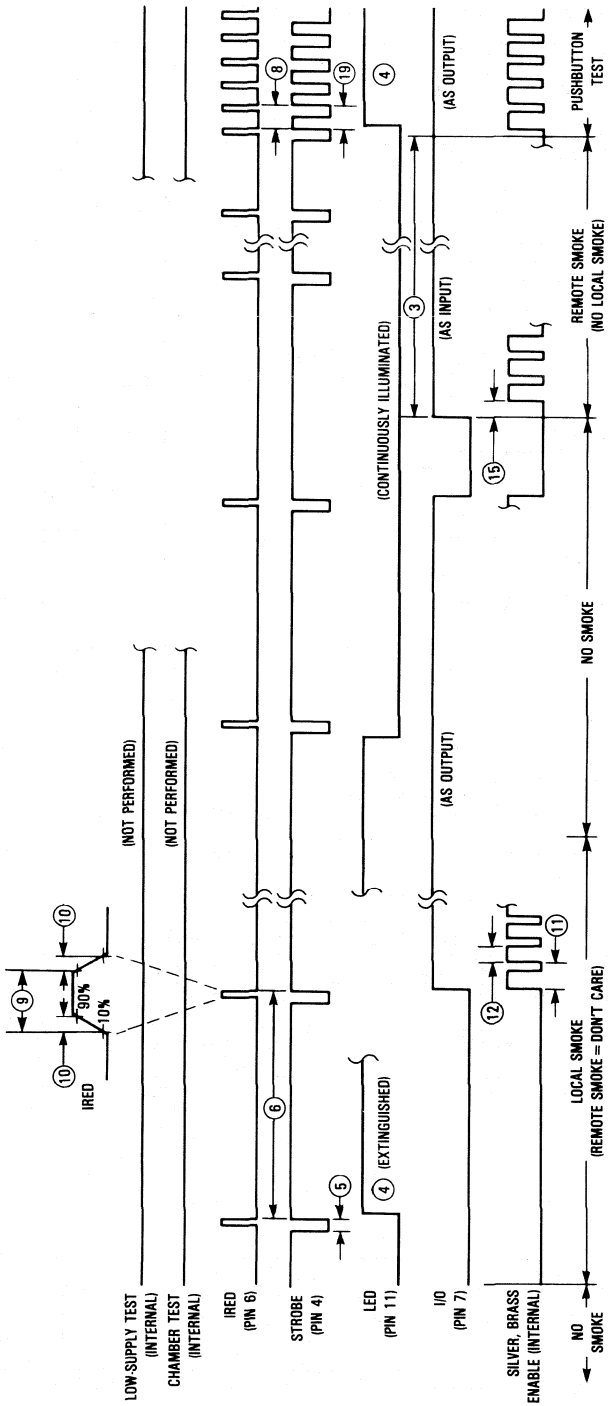
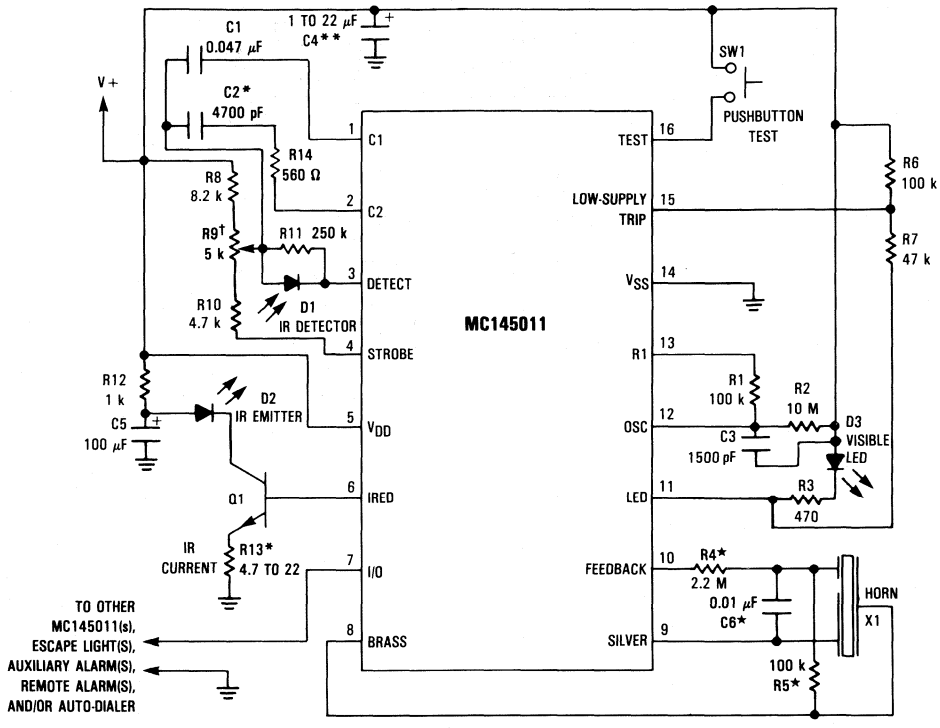


Figure 4. Smoke Timing Diagram

NOTES: Numbers refer to the AC Electrical Characteristics Table.
Illustration is not to scale.



*Values for R4, R5, and C6 may differ depending on type of piezoelectric horn used.
*C2 and R13 are used for coarse sensitivity adjustment. Typical values are shown.
†R9 is for fine sensitivity adjustment (optional). If fixed resistors are used, R8 = 12 k, R10 is 5.6 k to 10 k, and R9 is eliminated. When R9 is used, noise pickup is increased due to antenna effects. Shielding may be required.
**C4 should be 22 μF if supply line resistance is high (up to 50 Ω). C4 could be reduced to 1 μF when supply line resistance <30 Ω.

Figure 5. Application

Table 1. Suppliers of Ancillary Components

Reference	Part Number	Description	Supplier	Contact Information
D1	MRD821	Photodiode Detector	Motorola Semiconductor Products Sector	Phone: 1-800-521-6274 or contact your local Motorola Semiconductor Sales Office
D2	MLED81	Infrared Emitting Diode (IRED)	Motorola Semiconductor Products Sector	
D3	–	Light Emitting Diode (LED)	General Instruments, Optoelectronics Div.*	Phone: (415) 493-0400 TWX/TLX: 470208 FAX: (415) 493-7055
			Hewlett-Packard, Components Group*	Contact your local H-P Components Sales Office
			Wilbrecht Electronics, LEDCO Div.*	Phone: (612) 222-2791 TWX: (910) 563-3679 FAX: (612) 222-7639
Q1	MPS2222 MMBT2222	TO-92 Plastic SOT-23 Surface Mount } NPN Transistor, $\beta \geq 100$	Motorola Semiconductor Products Sector	(see above)
X1	–	Piezoelectric Audio Transducer	Motorola Components Div.	Phone: (505) 822-8801 TLX: 4999100 FAX: (505) 822-8801, x265

*Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of LED suppliers.

PIN DESCRIPTIONS

C1 (PIN 1)

A capacitor connected to this pin as shown in Figure 5 determines the gain of the on-chip photo amplifier during pushbutton test and chamber sensitivity test (high gain). The capacitor value is chosen such that the alarm is tripped from background reflections in the chamber during pushbutton test.

$A_V \approx 1 + (C1/10)$ where C1 is in pF. CAUTION: The value of the closed-loop gain should not exceed 10,000.

C2 (PIN 2)

A capacitor connected to this pin as shown in Figure 5 determines the gain of the on-chip photo amplifier except during pushbutton or chamber sensitivity tests.

$A_V \approx 1 + (C2/10)$ where C2 is in pF. This gain increases about 10% during the IRED pulse, after two consecutive local smoke detections.

Resistor R14 must be installed in series with C2. $R14 \approx [1/(12\sqrt{C2})] - 680$ where R14 is in ohms and C2 is in farads.

DETECT (PIN 3)

This input to the high-gain pulse amplifier is tied to the cathode of an external photodiode. The photodiode should have low capacitance and low dark leakage current. The diode must be shunted by a load resistor and is operated at zero bias.

The Detect input must be ac/dc decoupled from all other signals, V_{DD}, and V_{SS}. Lead length and/or foil traces to this pin must be minimized, also. See Figure 6.

STROBE (PIN 4)

This output provides a strobed, regulated voltage referenced to V_{DD}. The temperature coefficient of this voltage is ±0.2%/°C maximum from −10° to 60°C. The supply-voltage coefficient (line regulation) is ±0.2%/V maximum from 6 to 12 V. Strobe is tied to external resistor string R8, R9, and R10.

V_{DD} (PIN 5)

This pin is connected to the positive supply potential and may range from +6 to +12 V with respect to V_{SS}.

IRED (PIN 6)

This output provides pulsed base current for external NPN transistor Q1 used as the infrared emitter driver. Q1 must have $\beta \geq 100$. At 10 mA, the temperature coefficient of the output voltage is typically +0.5%/°C from −10° to 60°C. The supply-voltage coefficient (line regulation) is ±0.2%/V maximum from 6 to 12 V. The IRED pulse width (active-high) is determined by external components R1 and C3. With a 100 kΩ/1500 pF combination, the nominal width is 105 μs.

To minimize noise impact, IRED is not active when the visible LED and horn outputs are active. IRED is active near the end of Strobe pulses for Smoke Tests, Chamber Sensitivity Test, and Pushbutton Test.

I/O (PIN 7)

This pin can be used to connect up to 40 units together in a wired-OR configuration for common signaling. V_{SS} is used as the return. An on-chip current sink minimizes noise pick up during non-smoke conditions and eliminates the need for an external pull-down resistor to complete the wired-OR. Remote units at lower supply voltages do not draw excessive current from a sending unit at a higher supply voltage.

I/O can also be used to activate escape lights, auxiliary alarms, remote alarms, and/or auto-dialers.

As an input, this pin feeds a positive-edge-triggered flip-flop whose output is sampled nominally every 625 ms during standby (using the recommended component values). A local-smoke condition or the pushbutton-test mode forces this current-limited output to source current. All input signals are ignored when I/O is sourcing current.

I/O is disabled by the on-chip power-on reset to eliminate nuisance signaling during battery changes or system power up.

If unused, I/O must be left unconnected.

BRASS (PIN 8)

This half of the push-pull driver output is connected to the metal support electrode of a piezoelectric audio transducer and to the horn-starting resistor. A continuous modulated tone from the transducer is a smoke alarm indicating either local or remote smoke. A short beep or chirp is a trouble alarm indicating a low supply or degraded chamber sensitivity.

SILVER (PIN 9)

This half of the push-pull driver output is connected to the ceramic electrode of a piezoelectric transducer and to the horn-starting capacitor.

FEEDBACK (PIN 10)

This input is connected to both the feedback electrode of a self-resonating piezoelectric transducer and the horn-starting resistor and capacitor through current-limiting resistor R4. If unused, this pin must be tied to V_{SS} or V_{DD}.

LED (PIN 11)

This active-low open-drain output directly drives an external visible LED.

The load for the low-supply test is applied by this output. This low-supply test is non-coincident with the smoke tests, chamber sensitivity test, pushbutton test, or any alarm signals.

The LED also provides a visual indication of the detector status as follows, assuming the component values shown in Figure 5:

Standby (includes low-supply and chamber sensitivity tests)—constantly illuminated

Local Smoke—constantly extinguished

Remote Smoke—constantly illuminated

Pushbutton Test—constantly extinguished (system OK)
constantly illuminated (system problem)

OSC (PIN 12)

This pin is used in conjunction with external resistor R2 (10 MΩ) to V_{DD} and external capacitor C3 (1500 pF) to V_{DD} to form an oscillator with a nominal period of 10.5 ms.

R1 (PIN 13)

This pin is used in conjunction with resistor R1 (100 kΩ) to pin 12 and C3 (1500 pF, see pin 12 description) to determine the IRED pulse width. With this RC combination, the nominal pulse width is 105 μs.

V_{SS} (PIN 14)

This pin is the negative supply potential and the return for the I/O pin. Pin 14 is usually tied to ground.

LOW-SUPPLY TRIP (PIN 15)

This pin is connected to an external voltage which determines the low-supply alarm threshold. The trip voltage is obtained through a resistor divider connected between the V_{DD} and LED pins. The low-supply alarm threshold voltage (in volts) $\approx$ (5R7/R6) + 5 where R6 and R7 are in the same units.

TEST (PIN 16)

This input has an on-chip pull-down device and is used to manually invoke a test mode.

The *Pushbutton Test* mode is initiated by a high level at pin 16 (usually depression of a S.P.S.T. normally-open pushbutton switch to V_{DD}). After one oscillator cycle, IRED pulses approximately every 336 ms, regardless of the presence of smoke. Additionally, the amplifier gain is increased by automatic selection of C1. Therefore, the background reflections in the smoke chamber may be interpreted as smoke, generating a simulated-smoke condition. After the second IRED pulse, a successful test activates the horn-driver and I/O circuits. The active I/O allows remote signaling for system testing. When the Pushbutton Test switch is released, the Test input returns to V_{SS} due to the on-chip pull-down device. After one oscillator cycle, the amplifier gain returns to normal, thereby removing the simulated-smoke condition. After two additional IRED pulses, less than a second, the IC exits the alarm mode and returns to standby timing.

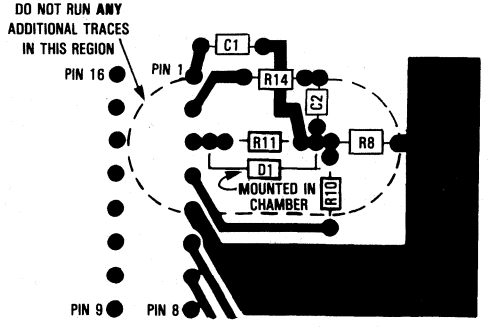
CALIBRATION

To facilitate checking the sensitivity and calibrating smoke detectors, the MC145011 can be placed in a calibration mode. In this mode, certain device pins are controlled/reconfigured as shown in Table 2. To place the part in the calibration mode, pin 16 (Test) must be pulled below the V_{SS} pin with 100 μA continuously drawn out of the pin for at least one cycle on the OSC pin. To exit this mode, the Test pin is floated for at least one OSC cycle.

In the calibration mode, the IRED pulse rate is increased to one for every OSC cycle. Also, Strobe is always active low.

Table 2. Configuration of Pins in the Calibration Mode

Description	Pin	Comment
I/O	7	Disabled as an output. Forcing this pin high places the photo amp output on pin 1 or 2, as determined by Low-Supply Trip. The amp's output appears as pulses.
Low-Supply Trip	15	If the I/O pin is high, pin 15 controls which gain capacitor is used. Low: normal gain, amp output on pin 1. High: supervisory gain, amp output on pin 2.
Feedback	10	Driving this input high enables hysteresis (10% gain increase) in the photo amp; pin 15 must be low.
Osc	12	Driving this input high brings the internal clock high. Driving the input low brings the internal clock low. If desired, the RC network for the oscillator may be left intact; this allows the oscillator to run similar to the normal mode of operation.
Silver	9	This pin becomes the smoke comparator output. A high level indicates that smoke has been detected.
Brass	8	This pin becomes the smoke integrator output. That is, 2 consecutive smoke detections are required for "on" (high level) and 2 consecutive no-detections for "off" (low level).



NOTES: Illustration is bottom view of layout using a DIP. Top view for SOIC layout is mirror image.
Optional potentiometer R9 is not included.
Drawing is not to scale.
Leads on D1, R11, R8, and R10 and their associated traces must be kept as short as possible. This practice minimizes noise pick up.
Pin 3 must be decoupled from all other traces.

Figure 6. Recommended PCB Layout

Miscellaneous Functions

Miscellaneous Functions

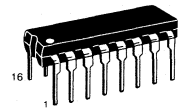
		Page No.
MC68HC68T1	Real-Time Clock plus RAM with Serial Interface	8-3
MC141620	Enhanced Comb Filter	8-25

MC68HC68T1

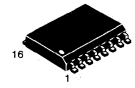
Advance Information

Real-Time Clock plus RAM with Serial Interface

CMOS



P SUFFIX
PLASTIC DIP
CASE 648

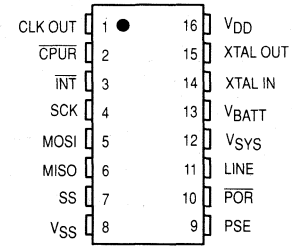


DW SUFFIX
SOG
CASE 751G

ORDERING INFORMATION

MC68HC68T1P Plastic DIP
MC68HC68T1DW SOG Package

PIN ASSIGNMENT



The MC68HC68T1 HCMOS Clock/RAM peripheral contains a real-time clock/calendar, a 32 × 8 static RAM, and a synchronous, serial, three-wire interface for communication with a microcomputer. Operating in a burst mode, successive Clock/RAM locations can be read or written using only a single starting address. An on-chip oscillator allows acceptance of a selectable crystal frequency or the device can be programmed to accept a 50/60 Hz line input frequency.

The LINE and V_{SYS} pins give the MC68HC68T1 the capability for sensing power-up/power-down conditions, a capability useful for battery-backup systems. The device has an interrupt output capable of signaling the microcomputer of an alarm, periodic interrupt, or power sense condition. An alarm can be set for comparison with the seconds, minutes, and hours registers. This alarm can be used in conjunction with the power supply enable (PSE) output to initiate a system power-up sequence if the V_{SYS} pin is powered to the proper level.

A software power-down sequence can be initiated by setting a bit in the interrupt control register. This applies a reset to the CPU via the $\overline{CPUR}$ pin, sets the clock out (CLK OUT) and power supply enable (PSE) pins low, and disables the serial interface. This condition is held until a rising edge is sensed on the system voltage (V_{SYS}) input pin, signaling system power coming on, or by activation of a previously enabled interrupt if the V_{SYS} pin is powered up.

A watch-dog circuit can be enabled that requires the microcomputer to toggle the slave select (SS) pin of the MC68HC68T1 periodically without performing a serial transfer. If this condition is not sensed, the $\overline{CPUR}$ line resets the CPU.

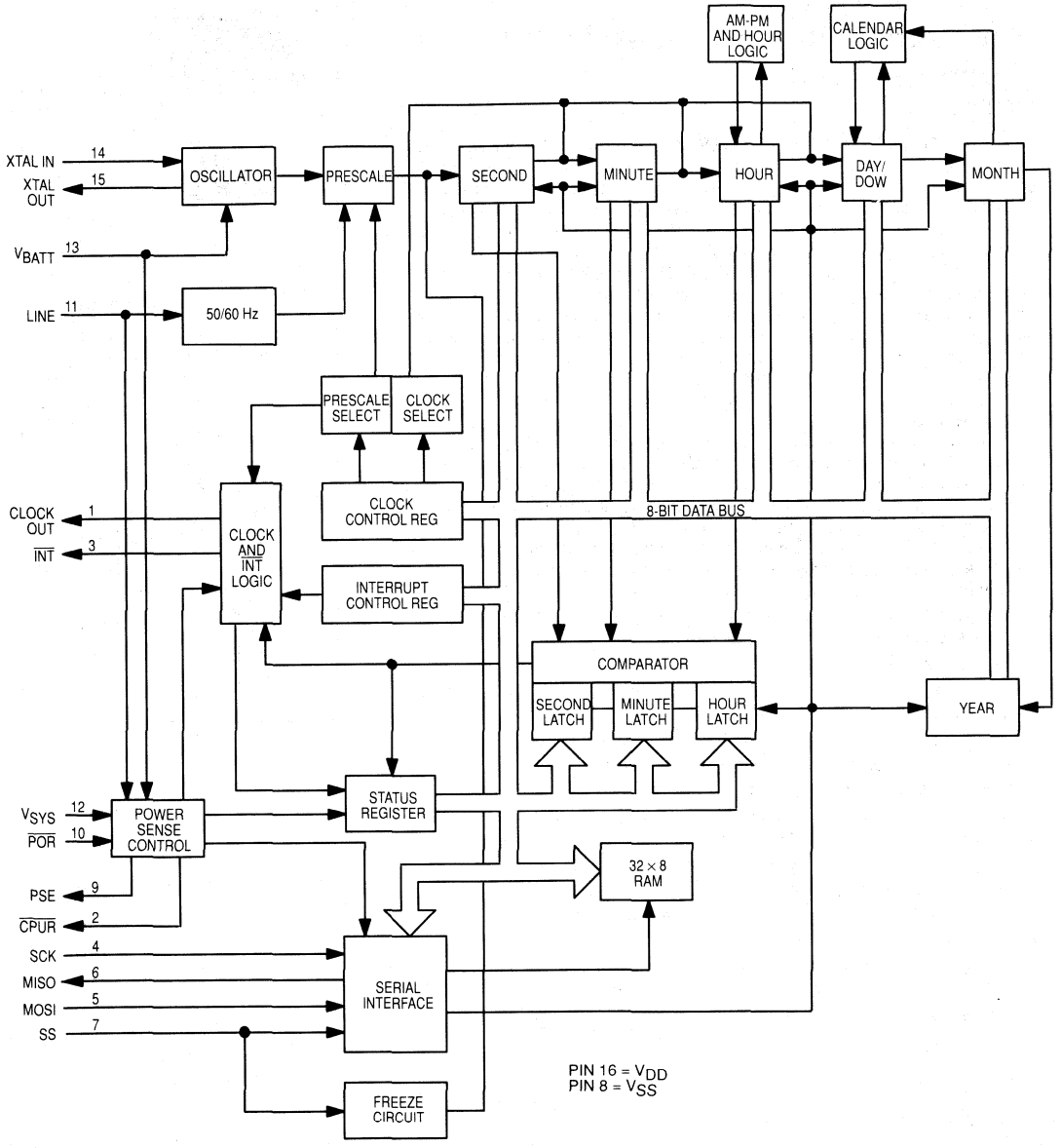
- Full Clock Features — Seconds, Minutes, Hours (AM/PM), Day-of-Week, Date, Month, Year (0-99), Auto Leap Year
- 32 Byte General-Purpose RAM
- Direct Interface to Motorola SPI and National MICROWIRE™ Serial Data Ports
- Minimum Timekeeping Voltage: 2.2 V
- Burst Mode for Reading/Writing Successive Addresses in Clock/RAM
- Selectable Crystal or 50/60 Hz Line Input Frequency
- Clock Registers Utilize BCD Data
- Buffered Clock Output for Driving CPU Clock, Timer, Colon, or LCD Backplane
- Power-On Reset with First-Time-Up Bit
- Freeze Circuit Eliminates Software Overhead During a Clock Read
- Three Independent Interrupt Modes — Alarm, Periodic, or Power-Down
- CPU Reset Output — Provides Orderly Power Up/Power Down
- Watch-Dog Circuit
- Pin-for-Pin Replacement for CDP68HC68T1
- Chip Complexity: 8500 FETs or 2125 Equivalent Gates
- Also See Application Note ANE425

8

MICROWIRE is a trademark of National Semiconductor Inc.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (except Line Input**)	– 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage	–0.5 to V_{DD} + 0.5	V
I_{in}	DC Input Current, per Pin	± 10	mA
I_{out}	DC Output Current, per Pin	± 10	mA
I_{DD}	DC Supply Current, V_{DD} and V_{SS} Pins	± 30	mA
P_D	Power Dissipation, per Package***	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature (10-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
**See Electrical Characteristics Table
***Power Dissipation Temperature Derating: – 12 mW/°C from 65°C to 85°C.

This device contains protection circuitry to guard against damage due to high static voltages or electrical fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always to tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (T_A = – 40 to + 85°C, Voltages Referenced to V_{SS})

Symbol	Parameter	Test Condition	V_{DD} V	Guaranteed Limit	Unit
V_{DD}	Power Supply Voltage Range		—	3.0 to 6.0	V
$V_{(stdby)}$	Minimum Standby (Timekeeping) Voltage*		—	2.2	V
V_{IL}	Maximum Low-Level Input Voltage		3.0 4.5 6.0	0.9 1.35 1.8	V
V_{IH}	Minimum High-Level Input Voltage		3.0 4.5 6.0	2.1 3.15 4.2	V
V_{in}	Maximum Input Voltage, Line Input	Power-Sense Mode	5.0	12	V p-p
V_{OL}	Maximum Low-Level Output Voltage	I_{out} = 0 µA I_{out} = 1.6 mA	4.5	0.1 0.4	V
V_{OH}	Minimum High-Level Output Voltage	I_{out} = 0 µA I_{out} = 1.6 mA	4.5	4.4 3.7	V
I_{in}	Maximum Input Current, Except SS	V_{in} = V_{DD} or V_{SS}	6.0	± 1	µA
I_{IL}	Maximum Low-Level Input Current, SS	V_{in} = V_{SS}	6.0	– 1.0	µA
I_{IH}	Maximum Pull-Down Current, SS	V_{in} = V_{DD}	6.0	100	µA
I_{OZ}	Maximum 3-State Leakage Current	V_{out} = V_{DD} or V_{SS}	6.0	± 10	µA
I_{DD}	Maximum Quiescent Supply Current	V_{in} = V_{DD} or V_{SS}, All Inputs I_{out} = 0 µA	6.0	50	µA
I_{DD}	Maximum RMS Operating Supply Current Crystal Operation	I_{out} = 0 µA, $f_{XTAL\ IN}$ = 32 kHz V_{in} = V_{DD} or V_{SS}, all inputs except XTAL IN, $f_{XTAL\ IN}$ = 1 MHz $f_{XTAL\ IN}$ = 2 MHz $f_{XTAL\ IN}$ = 4 MHz Clock Out Disabled, No Serial Access Cycles	5.0	0.1 0.6 0.84 1.2	mA
	Maximum RMS Operating Supply Current External Frequency Source Driving XTAL IN, XTAL OUT Open	I_{out} = 0 µA, $f_{XTAL\ IN}$ = 32 kHz V_{in} = V_{DD} or V_{SS}, $f_{XTAL\ IN}$ = 1 MHz Clock Out Disabled, $f_{XTAL\ IN}$ = 2 MHz No Serial Access Cycles $f_{XTAL\ IN}$ = 4 MHz	5.0	0.024 0.12 0.24 0.5	

*Timekeeping function only, no read/write accesses. Data in the registers and RAM retained.

(Continued)

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Condition	V_{DD} V	Guaranteed Limit	Unit
I_{batt}	Maximum RMS Standby Current Crystal Operation	V_{batt} = 3.0 V, V_{sys} = 0.0 V, V_{DD} = 0.0 V, I_{out} = 0 μA, V_{in} = Don't Care, all inputs except XTAL IN, Clock Out Disabled, No Serial Access Cycles	0.0	25 250 360 600	μA
		$f_{XTAL\ IN}$ = 32 kHz $f_{XTAL\ IN}$ = 1 MHz $f_{XTAL\ IN}$ = 2 MHz $f_{XTAL\ IN}$ = 4 MHz			

AC ELECTRICAL CHARACTERISTICS (T_A = −40 to + 85°C, C_L = 200 pF, Input $t_r = t_f$ = 6 ns, Voltages Referenced to V_{SS})

Symbol	Parameter	V_{DD} V	Guaranteed Limit	Unit
f_{SCK}	Maximum Clock Frequency (Refer to SCK t_w, below) (Figures 1, 2, and 3)	3.0 4.5 6.0	TBD 2.1 2.1	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, SCK to MISO (Figures 2 and 3)	3.0 4.5 6.0	200 100 100	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, SS to MISO (Figures 2 and 4)	3.0 4.5 6.0	200 100 100	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, SCK to MISO (Figures 2 and 4)	3.0 4.5 6.0	200 100 100	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 2 and 3) (Measured Between 70% V_{DD} and 20% V_{DD})	3.0 4.5 6.0	200 100 100	ns
C_{in}	Maximum Input Capacitance	—	10	pF

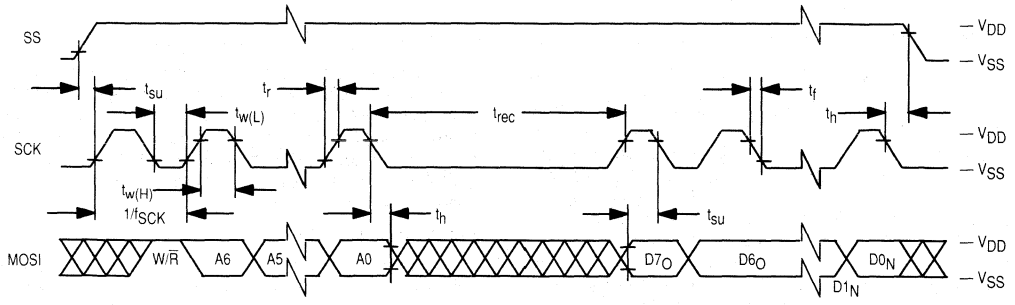
TIMING REQUIREMENTS (T_A = − 40 to + 85°C, Input $t_r = t_f$ = 6 ns, Voltages Referenced to V_{SS})

Symbol	Parameter	V_{DD} V	Guaranteed Limit	Unit
t_{su}	Minimum Setup Time, SS to SCK (Figures 1 and 2)	3.0 4.5 6.0	200 100 100	ns
t_{su}	Minimum Setup Time, MOSI to SCK (Figures 1 and 2)	3.0 4.5 6.0	200 100 100	ns
t_h	Minimum Hold Time, SCK to SS (Figures 1 and 2)	3.0 4.5 6.0	200 125 125	ns
t_h	Minimum Hold Time, SCK to MOSI (Figures 1 and 2)	3.0 4.5 6.0	200 100 100	ns
t_{rec}	Minimum Recovery Time, SCK (Figures 1 and 2)	3.0 4.5 6.0	200 200 200	ns
$t_{w(H)}$, $t_{w(L)}$	Minimum Pulse Width, SCK (Figures 1 and 2)	3.0 4.5 6.0	400 200 200	ns

(Continued)

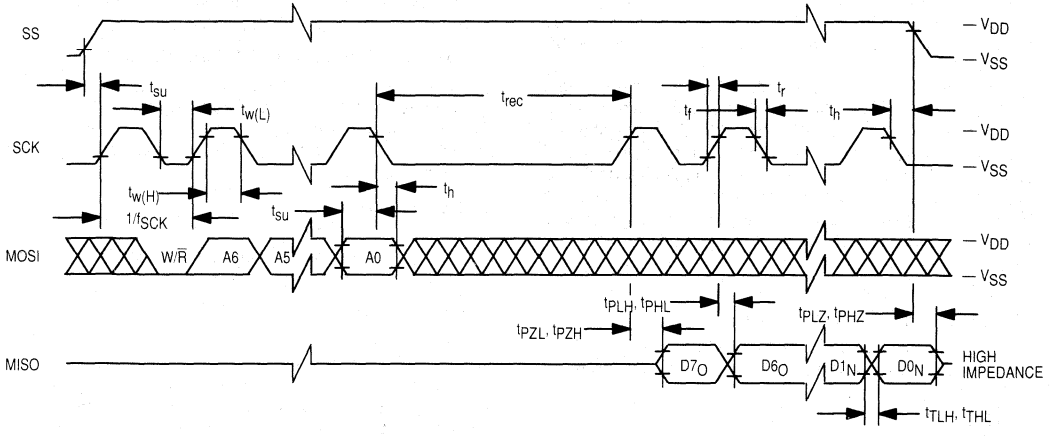
TIMING REQUIREMENTS (Continued)

Symbol	Parameter	VDD V	Guaranteed Limit	Unit
t_w	Minimum Pulse Width, $\overline{POR}$	3.0 4.5 6.0	TBD 100 100	ns
t_r, t_f	Maximum Input Rise and Fall Times (Except XTAL IN and $\overline{POR}$) (Figures 1 and 2) (Measured Between 70% V_{DD} and 20% V_{DD})	3.0 4.5 6.0	TBD 2 2	µs



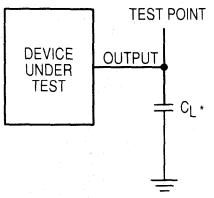
NOTE: Measurement points are V_{IL} and V_{IH} unless otherwise noted on the ac electrical characteristics table.

Figure 1. Write Cycle



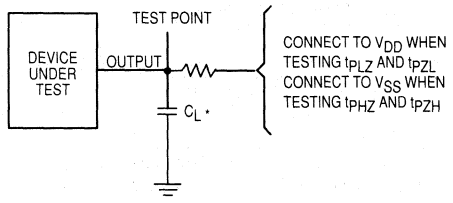
NOTE: Measurement points are V_{OL}, V_{OH}, V_{IL}, and V_{IH} unless otherwise noted on the ac electrical characteristics table.

Figure 2. Read Cycle



*Includes all probe and jig capacitance.

Figure 3. Test Circuit



*Includes all probe and jig capacitance.

Figure 4. Test Circuit

OPERATING CHARACTERISTICS

The real-time clock consists of a clock/calendar and a 32 x 8 RAM. (See Figure 5). Communication with the device may be established via a serial peripheral interface (SPI) or MICROWIRE bus. In addition to the clock/calendar data from seconds to years, and systems flexibility provided by the 32-byte RAM, the clock features computer handshaking with an interrupt output and a separate square-wave clock output that can be one of seven different frequencies. An alarm circuit is available that compares the alarm latches with the seconds, minutes, and hours time counters and activates the interrupt output when they are equal. The clock is specifically designed to aid in power up/power down applications and offers several pins to aid the designer of battery-backup systems.

CLOCK/CALENDAR

The clock/calendar portion of this device consists of a long string of counters that is toggled by a 1 Hz input. The 1 Hz input is derived from the on-chip oscillator that utilizes one of four possible external crystals or that can be driven by an external frequency source. The 1 Hz trigger to the counters can also be supplied by a 50 or 60 Hz source that is connected to the LINE input pin.

The time counters offer seconds, minutes, and hours data in 12- or 24-hour format. An AM/PM indicator is available that once set, toggles at 12:00 AM and 12:00 PM. The calendar counters consist of day of week, date of month, month, and year information. Data in the counters is in BCD format. The hours counter utilizes BCD for hours data plus bits for 12/24 hour and AM/PM modes. The seven time counters are read serially at addresses $20 through $26. The time counters are written to at addresses $A0 through $A6. (See Table 1 and Figure 6.)

32 x 8 GENERAL-PURPOSE RAM

The real-time clock also has a static 32 x 8 RAM. The RAM is read at addresses $00 through $1F and written to at addresses $80 through $9F. (See Figure 5.)

ALARM

The alarm is set by accessing the three alarm latches and loading the desired data. (See **SERIAL PERIPHERAL INTERFACE**.) The alarm latches consist of seconds, minutes, and hours registers. When their outputs equal the values of the seconds, minutes, and hours time counters, an interrupt is generated. The interrupt output goes low if the alarm bit in the status register is set and the interrupt output is activated after an alarm time is sensed (see **PIN DESCRIPTIONS, $\overline{\text{INT}}$** pin). To preclude a false interrupt when loading the time counters, the alarm interrupt bit in the interrupt control register should be reset. This procedure is not required when the alarm time is being loaded.

WATCH-DOG FUNCTION

When Watch Dog (bit 7) in the interrupt control register is set high, the clock's slave select pin must be toggled at regular intervals without a serial data transfer. If SS is not toggled, the MC68HC68T1 supplies a CPU reset pulse at pin 2 and Watch-Dog (bit 6) in the status register is set. (See Figure 7.) Typical service and reset times are shown in Table 2.

CLOCK OUT

The value in the three least significant bits of the clock control register selects one of seven possible output frequencies. (See **CLOCK CONTROL REGISTER**.) This square-wave signal is available at the CLK OUT pin. When the power-down operation is initialized, the output is reset low.

CONTROL REGISTER AND STATUS REGISTER

The operation of the real-time clock is controlled by the clock control and interrupt control registers, which are read/write registers. Another register, the status register, is available to indicate the operating conditions. The status register is a read-only register.

MODE SELECT

The voltage level that is present at the V_{SYS} input pin at the end of power-on reset selects the device to be in the single-supply mode or battery-backup mode.

Single-Supply Mode

If V_{SYS} is powered up when power-on reset is completed, CLK OUT, PSE, and $\overline{\text{CPUR}}$ are enabled high and the device is completely operational. $\overline{\text{CPUR}}$ is placed low if the voltage level at the V_{SYS} pin subsequently goes 0.7 V below V_{DD}. If CLK OUT, PSE, and $\overline{\text{CPUR}}$ are reset low due to a power-down instruction, V_{SYS} brought low and then powered high enables these outputs.

An example of the single-supply mode is where only one supply is available and V_{DD}, V_{BATT}, and V_{SYS} are tied together to the supply.

Battery-Backup Mode

If V_{SYS} is not powered up at the end of power-on reset, CLK OUT, PSE, $\overline{CPUR}$, and SS are disabled (CLK OUT, PSE, and $\overline{CPUR}$ low). This condition is held until V_{SYS} rises to a threshold (approximately 0.7 V) above V_{BATT}. CLK OUT, PSE, and $\overline{CPUR}$ are then enabled and the device is operational. If V_{SYS} falls below a threshold above V_{BATT}, the outputs CLK OUT, PSE, and $\overline{CPUR}$ are reset low.

An example of battery-backup operation occurs if V_{SYS} is tied to V_{DD} and V_{DD} is not receiving voltage from a supply. A rechargeable battery is connected to the V_{BATT} pin. The device retains data and keeps time down to a minimum V_{BATT} voltage of 2.2 V.

POWER CONTROL

Power control is composed of two operations, power sense and power down/power up. Two pins are involved in power sensing, the LINE input pin and the $\overline{INT}$ output pin. Two additional pins, PSE and V_{SYS}, are utilized during power down/up operation.

FREEZE FUNCTION

The freeze function prevents an increment of the time counters, if any of the time registers are being read. Also, alarm operation is delayed if the time registers are being read.

POWER SENSING

When power sensing is enabled (Power Sense Bit in the interrupt control register), ac/dc transitions are sensed at the LINE input pin. Threshold detectors determine when transitions cease. After a delay of 2.68 to 4.64 ms plus the external input RC circuit time constant, an interrupt true bit is set high in the status register. This bit can then be sampled to see if system power has turned back on. (See Figure 8.)

The power-sense circuitry operates by sensing the level of the voltage present at the LINE input pin. This voltage is centered around V_{DD}, and as long as the voltage is either plus or minus a threshold (approximately 0.7 V) from V_{DD}, a power sense failure is not indicated. With an ac signal present, remaining in this V_{DD} window longer than a maximum of 4.64 ms activates the power-sense circuit. The larger the amplitude of the signal, the less likely a power failure would be detected. A 50 or 60 Hz, 10 V p-p sine-wave voltage is an acceptable signal to present at the LINE input pin to set up the power-sense function.

Power Down

Power down is a processor-directed operation. The power down bit is set in the interrupt control register to initiate power down operation. During power down, the power supply enable (PSE) output, normally high, is placed low. The CLK OUT pin is placed low. The $\overline{CPUR}$ output, connected to the processor reset input pin, is also placed low. In addition, the serial interface (MOSI and MISO) is disabled (see Figure 9).

Power Up

There are four methods that can initiate the power-up mode. Two of the methods require an interrupt to the microcomputer by programming the interrupt control register. The interrupts can be generated by the alarm circuit by setting the alarm bit and the appropriate alarm registers. Also, an interrupt can be generated by programming the periodic interrupt bits in the interrupt control register.

The third method is by initiating the power sense circuit with the power sense bit in the interrupt control register to sense power loss along with the V_{SYS} pin to sense subsequent power-up condition. (See Figure 10.) (Reference Figure 19 for application circuit for third method.)

The fourth method that initiates power-up occurs when the level on the V_{SYS} pin rises 0.7 V above the level of the V_{BATT} pin, after previously falling to the level of V_{BATT} while in the battery-backup mode. An interrupt is not generated when the fourth method is utilized.

While in the single-supply mode, power-up is initiated when the V_{SYS} pin loses power and then returns high. There is no interrupt generated when using this method (see Figure 11).

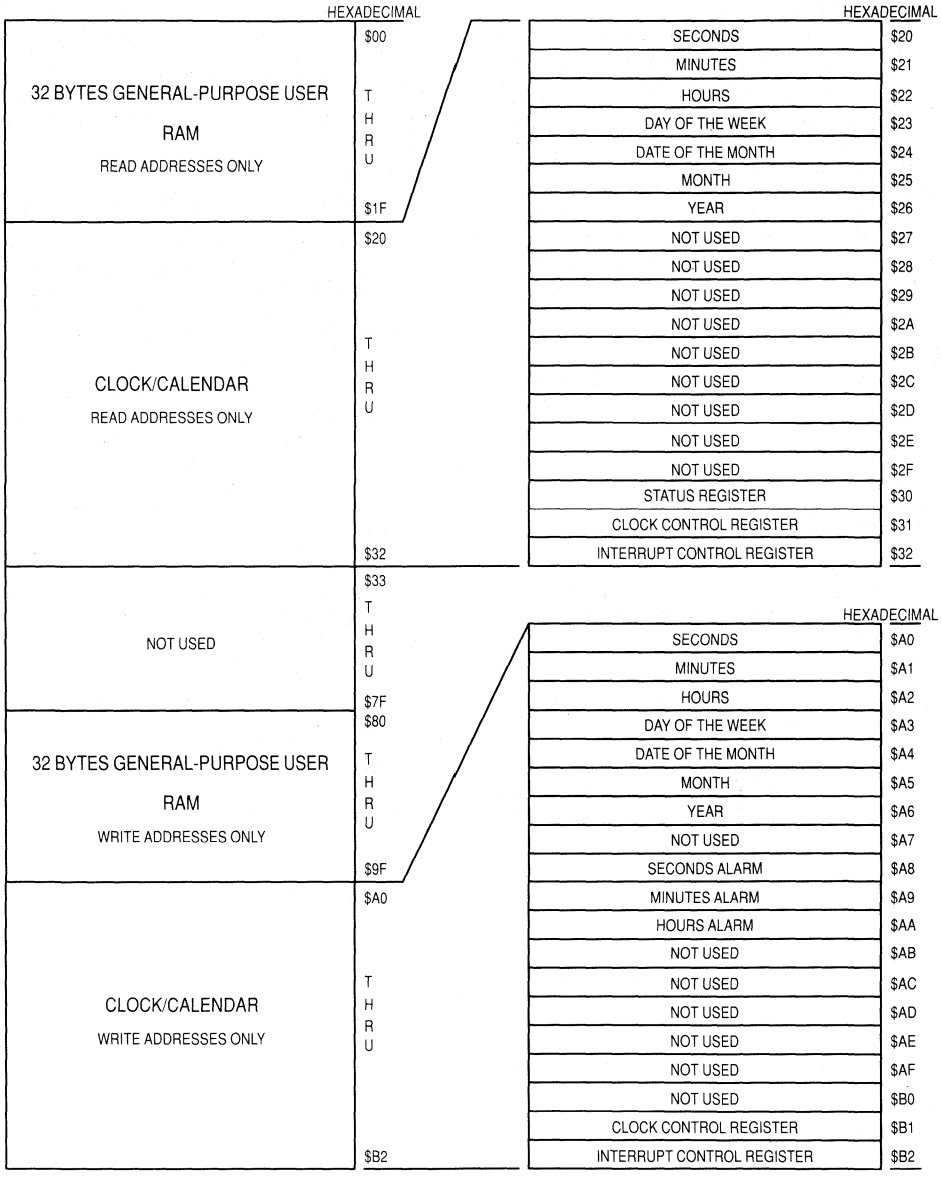


Figure 5. Address Map

Table 1. Clock/Calendar and Alarm Data Modes

Address Location		Function	Decimal Range	BCD Data Range	BCD Date* Example
Read	Write				
$20	$A0	Seconds	0–59	00–59	21
$21	$A1	Minutes	0–59	00–59	40
$22	$A2	Hours** (12 Hour Mode)	1–12	81–92 (AM) A1–B2 (PM)	90
		Hours (24 Hour Mode)	0–23	00–23	10
$23	$A3	Day of Week (Sunday = 1)	1–7	01–07	03
$24	$A4	Date of Month	1–31	01–31	16
$25	$A5	Month (Jan = 1)	1–12	01–12	06
$26	$A6	Year	0–99	00–99	87
N/A	$A8	Seonds Alarm	0–59	00–59	21
N/A	$A9	Minutes Alarm	0–59	00–59	40
N/A	$AA	Hours Alarm*** (12 Hour Mode)	1–12	01–12 (AM) 21–32 (PM)	10
		Hours Alarm (24 Hour Mode)	0–23	00–23	10

N/A = Not Applicable

*Example: 10:40:21 A.M., Tuesday, June 16, 1987.

**Most-Significant data bit, D7, is "0" for 24 hour mode and "1" for 12 hour mode. Data bit D5 is "1" for P.M. and "0" for A.M. in 12 hour mode.

***Data bit D5 is "1" for P.M. and "0" for A.M. in 12 hour mode. Data bits D7 and D6 are Don't Cares.

Table 2. Watchdog Service and Reset Times

	50 Hz		60 Hz		XTAL	
	Min	Max	Min	Max	Min	Max
Service Time	—	10 ms	—	8.3 ms	—	7.8 ms
Reset Time	20 ms	40 ms	16.7 ms	33.3 ms	15.6 ms	31.3 ms

HEX ADDRESS READ	HEX ADDRESS WRITE	WRITE/READ REGISTERS DB7	WRITE/READ REGISTERS DB0	FUNCTION
$20	$A0	TENS 0–5	UNITS 0–9	SECONDS (00–59)
$21	$A1	TENS 0–5	UNITS 0–9	MINUTES (00–59)
$22	$A2	12 HR / 24 X PM/AM TENS 0–2	UNITS 0–9	DB7, 1 = 12 HR, 0 = 24 HR DB5, 1 = PM, 0 = AM HOURS (01–12 OR 00–23)
$23	$A3	X X X X	X UNITS 1–7	DAY OF WEEK (01–07) SUNDAY = 1
$24	$A4	TENS 0–3	UNITS 0–9	DATE OF MONTH (01–31)
$25	$A5	TENS 0–1	UNITS 0–9	MONTH (01–12) JAN = 1
$26	$A6	TENS 0–9	UNITS 0–9	YEAR (00–99)
$31	$B1	7 6 5 4	3 2 1 0	CLOCK CONTROL REGISTER
$32	$B2	7 6 5 4	3 2 1 0	INTERRUPT CONTROL REGISTER

		WRITE-ONLY REGISTERS		
N/A	$A8	TENS 0–5	UNITS 0–9	SECONDS ALARM (00–59)
N/A	$A9	TENS 0–5	UNITS 0–9	MINUTES ALARM (00–59)
N/A	$AA	X X PM/AM TENS 0–2	UNITS 0–9	HOURS ALARM (01–21 OR 00–23) DB5, 1 = PM, 0 = AM IN 12 HR MODE

		READ-ONLY REGISTER		
$B0	N/A	7 6 5 4 3 2 1 0		STATUS REGISTER

		RAM DATA BYTE		
$00 TO $1F	$80 TO $9F	D7 D6 D5 D4 D3 D2 D1 D0		DATA

NOTE: X = Don't Care for write
X = 0 for read
N/A = Not Applicable

Figure 6. Clock/RAM Registers

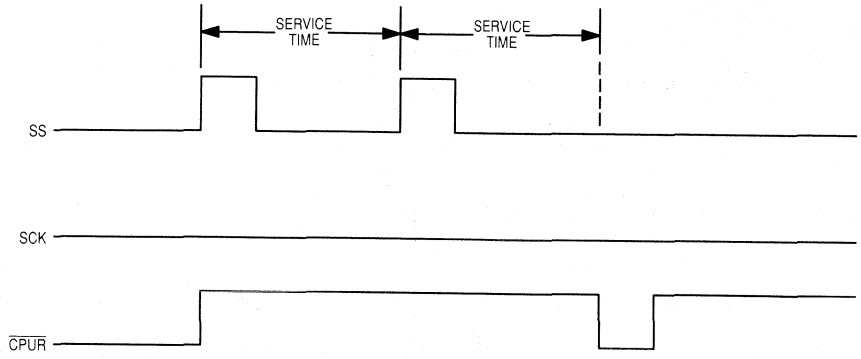
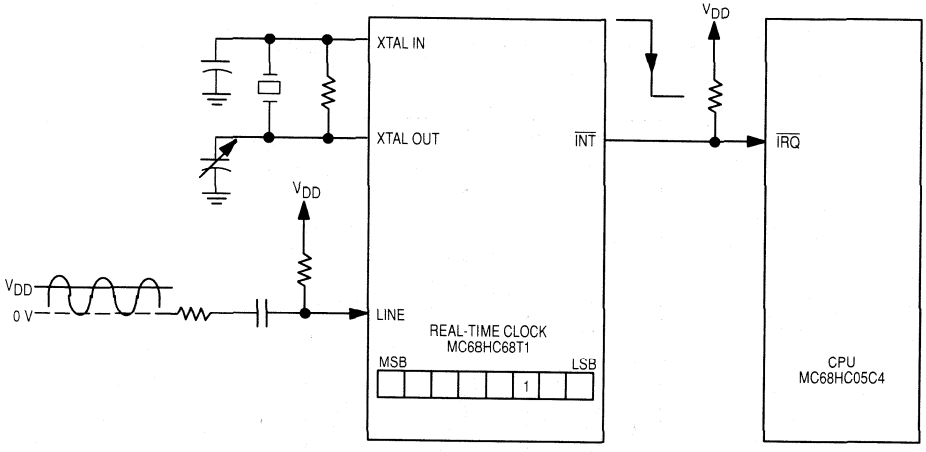


Figure 7. Watch-Dog Operation Waveforms



NOTE: A 60 Hz 10 V p-p sine-wave voltage is an acceptable signal to present at the LINE input pin.

Figure 8. Power Sensing Functional Diagram

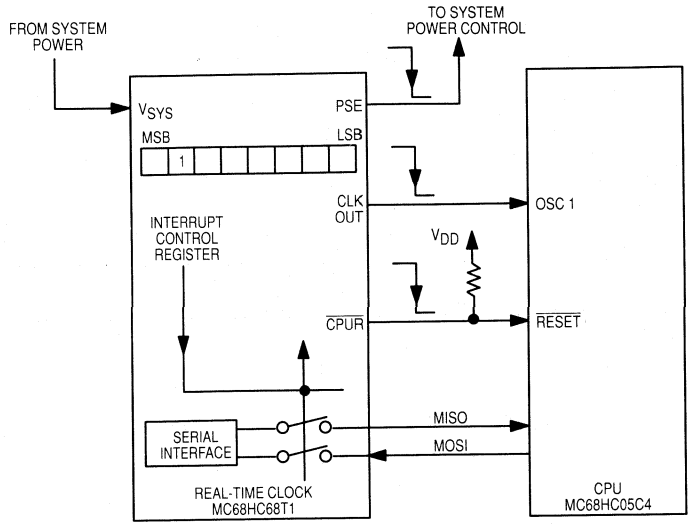
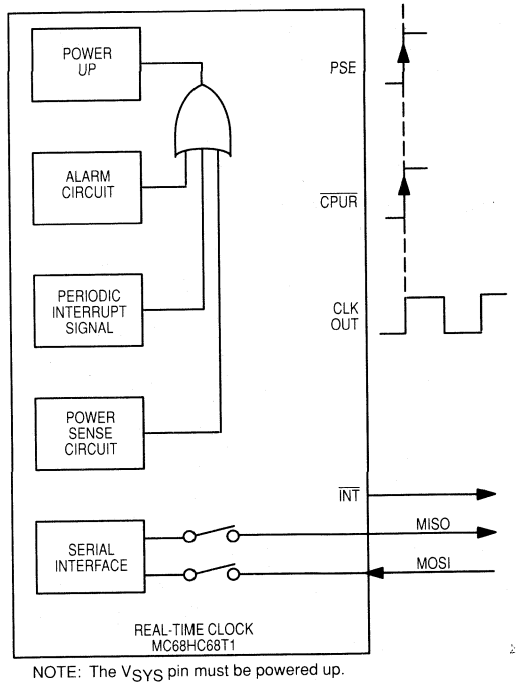


Figure 9. Power Down Functional Diagram



NOTE: The V_{SYS} pin must be powered up.

Figure 10. Power Up Functional Diagram (Initiated by Interrupt Signal)

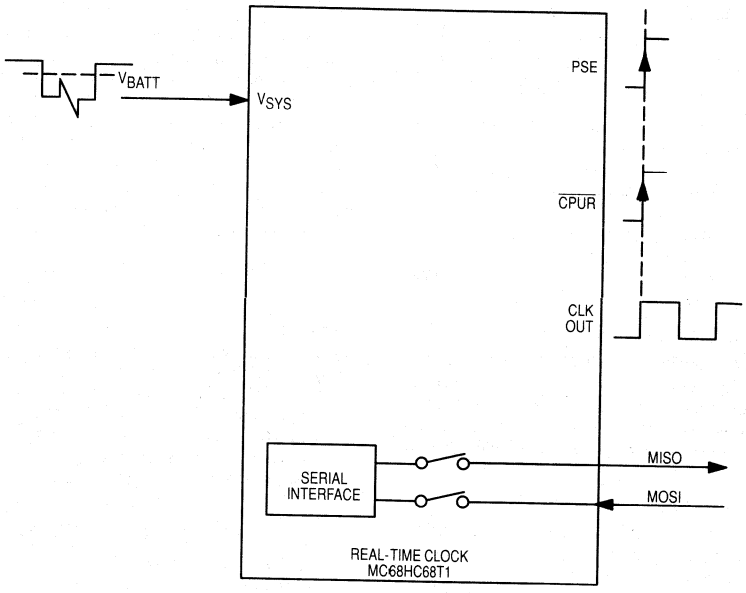


Figure 11. Power Up Functional Diagram (Initiated by a Rise in Voltage on the V_{SYS} Pin)

PIN DESCRIPTIONS

CLK OUT (PIN 1) — CLOCK OUTPUT

This signal is the buffered clock output which can provide one of the seven selectable frequencies (or this output can be reset low). The contents of the three least-significant bit positions in the clock control register determine the output frequency (50% duty cycle, except 2 Hz in the 50 Hz time-base mode). During power-down operation (Power Down bit in the interrupt control register set high), the clock output is reset low.

$\overline{\text{CPUR}}$ (PIN 2) — CPU RESET

This pin provides an N-channel, open-drain output and requires an external pullup resistor. This active low output can be used to drive the reset pin of a microprocessor to permit orderly power up/power down. The $\overline{\text{CPUR}}$ output is low from 15 to 40 ms when the watch-dog function detects a CPU failure (see Table 2). The low level time is determined by the input frequency source selected as the time standard. $\overline{\text{CPUR}}$ is reset low when power down is initiated.

This output has no ESD protection diode tied to V_{DD} which allows this pin's voltage to rise above V_{DD}. Care must be taken in handling this device.

$\overline{\text{INT}}$ (PIN 3) — INTERRUPT

This active-low output is driven from a single N-channel transistor and must be tied to an external pullup resistor. Interrupt is activated to a low level when any one of the following takes place:

1. Power sense operation is selected (Power Sense Bit in the interrupt control register is set high) and a power failure occurs.
2. A previously set alarm time occurs. The alarm bit in the status register and the interrupt signal are delayed 30.5 ms when 32 kHz or 1 MHz operation is selected, 15.3 ms for 2 MHz operation, and 7.6 ms for 4 MHz operation.
3. A previously selected periodic interrupt signal activates.

The status register must be read to disable the interrupt output after the selected periodic interval occurs. This is also true when conditions 1 and 2 activate the interrupt. If power down has been previously selected, the interrupt also sets the power-up function only if power is supplied to the V_{SYS} pin to the proper threshold level above V_{BATT}.

This output has no ESD protection diode tied to V_{DD} which allows this pin's voltage to rise above V_{DD}. Care must be taken in the handling of this device.

SCK (PIN 4) — SERIAL CLOCK

This serial clock input is used to shift data into and out of the on-chip interface logic. SCK retains its previous state if the line driving it goes into a high-impedance state. In other words, if the source driving SCK goes to the high-impedance state, the previous low or high level is retained by on-chip control circuitry.

MOSI (PIN 5) — MASTER OUT SLAVE IN

The serial data present at this port is latched into the interface logic by SCK if the logic is enabled. Data is shifted in, either on the rising or falling edges of SCK, with the most-significant bit (MSB) first.

In Motorola's microcomputers with SPI, the state of the CPOL bit determines which is the active edge of SCK. If SCK is high when SS goes high, the state of the CPOL bit is high. Likewise, if a rising edge of SS occurs while SCK is low (see Figure 13), then the CPOL bit in the microcomputer is low.

MOSI retains its previous state if the line driving it goes into high-impedance state. In other words, if the source driving MOSI goes to the high-impedance state, the previous low or high level is retained by on-chip control circuitry.

MISO (PIN 6) — MASTER IN SLAVE OUT

The serial data present at this port is shifted out of the interface logic by SCK if the logic is enabled. Data is shifted out, either on the rising or falling edge of SCK, with the most-significant bit (MSB) first. The state of the CPOL bit in the microcomputer determines which is the active edge of SCK. (See Figure 13.)

SS (PIN 7) — SLAVE SELECT

When high, the slave select input activates the interface logic, otherwise the logic is in a reset state and the MISO pin is in the high-impedance state. The watch-dog circuit is toggled at this pin. SS has an internal pulldown device. Therefore, if SS is in a low state before going to high impedance, SS can be left in a high-impedance state. That is, if the source driving SS goes to the high-impedance state, the previous low level is retained by on-chip control circuitry.

V_{SS} (PIN 8) — NEGATIVE POWER SUPPLY

This negative power supply reference pin is connected to ground.

PSE (PIN 9) — POWER SUPPLY ENABLE

The power supply enable output is used to control system power and is enabled high under any one of the following conditions:

1. V_{SYS} rises above the V_{batt} voltage after V_{SYS} is reset low by a system failure.
2. An interrupt occurs (if the V_{SYS} pin is powered up 0.7 V above V_{BATT}).
3. A power-on reset occurs (if the V_{SYS} pin is powered up 0.7 V above V_{BATT}).

PSE is reset low by writing a high into the power-down bit of the interrupt control register.

$\overline{POR}$ (PIN 10) — POWER-ON RESET

This active-low Schmitt-trigger input generates an internal power-on reset signal using an external RC network. (See Figures 18 through 21). Both control registers and frequency dividers for the oscillator and line inputs are reset. The status register is reset except for the first time-up bit (bit 4), which is set high. At the end of the power-on reset, single-supply or battery-backup mode is selected.

LINE (PIN 11) — LINE SENSE

The LINE sense input can be used to drive one of two functions. The first function utilizes the input signal as the frequency source for the timekeeping counters. This function is selected by setting the line/$\overline{XTAL}$ bit high in the clock control register. The second function enables the LINE input to detect a power failure. Threshold detectors operating above and below V_{DD} sense an ac voltage loss. The Power Sense bit in the interrupt control register must be set high and crystal or external clock source operation is required. The line/$\overline{XTAL}$ bit in the clock control register must be low to select crystal operation.

V_{SYS} (PIN 12) — SYSTEM VOLTAGE

This input is connected to system voltage. The level on this pin initiates power up if it rises 0.7 V above the level at the V_{BATT} input pin after previously falling below 0.7 V below V_{BATT}. When power-up is initiated, the PSE pin returns high and the CLK OUT pin is enabled. The $\overline{CPUR}$ output pin is also set high. Conversely, if the level of the V_{SYS} pin falls below V_{BATT} + 0.7 V, the PSE, CLK OUT, and $\overline{CPUR}$ pins are placed low. The voltage level present at this pin at the end of $\overline{POR}$ determines the device's operating mode.

V_{BATT} (PIN 13) — BATTERY VOLTAGE

This pin is the *only* oscillator power source and should be connected to the positive terminal of a rechargeable battery. **The V_{BATT} pin always supplies power to the MC68HC68T1, even when the device is not in the battery back-up mode.** To maintain timekeeping, the V_{BATT} pin must be at least 2.2 V. When the level on the V_{SYS} pin falls below V_{BATT} + 0.7 V, **V_{BATT} is internally connected to the V_{DD} pin.**

When the LINE input is used as the frequency source, the unused V_{BATT} and XTAL pins may be tied to V_{SS}. Alternatively, if V_{BATT} is connected to V_{DD}, XTAL IN can be tied to either V_{SS} or V_{DD}.

XTAL IN (PIN 14), XTAL OUT (PIN 15) — CRYSTAL INPUT/OUTPUT

For crystal operation, these two pins are connected to a 32.768 kHz, 1.048576 MHz, 2.097152 MHz, or 4.194304 MHz crystal. If crystal operation is not desired and Line Sense is used as frequency source, connect XTAL IN to V_{DD} or V_{SS} (caution: see V_{BATT} pin description) and leave XTAL OUT open. If an external clock is used, connect the external clock to XTAL IN and leave XTAL OUT open. The external clock must swing from at least 30% to 70% of (V_{DD}-V_{SS}). Preferably, this input should swing from V_{SS} to V_{DD}.

V_{DD} (PIN 16) — POSITIVE POWER SUPPLY

For full functionality, the positive power supply pin may range from 3.0 to 6.0 V with respect to V_{SS}. To maintain timekeeping, the minimum standby voltage is 2.2 V with respect to V_{SS}. **(Caution: Data transfer to/from the MC68HC68T1 must not be attempted if the supply voltage falls below 3.0 V.)**

REGISTERS

CLOCK CONTROL REGISTER (READ/WRITE) — READ ADDRESS $31/WRITE ADDRESS $B1

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
START / STOP	LINE / XTAL	XTAL SELECT 1	XTAL SELECT 0	50 Hz / 60 Hz	CLK OUT 2	CLK OUT 1	CLK OUT 0

Start-Stop

A high written into this bit enables the counter stages of clock circuitry. A low holds all bits reset in the divider chain from 32 Hz to 1 Hz. The clock out signal selected by bits D0, D1, and D2 is not affected by the stop function except the 1- and 2-Hz outputs.

Line-XTAL

When this bit is high, clock operation uses the 50 or 60 cycle input present at the LINE input pin. When the bit is low, the XTAL IN pin is the source of the time update.

XTAL Select

Accommodation of one of four possible crystals are selected by the value in bits D4 and D5.

0 = 4.194304 MHz
1 = 2.097152 MHz
2 = 1.048576 MHz
3 = 32.768 kHz

The MC68HC68T1 has an on-chip 150 K resistor that is switched in series with the internal inverter when 32 kHz is selected via the clock control register. This eliminates the usual external series requirement present in 32 kHz circuits. At power up, the device sets up for a 4 MHz oscillator and the series resistor is not part of the oscillator circuit. Until this resistor is switched in, oscillations may be unstable with the 32 kHz crystal. (See Figure 12.)

Resistor R1 is recommended to be 22 MΩ for 32 kHz operation. Consult crystal manufacturer for R1 value for other frequencies. Resistor R2 is used for 32 kHz operation only. Use a 100 kΩ to 300 kΩ range as specified by the crystal manufacturer.

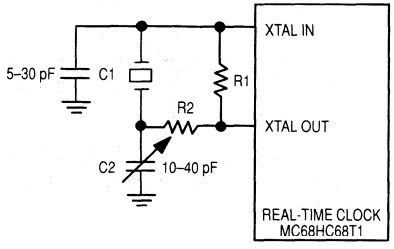


Figure 12. Recommended Oscillator Circuit (C1, C2 Values Depend Upon the Crystal Frequency)

50 Hz-60 Hz

50 Hz may be used as the input frequency at the LINE input when this bit is set high; a low accommodates 60 Hz. The power sense bit in the interrupt control register must be reset low for line frequency operation.

Clock Out

Three bits specify one of the seven frequencies to be used as the square-wave clock output (CLK OUT).

0 = XTAL
1 = XTAL/2
2 = XTAL/4
3 = XTAL/8
4 = Disable (low output)
5 = 1 Hz
6 = 2 Hz
7 = 50/60 Hz for LINE operation
7 = 64 Hz for XTAL operation

All bits in the clock control register are reset by a power-on reset. Therefore, XTAL is selected as the clock output at this time.

INTERRUPT CONTROL REGISTER (READ/WRITE) — READ ADDRESS $32/WRITE ADDRESS $B2

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
WATCH-DOG	POWER DOWN	POWER SENSE	ALARM	PERIODIC SELECT			

All bits are reset low by power-on reset.

Watch Dog

When this bit is set high, the watch-dog operation is enabled. This function requires the CPU to toggle the SS pin periodically without a serial transfer requirement. In event this does not occur, a CPU reset is issued at the CPUR pin. The status register must be read before re-enabling the watch-dog function.

Power Down

A high in this location initiates a power down. A CPU reset occurs via the CPUR output, the CLK OUT and PSE output pins are reset low, and the serial interface is disabled.

Power Sense

When set high, this bit is used to enable the LINE input pin to sense a power failure. When power sense is selected, the input to the 50/60 Hz prescaler is disconnected; therefore, crystal operation is required. An interrupt is generated when a power failure is sensed and the power sense and interrupt true bit in the status register are set. When power sense is activated, a logic low must be written to this location followed by a high to re-enable power sense.

Alarm

The output of the alarm comparator is enabled when this bit is set high. When an equal comparison occurs between the seconds, minutes, and hours time counters and alarm latches, the interrupt output is activated. When loading the time counters, this bit should be reset low to avoid a false interrupt. This is not required when loading the alarm latches. See INT pin description for explanation of alarm delay.

Periodic Select

The value in these four bits (D0, D1, D2, and D3) selects the frequency of the periodic output. (See Table 3).

Table 3. Periodic Interrupt Output Frequencies (at $\overline{INT}$ Pin)

D3–D0 Value (Hex)	Periodic Interrupt Output Frequency	Frequency Timebase	
		XTAL	Line
0	Disable		
1	2048 Hz	X	
2	1024 Hz	X	
3	512 Hz	X	
4	256 Hz	X	
5	128 Hz	X	
6	64 Hz	X	
	50 or 60 Hz		X
7	32 Hz	X	
8	16 Hz	X	
9	8 Hz	X	
A	4 Hz	X	
B	2 Hz	X	X
C	1 Hz	X	X
D	1 Cycle per Minute	X	X
E	1 Cycle per Hour	X	X
F	1 Cycle per Day	X	X

STATUS REGISTER (READ ONLY) — ADDRESS $30

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
0	WATCH-DOG	0	FIRST TIME UP	INTER-RUPT TRUE	POWER SENSE INT	ALARM INT	CLOCK INT

Watch Dog

If this bit is set high, the watch-dog circuit has detected a CPU failure.

First Time Up

Power-on reset sets this bit high. This signifies the data in the RAM and Clock is not valid and should be initialized. After the status register is read, the first time-up bit is set low if the $\overline{POR}$ pin is high. Conversely, if the $\overline{POR}$ pin is held low, the first time-up bit remains set high.

Interrupt True

A high in this bit signifies that one of the three interrupts (power sense, alarm, or clock) is valid.

Power-Sense Interrupt

This bit set high signifies that the power sense circuit has generated an interrupt. This bit is not reset after a read of this register.

Alarm Interrupt

When the contents of the seconds, minutes, and hours time counters and alarm latches are equal, this bit is set high. The status register must be read before loading the interrupt control register for valid alarm indication after the alarm activates.

Clock Interrupt

A periodic interrupt sets this bit high. (See Table 3.)

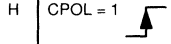
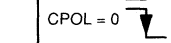
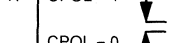
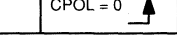
All bits are reset low by a power-on reset except the first time-up bit which is set high. All bits except the power sense bit are reset after a read of the status register.

SERIAL PERIPHERAL INTERFACE (SPI)

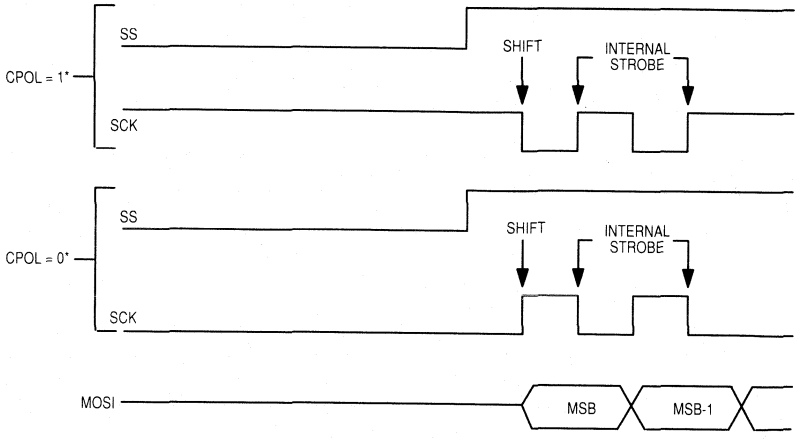
The serial peripheral interface (SPI) utilized by the MC68HC68T1 is a serial synchronous bus for address and data transfers. The shift clock (SCK), which is generated by the microcomputer, is active only during address and data transfer. In systems using the MC68HC05C4 or MC68HC11A8, the inactive clock polarity is determined by the clock polarity (CPOL) bit in the microcomputer's control register.

A unique feature of the MC68HC68T1 is that the level of the inactive clock is determined by sampling SCK when SS becomes active. Therefore, either SCK polarity is accommodated. Input data (MOSI) is latched internally on the internal strobe edge and output data (MISO) is shifted out on the shift edge (see Table 4 and Figure 13). There is one clock for each bit transferred. Address as well as data bits are transferred in groups of eight.

Table 4. Function Table

Mode	Signal			
	SS	SCK	MOSI	MISO
Disabled Reset	L	Input Disabled	Input Disabled	High Z
Write	H	CPOL = 1  CPOL = 0 	Data Bit Latch	High Z
Read	H	CPOL = 1  CPOL = 0 	X	Next Data Bit Shifted Out*

*MISO remains at a High Z until eight bits of data are ready to be shifted out during a read. MISO remains at a High Z during the entire write cycle.



*CPOL is a bit that is set in the microcomputer's Control Register.

Figure 13. Serial Clock (SCK) as a Function of MCU Clock Polarity (CPOL)

ADDRESS AND DATA FORMAT

There are three types of serial transfers:

1. Read or write address
2. Read or write data
3. Watch-dog reset (actually a non-transfer)

The address and data bytes are shifted MSB first, into the serial data input (MOSI) and out of the serial data output (MISO). Any transfer of data requires the address of the byte to specify a write or read Clock or RAM location, followed by one or more bytes of data. Data is transferred out of MISO for a read operation and into MOSI for a write operation. (See Figures 14 and 15.)

Address Byte

The address byte is always the first byte entered after SS goes true. To transmit a new address, SS must first be brought low and then taken high again.

MSB							LSB
A7	A6	A5	A4	A3	A2	A1	A0

A7 — High initiates one or more write cycles. Low initiates one or more read cycles.

A6 — Must be low (zero) for normal operation

A5 — High signifies a clock/calendar location. Low signifies a RAM location

A0-A4 — Remaining address bits. (See Figure 5.)

Address and Data

Data transfers can occur one byte at a time or in multi-byte burst mode. (See Figures 16 and 17). After the MC68HC68T1 is enabled (SS = high), an address byte selects either a read or a write of the Clock/Calendar or RAM. For a single-byte read or write, one byte is transferred to or from the Clock/Calendar register or RAM location specified by an address. Additional reading or writing requires re-enabling the device and providing a new address byte. If the MC68HC68T1 is not disabled, additional bytes can be read or written in a burst mode. Each read or write cycle causes the Clock/Calendar register or RAM address to automatically increment. Incrementing continues after each byte transfer until the device is disabled. After incrementing to $1F or $9F, the address wraps to $00 and continues if the RAM is selected. When the Clock/Calendar is selected, the address wraps to $20 after incrementing to $32 or $B2.

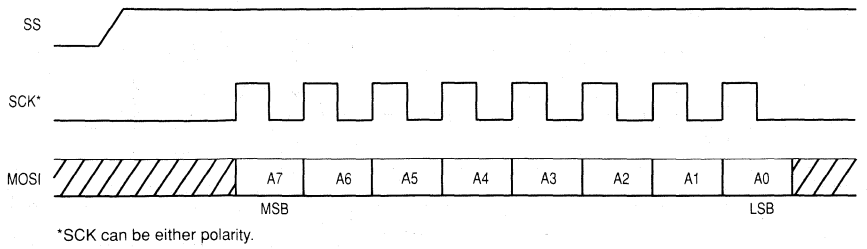


Figure 14. Address Byte Transfer Waveforms

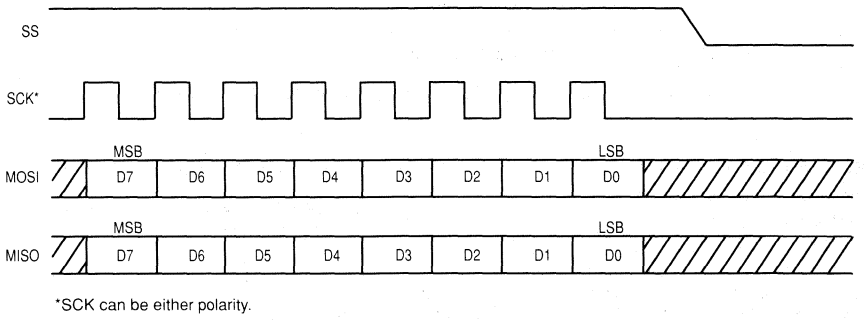


Figure 15. Read/Write Data Transfer Waveforms

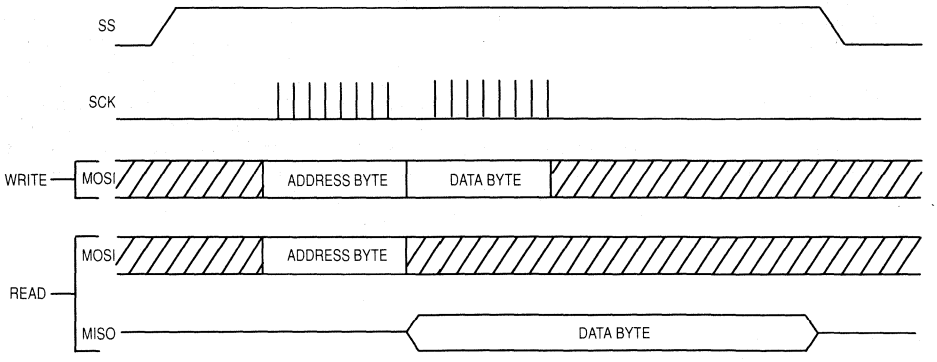


Figure 16. Single-Byte Transfer Waveforms

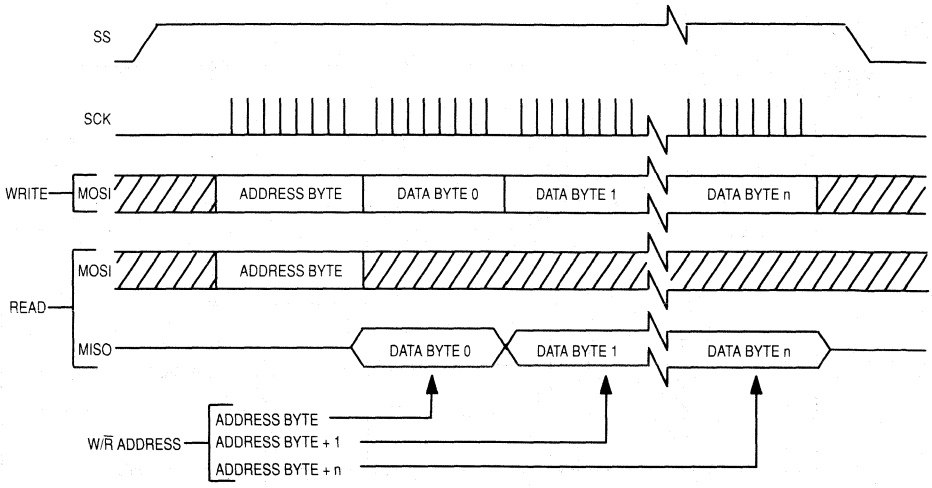
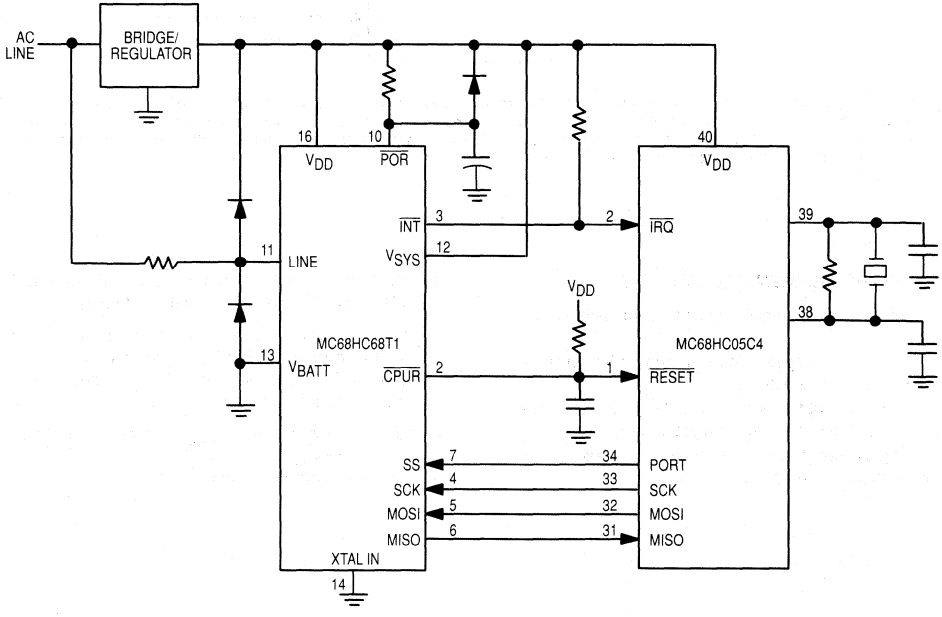
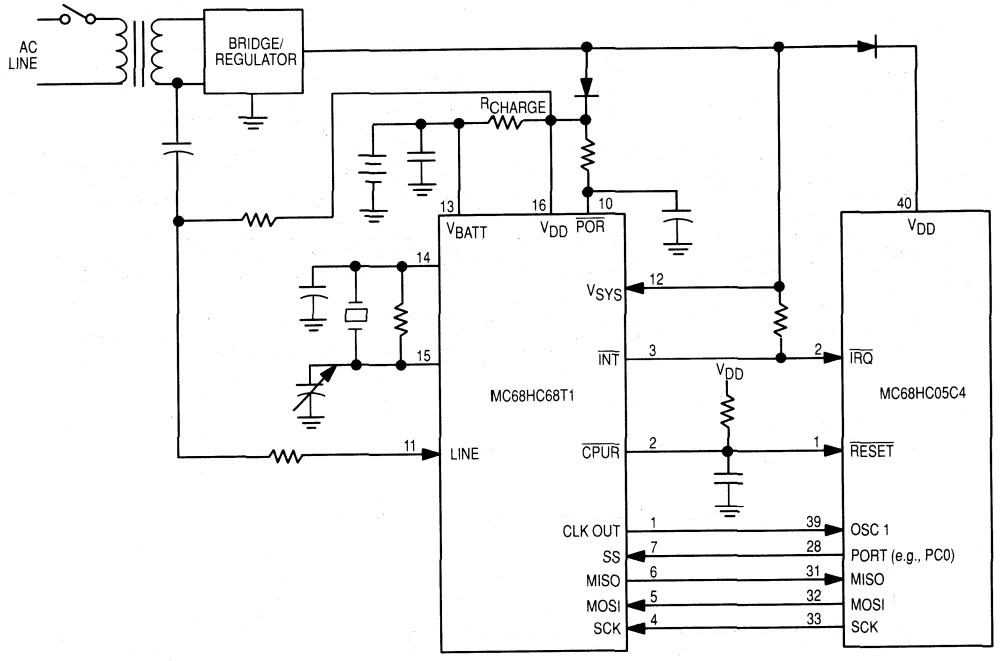


Figure 17. Multiple-Byte Transfer Waveforms



NOTE: Clock circuit driven by line input frequency. Power-on reset circuit included to detect power failure.

Figure 18. Power-Always-On System



NOTE: The LINE input pin can sense when the switch opens by use of the power sense interrupt. The MC68HC68T1 crystal drives the clock input to the CPU using the CLK OUT pin. On power down when $V_{SYS} < V_{BATT} + 0.7$ V, V_{BATT} powers the clock. A threshold detect activates an on-chip p-channel switch, connecting V_{BATT} to V_{DD}. V_{BATT} always supplies power to the oscillator, keeping voltage frequency variation to a minimum.

POWER-DOWN PROCEDURE

A procedure for power-down operation consists of the following:

1. Set power sense operation by writing bit 5 high in the interrupt control register.
2. When an interrupt occurs, the CPU reads the status register to determine the interrupt source.
3. Sensing a power failure, the CPU does the necessary housekeeping to prepare for shutdown.
4. The CPU reads the status register again after several milliseconds to determine validity of power failure.
5. The CPU sets power down (bit 6) and disables all interrupts in the interrupt control register when power down is verified. This causes the CPU reset and Clock Out pins to be held low and disconnects the serial interface.
6. When power returns and V_{SYS} rises above V_{BATT} + 0.7 V, power up is initiated. The CPU reset is released and serial communication is established.

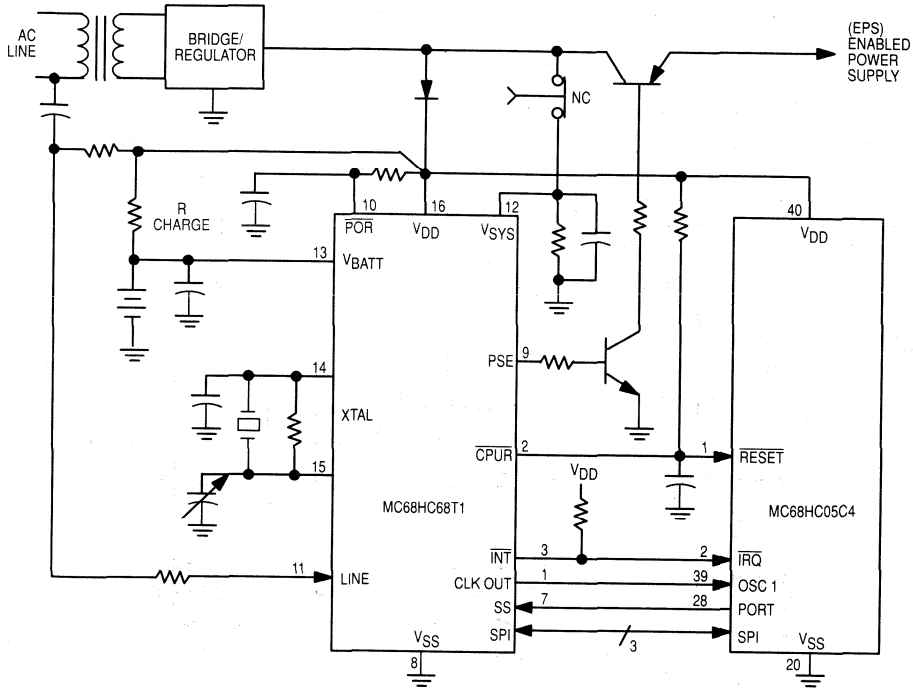
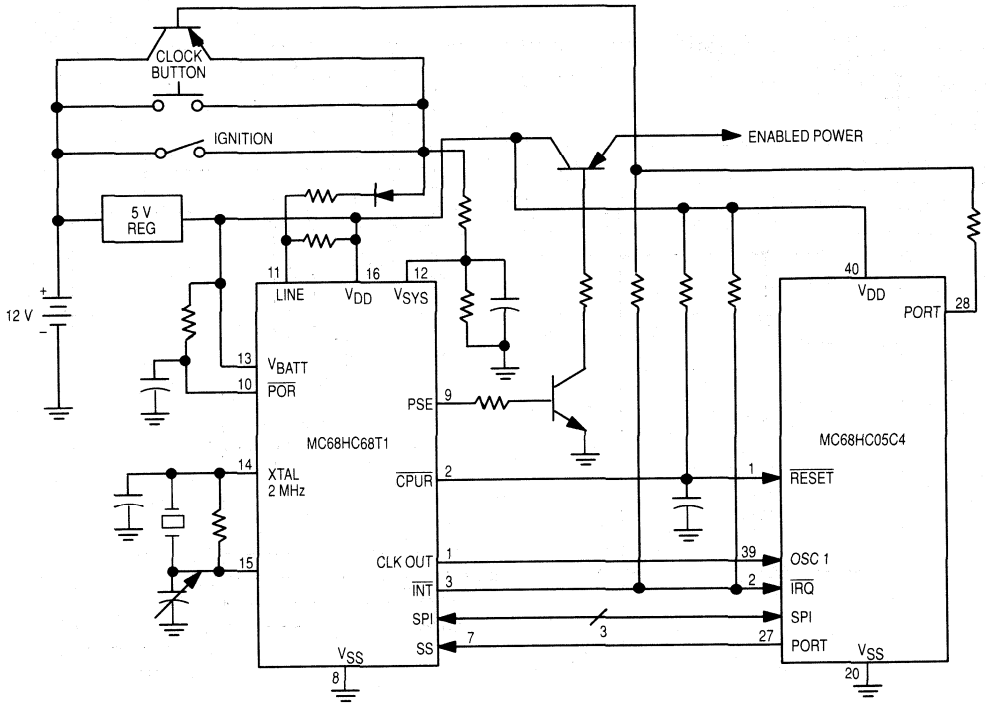


Figure 20. Battery Back-Up System



NOTE: The V_{SYS} and Line inputs can be used to sense the ignition turning on and off. An external switch is included to activate the sytem without turning on the ignition. Also, the CMOS CPU is not powered down with the system V_{DD}, but is held in a low power reset mode during power down. When restoring power, the MC68HC68T1 enables the CLK OUT pin and sets the PSE and $\overline{CPUR}$ pins high.

Figure 21. Automotive System

MC141620

Advance Information

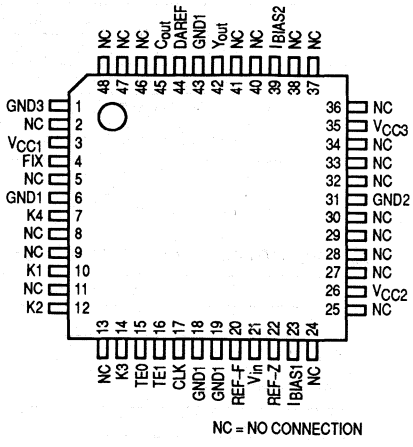
Enhanced Comb Filter
CMOS

The enhanced comb filter is a video signal processor for television and video recorder applications. The device separates the luminance Y and chrominance C from the NTSC composite video signal by using digital signal processing techniques. This filter allows an extended frequency bandwidth of the luminance signal while minimizing the common comb-filter problems such as dot-crawl and cross-color. This chip easily connects to analog TV and VCR chips due to the on-board A/D and D/A converters.

- Fast 8-Bit A/D Converter
- Two Line-Delay Memories
- Enhanced Combing Process
- Two 8-Bit D/A Converters
- Utilizes NTSC 4fsc (sub-carrier frequency) Clock

FU SUFFIX
QFP
CASE TBD

ORDERING INFORMATION
MC141620FU Quad Flat Package



NC = NO CONNECTION

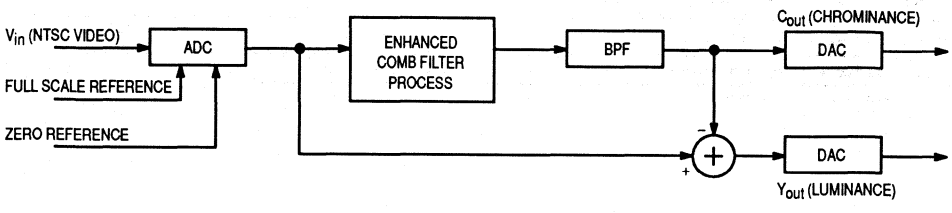


Figure 1. Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Symbol	Characteristic	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current (per pin)	±20	mA
I_{out}	DC Output Current (per pin)	±25	mA
I_{CC}	DC Supply Current (V_{CC} and GND pins)	±100	mA
P_D	Power Dissipation	750	mW
T_{stg}	Storage Temperature	−65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

GENERAL ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C Unless Otherwise Noted)

Symbol	Characteristic	Min	Max	Unit
V_{CC}	Supply Voltage (V_{CC1}, V_{CC2}, V_{CC3})	4.5	5.5	V
I_{CC}	Operating Supply Current	—	75	mA
P_D	Operating Power Dissipation	—	420	mW
T_A	Ambient Operating Temperature	−20	80	°C
t_d	Total Signal Delay	—	64.95*	µs

*Nominal value. System clock for 930.5 cycles.

ADC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Characteristic	Min	Typ*	Max	Unit
Resolution	8	—	—	Bits
Integral Nonlinearity	—	—	±1.5	LSB
Differential Nonlinearity	—	—	±1.0	LSB
Analog Input Level	—	—	3.0	V p-p
Full-Scale Reference Level	REF-Z	V_{CC2} − 0.4	V_{CC2} − 0.3	V
Zero Reference Level	1.4	1.6	REF-F	V
Reference Resistor Value (between REF-F & REF-Z)	—	380	600	Ω
Bias Current (Resistor = 10 kΩ)	—	120	—	µA
Input Capacitance (Design Ref. Value)	—	35	—	pF

*Data labeled "typ" is not guaranteed.

CLOCK INPUT ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Characteristic	Min	Max	Unit
Clock Frequency (Note 1)	12	15	MHz
Clock Jitter	—	2.0	ns
Input Level (Figure 8)	0.20	5.0	V p-p

Note 1 — This signal is usually 14.31818 MHz

FILTERING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Characteristic	Min	Max	Unit
Y/C Separation (clock jitter < 2.0 ns)	—	40*	dB

*Typical value. Not guaranteed.

DAC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Characteristic	Min	Max	Unit
Resolution	8	—	Bits
Output Bandwidth (at –3.0 dB)	5.5	—	MHz
Integral Nonlinearity	—	±1.0	LSB
Differential Nonlinearity	—	±0.3	LSB
Differential Gain	—	5.0	%
Differential Phase	—	5.0	Deg
Analog Output Voltage, Y_{out}	1.1	1.3	V p-p
Analog Output Voltage, C_{out}	1.1	1.3	V p-p
Full Scale Voltage, Y_{out}	1.3	1.7	V
Full Scale Voltage, C_{out}	1.3	1.7	V
Zero Scale Voltage, Y_{out}	0.1	0.5	V
Zero Scale Voltage, C_{out}	0.1	0.5	V
Bias Current [DAC only] — Resistor = 10 kΩ	120*	—	μA
Output Impedance	—	300	Ω

*Typical value. Not guaranteed.

DIGITAL ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Symbol	Characteristic	Min	Max	Unit
V_{IH}	High Level Input Voltage (K1 ~ K4, FIX)	3.15	—	V
V_{IL}	Low Level Input Voltage (K1 ~ K4, FIX)	—	1.1	V
I_{IH}	High Level Input Current (K1 ~ K4, FIX)	—	0.1	μA
I_{IL}	Low Level Input Current (K1 ~ K4, FIX)	—	0.1	μA

PIN DESCRIPTIONS

V_{CC1} (Pin 3)
+5.0 V ± 10% dc power supply for the digital circuits.

V_{CC2} (Pin 26)
+5.0 V ± 10% dc power supply for the ADC.

V_{CC3} (Pin 35)
+5.0 V ± 10% dc power supply for the DAC.

GND1 (Pins 6, 18, 19, 43)
Ground for the digital circuits. For optimum performance, all pins must be tied to ground.

GND2 (Pin 31)
Ground for the ADC.

GND3 (Pin 1)
Ground for the DAC.

CLK (Pin 17)
4fsc (sub-carrier frequency) 14.31818 MHz input. This signal is usually ac-coupled through an external capacitance. See User Information. The clock signal must synchronize with the NTSC video signal.

V_{in} (Pin 21)
Composite video signal input. The composite video signal, clamped externally, should be supplied with dc coupling. The video input level should be nominally 3.0 V p-p. Input signal bandwidth should be limited to less than 1/2 of the frequency of the sampling clock by anti-aliasing filtering, etc.

REF-F (Pin 20)
ADC reference for the full-scale voltage.

REF-Z (Pin 22)
ADC reference for the zero input voltage.

DAREF (Pin 44)
Reference for the luminance and chrominance DACs. Insert a capacitor of 0.1 µF between DAREF and GND3.

I_{BIAS1} (Pin 23)
ADC bias circuit current control. Insert a resistor of 10 kΩ between I_{BIAS1} and GND2.

I_{BIAS2} (Pin 39)
DAC bias circuit current control. Insert a resistor of 10 kΩ between I_{BIAS2} and GND3.

Y_{out} (Pin 42)
Luminance output. This output signal is fed into the general analog VCR/TV system. Typical output voltage is 1.2 V p-p swinging from 0.3 V to 1.5 V.

C_{out} (Pin 45)
Chrominance output. This output signal is fed into the general analog VCR/TV system. Typical output voltage is 1.2 V p-p swinging from 0.3 V to 1.5 V.

TE0 (Pin 15)
Test enable pin. If this pin is a high level, the test mode is enabled. This pin must be grounded by the user.

TE1 (Pin 16)
Test select pin. This pin must be grounded by the user.

FIX (Pin 4)
Filter mode select pin. It must be a high level for the normal mode. Comb filter/bandpass filter fixed mode can be selected by the K1 pin. Each mode is shown below.

FIX	K1	MODE
H	H	Normal mode
H	L	Normal mode
L	H	Bandpass filter fixed mode
L	L	Comb filter fixed mode

K1, K2, K3, and K4 (Pins 10, 12, 14, 7)
K factor inputs. These pins are provided to set up the K value for the select control circuit, and to set up the threshold level of comb filter and bandpass filter. Each input (K1 ~ K4) are assigned to b1 ~ b4 of the K factor. Input must be at CMOS levels. The assignment of K pins are shown below. Also, when the FIX pin is at a low level, the K1 pin becomes a filter mode select pin. If the K1 pin is low, the comb filter is enabled; otherwise, the bandpass filter is enabled.

b0	b1	b2	b3	b4	b5	b6	b7
L	K1	K2	K3	K4	H	H	L

OVERVIEW

The enhanced comb filter is a high performance HCMOS digital filter combined with A/D and D/A converters. The basic functions of this chip are the separation of the luminance Y and chrominance C signals from the NTSC video signal which is composed of luminance and chrominance components interleaved with each other in the same frequency band.

The visual performance advantages of the enhanced comb filter are that the chip eliminates the sub-carrier dot-crawl from the luminance channel in large color areas and eliminates the cross color from the chrominance in high frequency luminance areas. Also, the horizontal resolution of the picture is allowed from zero to an arbitrary high by this chip. The Y/C separation is performed by a combination of a digital 2H comb filter and a digital bandpass filter.

To perform the enhanced combing process, two horizontal scan line delay memories for a 2H comb filter, several pairs of latches for a bandpass filter, and selective control circuitry are provided. The 2H comb filter separates the chrominance components from the composite video signal by integration of 3 successive lines. However, when the comb filter is performing the line integration, the horizontal color smears on the boundary. This chip solves the color smear and dot-crawl problems while keeping the advantages of 2H comb filter by selecting one filter process from the bandpass filter or the 2H comb filter at a particular picture transition.

Enhanced Comb Filter Description

Figure 1 shows the block diagram of the enhanced comb filter chip. There are three major functions on this block diagram.

The first is the analog-to-digital conversion block. One 8-bit binary A/D converter is provided for digitizing the incoming analog video signal to 8-bit binary data. The conversion frequency is 14.3 MHz which is four times the color sub-carrier frequency. The analog video input is nominally 3.0 V p-p.

The second is the digital filters and selective control block. There are two digital filters on this block which are vertical filter (2H comb filter) and horizontal filter (bandpass filter). The selective control determines which type of filter should be chosen for the current process.

The third is the digital-to-analog conversion block. Two 8-bit D/A converters are provided for the luminance and chrominance analog output. The conversion frequency is four times the sub-carrier signal (14.3 MHz). The chrominance analog output has a dc offset bias of half the maximum output voltage.

Algorithm of Enhanced Comb Filter

Figure 2 illustrates the basic principles of the Y/C separation algorithm. The NTSC video signal has an alternate relationship in the horizontal and vertical direction on the sampled data array. V1 through V9 in Figure 2 represent a sampled data array of an appropriate area of the screen. The sampling frequency is four times the sub-carrier frequency (14.3 MHz). There are four data samples in one sub-carrier cycle, and the sub-carrier phase is reversed every scan line. In other words, V1 and V7 have same phase and V4 is reversed; V2 and V8 have same phase and V5 is reversed. Also, the sampled data V1 through V3 are placed on scan line N, V4 through V6 are on N-1, and so on. On the individual lines, every four data samples have the same phase — for instance, V1 and V3, V4 and V6, and so forth.

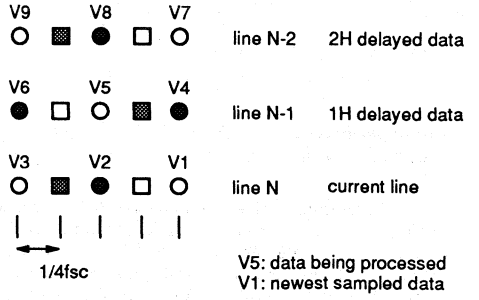


Figure 2.

Vertical Filtering

The typical vertical filter is a comb filter which may use 1H or 2H scan line delay. The comb filter integrates successive scan line data to separate Y and C. The formula is:

$$\text{Chrominance} = (V5 - (V2 + V8) / 2) / 2 \times H_{BPF}$$

$$\text{Luminance} = V5 - \text{Chrominance}$$

Where H_{BPF} is the BPF transfer function.

The combing process allows the luminance signal separation for the extension of the frequency bandwidth. However, the integration of the successive lines causes a loss of vertical resolution. The combing process causes color smears on the line, if there is color transition between the lines. It can be observed as color smear on the color boundary or horizontal running dot-crawl.

Horizontal Filtering

The conventional filtering, such as a bandpass filter, has typical dot-crawl and cross-color problems. Even the digital horizontal filtering has similar problems. However, the MC141620's digital horizontal filtering yields superior performance over a regular bandpass filter. The formula is:

$$\text{Chrominance} = (V5 - (V4 + V6) / 2) / 2 \times H_{BPF}$$

$$\text{Luminance} = V5 - \text{Chrominance}$$

Where H_{BPF} is the BPF transfer function.

Enhanced Comb Filtering (Combination of Vertical and Horizontal Filtering)

This is a combination approach of the vertical filtering and horizontal filtering so that the overall filtering can take advantage of both filters. The algorithm of this filter is as follows:

If $|V8 - V2| + K \leq |V6 - V4|$
(Vertical Transition ≤ Horizontal Transition)

K: constant value

then Chrominance = $(V5 - (V2 + V8) / 2) / 2 \times H_{BPF}$
— Vertical Filter

If $|V8 - V2| + K > |V6 - V4|$
(Vertical Transition > Horizontal Transition)

then Chrominance = $(V5 - (V6 + V4) / 2) / 2 \times H_{BPF}$
Luminance = V5 – Chrominance — Horizontal Filter

This algorithm determines the amount of Y/C separation according to the result of comparison between the value change V2 to V8 and V4 to V6. Measurement of this data array allows minimization of the problems caused by horizontal and vertical filtering, such as dot-crawl or color smear. Also, it can give a weight to select a filter, vertical or horizontal, according to the K factor set up.

OPERATIONAL DESCRIPTION

A/D Converter

The clamped external composite-video signal is converted to 8-bit binary code by this fast A/D converter. The input video voltage is expected to be 3.0 V p-p nominal. The sampling clock frequency is 14.3 MHz which is four times the color subcarrier signal.

Comb Filter Function

The comb filter consists of a delay-line memory, absolute value function, latches, and 8-bit adders. The basic functions of the filtering are additions and subtractions by the adders. The calculations for each sampled data are expected to be completed within one clock cycle, about 70 ns. Each adder has latches to hold the value calculated. If the speed of the adders is not fast enough, other latches may be inserted into the adders to save the partial value of the calculations. These latches are counted as the digital process delay of the filter. There are two major data passes in this filter: chrominance and luminance. Both data passes are designed such that all delays match when they output.

Vertical Filter

The basic structure of this filter is a 2H line-delay comb filter. The simplified functional block diagram is shown in Figure 3. Two 1H scan delay lines are provided for vertical filtering. Video memory structure can be used for the line delay component. The cycle time of this memory has to be less than 70 ns, and total delay time is 1 scan line time for each.

Horizontal Filter

The other basic function of this filter is called horizontal filtering which has the same function as a bandpass filter. The horizontal filter consists of a 4th order FIR filter which has a bandpass characteristic. Figure 4 shows the simplified functional block diagram of the horizontal filter.

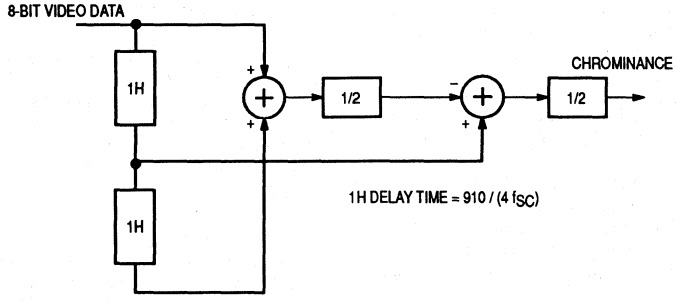


Figure 3. Vertical Filter

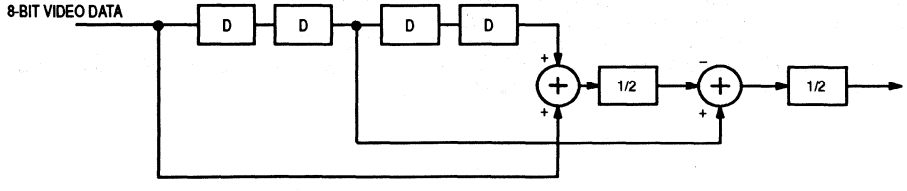


Figure 4. Horizontal Filter

Selective Control

The selective control checks the horizontal transition and vertical transition of the picture in order to select a filtering method that minimizes the dot-crawl, cross color, and color smear. The major filtering algorithm of the chip is performed in this block.

Horizontal transition = |V6 – V4|

Vertical transition = |V8 – V2|

The difference of the transition = |V8 – V2| – |V6 – V4| + K

If |V8 – V2| – |V6 – V4| + K > 0 then Horizontal Filter

If |V8 – V2| – |V6 – V4| + K ≤ 0 then Vertical Filter

K factor

Selective control switches the filtering modes by the transit difference of horizontal and vertical direction. K factor assignment is shown below. If K1 through K4 are all low, a weighting factor is given to the comb filter side. If all are a high level, it gives a weighting factor of 50% comb and bandpass side. The recommended level is b1 = L, b2 through b4 = H.

b0	b1	b2	b3	b4	b5	b6	b7
L	K1	K2	K3	K4	H	H	L

b0, b5, b6, b7 are fixed.

Bandpass Filter (BPF)

This filter has the same functions as the horizontal filter. The bandpass filter reduces low and high frequency components in the chrominance signal.

Video Input Signal

The recommended video input signal for the comb filter is shown in Figure 5. The nominal video input is 3.0 V p-p.

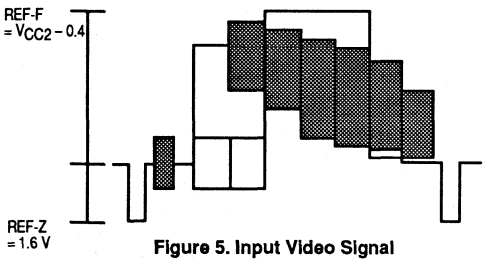


Figure 5. Input Video Signal

USER INFORMATION

VCC, GND

Each of the VCC/GND-pin pairs should be connected to separate power supplies in order to reduce noise problems. All VCC pins should be by passed through 0.1 µF ceramic and 47 µF tantalum capacitors mounted as close as possible to the MC141620.

Vin

The video input signal must be clamped with an appropriate voltage level. It might be necessary to amplify the signal to drive this chip. In order to reduce noise effects, the wiring pattern on the Vin signal should be short as possible. Vin should be driven with a low-impedance source. The frequency bandwidth of the input signal should be limited to less than half of the sampling clock frequency (Nyquist criteria).

AD Reference Inputs

REF-F and REF-Z set the dynamic range of the ADC input. These should be by passed through 0.1 µF ceramic and 10 µF tantalum capacitors mounted close to GND2. The voltage supplied to REF-F and REF-Z must be stable within allowable time and temperature ranges.

Reference accuracy is ±0.5 LSB (voltage difference between REF-F and REF-Z), if all portions of circuit are not changed in compliance with temperature. But, most circuits are changed in compliance with the temperature. Therefore, in this case, the reference voltage accuracy should be less than ±0.5 LSB. A stable power supply is required for these reference inputs and the resistor value of the reference ladder is low (typically about 300 Ω).

Clock Input

Reference Figures 6, 7 and 8.

Clock (14.31818 MHz) must be synchronized with a subcarrier (NTSC) or horizontal sync signal. The clock line should be a short printed circuit board trace, and should be separated from other circuits in order to reduce crosstalk. TTL or CMOS levels may be connected by dc coupling. 5.0 V p-p sine waves may be ac coupled with a 0.1 µF ceramic capacitor.

A small signal, such as a 200 mV p-p or greater sine wave, may be ac coupled with a 0.1 µF ceramic capacitor, then biased to half of VCC1 by a pair of 330 kΩ resistors.

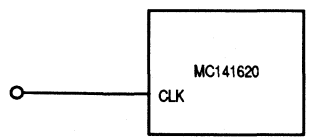


Figure 6. TTL Level

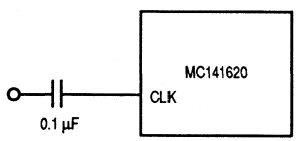


Figure 7. 5.0 V p-p Sine Wave

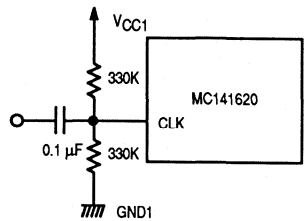


Figure 8. 200 mV p-p to 5.0 V p-p Sine Wave

When the clock level is less than 200 mV p-p, it should be supplied to the circuit of Figure 8 after being increased to more than 200 mV p-p using a buffer amplifier.

I_{BIAS} Pins

The I_{BIAS} pins determine the bias current of the ADC and DAC by external resistors. I_{BIAS1} is associated with the ADC and I_{BIAS2} is for the DAC. In both cases, a 10 kΩ resistor is connected from each of these pins to the closest GND.

DA Reference

This is a bypass pin for the DA reference. Insert a bypass capacitor of about 0.1 μF between DAREF and GND3.

Power-On Sequence

The GND1, GND2, and GND3 pins are connected to a common ground. Power should be supplied sequentially to V_{CC1}, V_{CC2}, then V_{CC3}.

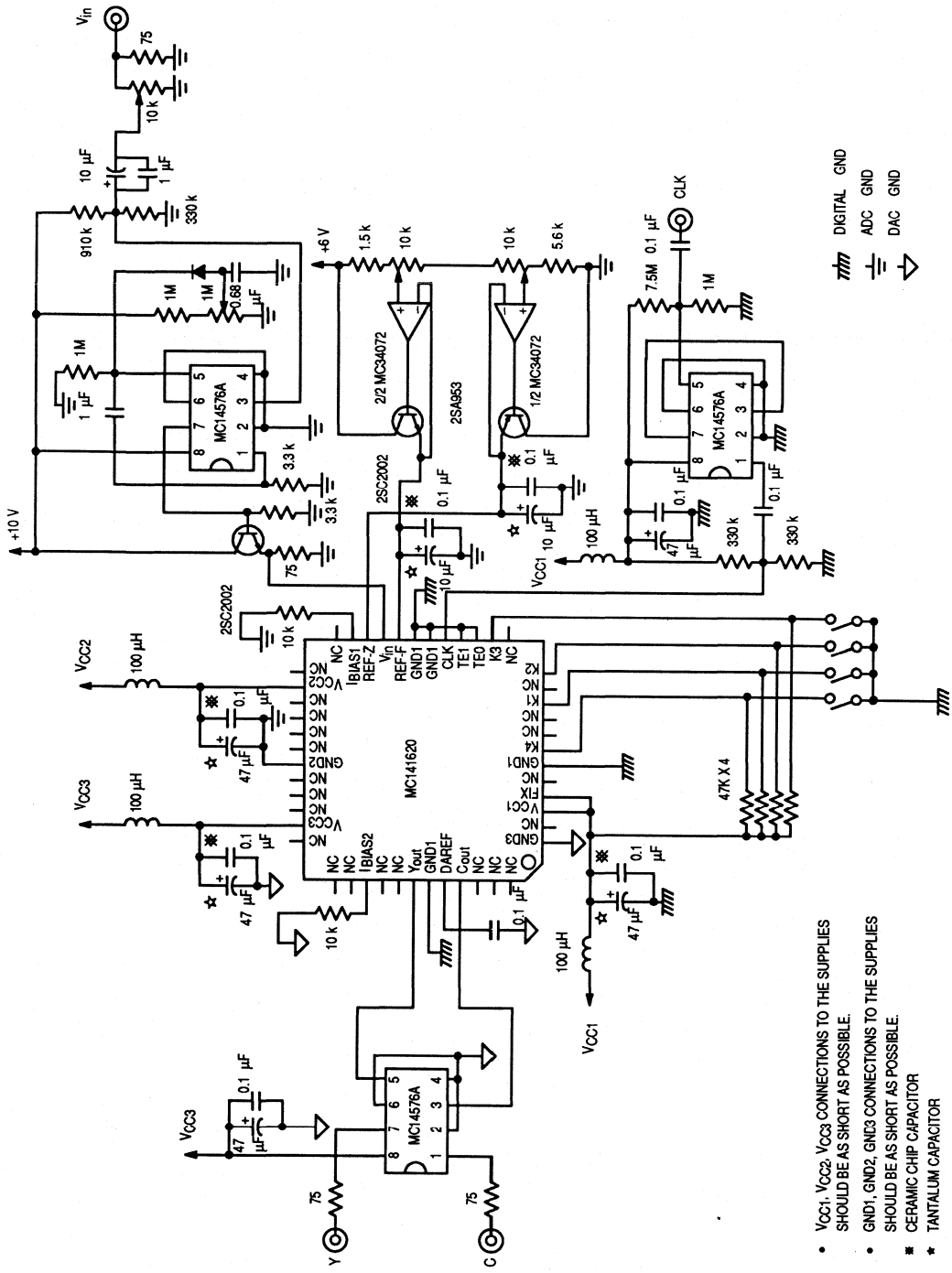


Figure 9. Application Circuit

MOTOROLA INC.
Semiconductor Products Sector

QUALITY POLICY

"It is the policy of the Motorola Semiconductor Products Sector to produce products and provide services exactly according to CUSTOMER expectations, specifications and delivery schedule. Our system is based on prevention using statistical process control. The standard is a Six Sigma level of error-free performance. These results come from the participative efforts of each employee in conjunction with supportive participation from all levels of management."

James A. Norling
Executive Vice President and
General Manager
Semiconductor Products Sector

Thomas D. George
Senior Vice President and
Assistant General Manager
Semiconductor Products Sector

SIX SIGMA
6σ
MOTOROLA

Reliability

The following pages are excerpts from BR518/D, Rev 3, the *Reliability and Quality Handbook—1990 Edition*, Chapter 9, "Standard Logic and Analog Integrated Circuits." For more information, request BR518/D from your Motorola representative.

Standard Logic and Analog Integrated Circuits

INTRODUCTION

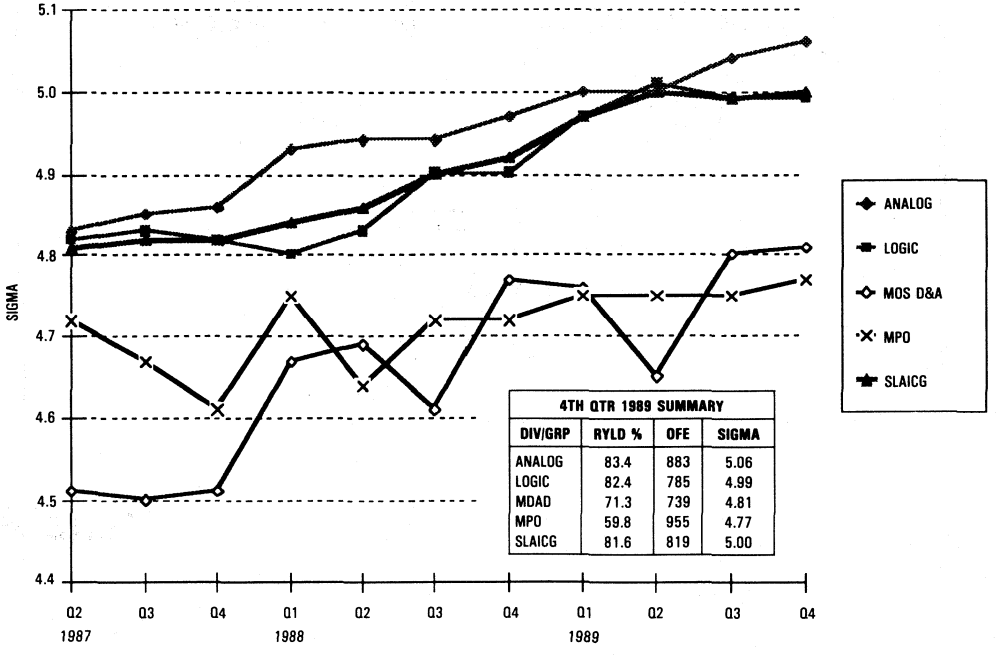
Standard Logic and Analog has an extensive quality and reliability program consisting of:

- New product design review and qualification prior to introduction.
- Quality improvement program consistent with Six Sigma philosophy and utilizing statistical process control and benchmarking.
- Process change qualification and customer notification.
- Development of accelerated testing for real time assessment of quality and reliability.
- Long term reliability audit program to separate infant mortality failure rates and long term failure rates.

The attached data is a summary from the various reports generated in the various assembly sites and business centers of the world. For more detailed information, contact the R&QA organization of your nearest business center.

SIGMA PERFORMANCE FOR ALL PRODUCTS

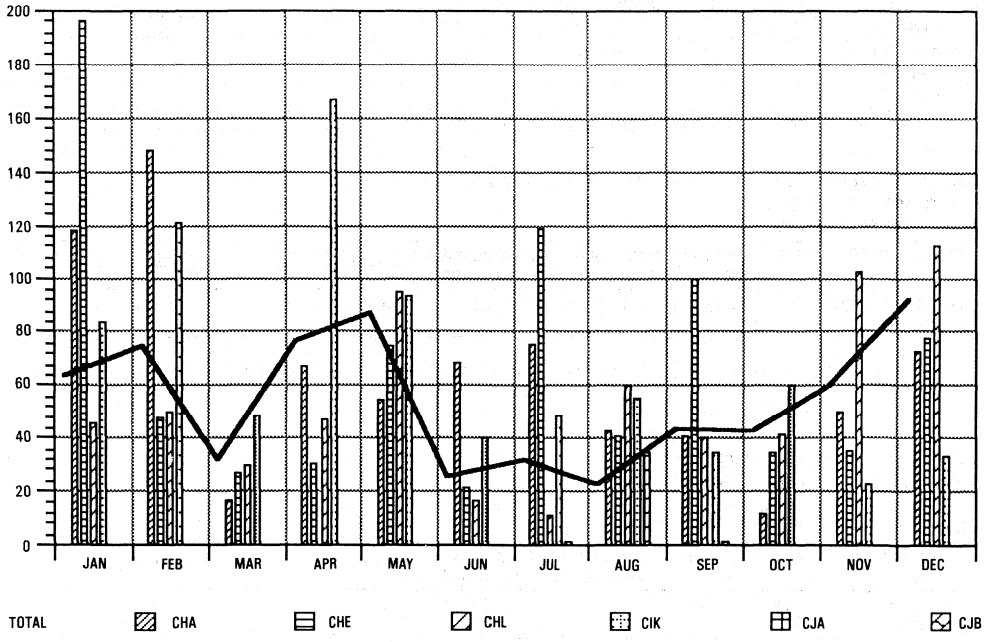
Sigma Performance



4TH QTR 1989 SUMMARY			
DIV/GRP	RYLD %	OFE	SIGMA
ANALOG	83.4	883	5.06
LOGIC	82.4	785	4.99
MDAD	71.3	739	4.81
MPO	59.8	955	4.77
SLAICG	81.6	819	5.00

MOS Digital and Analog Products

U.S. Factory Electrical AOQ—1989



OPERATING LIFE TEST DATA—EARLY LIFE
T_A = 125°C; EA = 0.7 eV; DURATION = 168 HRS
BIAS: FAMILY STANDARD OPERATING VOLTAGE; STATIC CONFIGURATION

PRODUCT FAMILY	# OF LOTS	DEVICES TESTED	CUMULATIVE DEVICE HRS	# OF REJECTS	% FAIL @ 125°C	EQUIV. DEVICE HRS @ 55°C	55°C FIT RATE		COMMENTS
							60% CL	90% CL	
SPECIAL/CUSTOM & TELECOM	171	16,299	2.73×10^6	2	0.012	2.12×10^8	15	25	(1)

NOTE:
1. TWO UNITS FAILED AT 168 HOURS. ONE DUE TO WIRE BOND FRACTURE. TWO DUE TO IONIC CONTAMINATION.

OPERATING LIFE TEST DATA—LONG TERM
T_A = 125°C; EA = 0.7 eV; DURATION: 1008 HRS
BIAS: FAMILY STANDARD OPERATING VOLTAGE; STATIC CONFIGURATION

PRODUCT FAMILY	# OF LOTS	DEVICES TESTED	CUMULATIVE DEVICE HRS	# OF REJECTS	% FAIL @ 125°C	EQUIV. DEVICE HRS @ 55°C	55°C FIT RATE		COMMENTS
							60% CL	90% CL	
SPECIAL/CUSTOM & TELECOM	171	16,278	1.36×10^7	0	0	1.06×10^9	0.87	2.3	

TEMPERATURE HUMIDITY BIAS (THB) TEST DATA
T_A = 85°C; RH = 85%
READOUT 1008 & 2016 HRS
BIAS: FAMILY STANDARD OPERATING VOLTAGE; STATIC BIAS

PRODUCT FAMILY	# OF LOTS	DEVICES TESTED	CUMULATIVE DEVICE HRS	CUMULATIVE FAILURES	% FAIL	COMMENTS
SPECIAL/CUSTOM & TELECOM	56	3,974	8.01×10^7	3	0.075	(1)

NOTE:
1. THREE UNITS FAILED @ 2016 HOURS DUE TO CORRODED BOND PAD.

PRESSURE TEMPERATURE HUMIDITY (PTH OR AUTOCLAVE)
121°C; 100% RH; 15 PSIG
READOUT 96, 240 HRS

PRODUCT FAMILY	# OF LOTS	DEVICES TESTED	CUMULATIVE DEVICE HRS	CUMULATIVE FAILURES	% FAIL	COMMENTS
SPECIAL/CUSTOM & TELECOM	655	21,291	5.10×10^6	13	0.06	(1)

NOTE:
1. THIRTEEN UNITS FAILED @ 240 HOURS DUE TO CORRODED BOND PAD. ONE UNIT FAILED @ 96 HOURS DUE TO OXIDE, GATE DEFECT.

TEMPERATURE CYCLE TEST DATA
CONDITION: −65°C TO +150°C
ENVIRONMENT: AIR TO AIR
READOUT WITH 1000 AND 2000 CYCLES

PRODUCT FAMILY	# OF LOTS	DEVICES TESTED	CUMULATIVE DEVICE CYC	CUMULATIVE FAILURES	% FAIL	COMMENTS
SPECIAL/CUSTOM & TELECOM	128	12,422	2.48×10^7	52	0.42	(1)

NOTE:
1. THREE UNITS FAILED @ 1000 CYCLES DUE TO PASSIVATION CRACKS. ONE UNIT FAILED @ 1000 CYCLES DUE TO BROKEN BOND WIRE. TWELVE UNITS @ 1000 CYCLES AND TWENTY-ONE UNITS @ 2000 CYCLES FAILED DUE TO METAL SMEARING AND PASSIVATION CRACKS, ALL THESE FAILURES WERE CREATED FROM TWO DEVICE TYPES. FIFTEEN UNITS FAILED @ 2000 CYCLES DUE TO PASSIVATION CRACKS.

POWER TEMPERATURE CYCLING
TEMPERATURE = −40°C TO +125°C
LONGEST STRESS = 1000 CYCLES; EACH CYCLE ~ 1 HR
BIAS: 5 VOLTS DYNAMIC, POWER CYCLING RATE = 5 MINUTES (ON)/5 MINUTES OFF

PRODUCT FAMILY	# OF LOTS	DEVICES TESTED	CUMULATIVE DEVICE CYC	CUMULATIVE FAILURES	% FAIL	COMMENTS
SPECIAL/CUSTOM	43	1949	1.95×10^6	2	0.1	(1)

NOTE:
1. TWO UNITS FAILED @ 500 CYCLES DUE TO CORRODED BOND.

CYCLED TEMPERATURE HUMIDITY BIAS (CTHB)
TEMPERATURE: 25°C TO 65°C; HUMIDITY ~90%
LONGEST STRESS = 1008 HRS
BIAS: 5 VOLTS STATIC, POWER CYCLING RATE = 5 MINUTES (ON)/5 MINUTES OFF

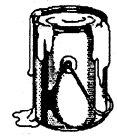
PRODUCT FAMILY	# OF LOTS	DEVICES TESTED	CUMULATIVE DEVICE CYC	CUMULATIVE FAILURES	% FAIL	COMMENTS
SPECIAL/CUSTOM	23	1,275	1.28×10^6	0		

Applications Information

Decoders / Display Drivers
LCD Driver with Serial Interface (MC145453) (AR266) 10-3
PLL Frequency Synthesizers
Phase-Locked Loop Design Fundamentals (AN535) 10-5
The Technique of Direct Programming by Using a Two-Modulus Prescaler (AN 827) 10-16
Operation of the MC145159 PLL Frequency Synthesizer with Analog Phase Detector (AN969) 10-21
VHF Narrowband FM Receiver Using the MC3362 and MC3363 Dual Conversion Receivers (MC145152) (AN980) 10-32
Analyze, Don't Estimate, Phase-Lock-Loop (AR254#1) 10-46
Optimize Phase Lock Loops to Meet Your Needs—Or Determine Why You Can't (AR254#2) . 10-49
Suppress Phase Lock Loop Sidebands without Introducing Instability (AR254#3) 10-53
Programmable Calculator Computes PLL Noise, Stability (AR254#4) 10-56
Remote Control
Operation of the MC14469 (AN806A) 10-65
Infrared Sensing and Data Transmission Fundamentals (AN1016) 10-72
Simplified Remote Control Circuits (MC145030) (AR255) 10-77
Miscellaneous Functions
Use of the MC68HC68T1 RTC with M6805 Microprocessors (ANE425) 10-79

AR266/D

Bit-Bucket



By: All of us

"Contribute Nothing · Expect Nothing", DMW '86

LCD Driver with Serial Interface

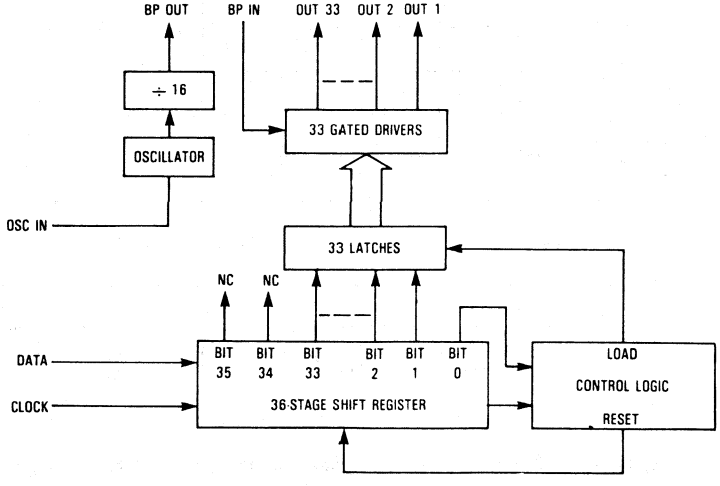
By: David Babin, P.E.
Motorola
MOS Digital-Analog IC Division

The MC145453 directly drives up to 33 non-multiplexed liquid-crystal elements per package. Both small and large displays can be driven by this CMOS IC. (A large 25mm 7-segment display has been successfully driven with the chip.) This flexible device allows external formatting of the display information, thus permitting use with alphanumeric, bar-graph, dot-matrix, or custom LCDs.

The IC's serial port only requires data and clock signals at CMOS or TTL levels. The double-buffered interface is realized with a 36-stage shift register which feeds 33 latches. The shift register is static, allowing data rates down to dc in a continuous or intermittent mode. The latches hold the display information, permitting an undisturbed display during shifting.

The usual data format is a start bit (high), followed by 33 display bits, plus 2 trailing bits (don't cares). If a display bit is high, the associated liquid-crystal element is activated. The start bit causes internal generation of a load signal which transfers the 33 display bits into the latches. After the load signal, an internal reset clears the shift register to ready the device for the next set of data.

Figure 1. Block Diagram



Reprinted with permission, from the December 1987 issue of '68' Micro Journal.

Alternately, a 5-byte (40-bit) transfer can be used as is encountered with SPI. As shown in Figure 2, 4 preamble bits (lows) precede the start bit (high). The start bit is followed by the 33 display bits plus 2 trailing bits. If desired, the bit stream can be formatted as in Figure 3 where the extra 4 bits (lows) follow the 2 trailing bits (don't cares).

Figure 2. 5-Byte Format

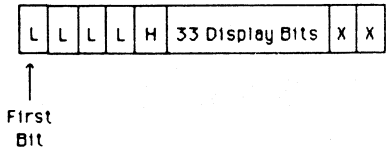
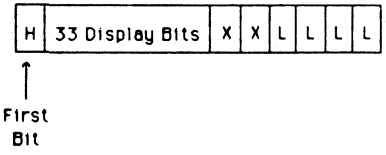


Figure 3. 5-Byte Format



The MC145453 must be initialized after power up. To initialize the IC, purge the shift register by clocking in at least 36 lows. The unit is then synchronized to the processor.

LCD elements respond to the differential RMS voltage between their frontplanes and backplanes. The non-muxed (direct-drive) system offers a much higher voltage contrast ratio ($V_{RMS\text{-}ON}$ / $V_{RMS\text{-}OFF}$) than muxed types. The MC145453 has an excellent voltage contrast ratio of 9. (A muxed-by-2 driver drops this ratio to 2.24.) A high ratio maintains optimum display contrast while allowing the LCD threshold voltage (Figure 4) to have a loose tolerance. This threshold not only varies from LCD to LCD (batch to batch), but a particular LCD's threshold varies over temperature. Utilizing the MC145453, a wide operating temperature range is achieved without using temperature-compensating reference voltages, heaters for the LCD, or high-speed liquid crystals.

To relieve MPU/MCU overhead, an on-chip oscillator supports an external RC which generates the backplane and frontplane drive waveforms. Values of 1MΩ and 470pF produce a 60 to 150 Hz backplane frequency. The capacitor value can be increased up to 1200pF to reduce this frequency.

The MC145453's electrical characteristics are guaranteed over a supply voltage range of 3 to 10V and an ambient temperature range of -40° to 85°C. The operating supply current is only 40μA with all outputs open.

Two packages are presently available: a 40-pin DIP and a space-saving 44-lead PLCC (plastic leaded chip carrier).

To obtain a data sheet call 800/521-6274.

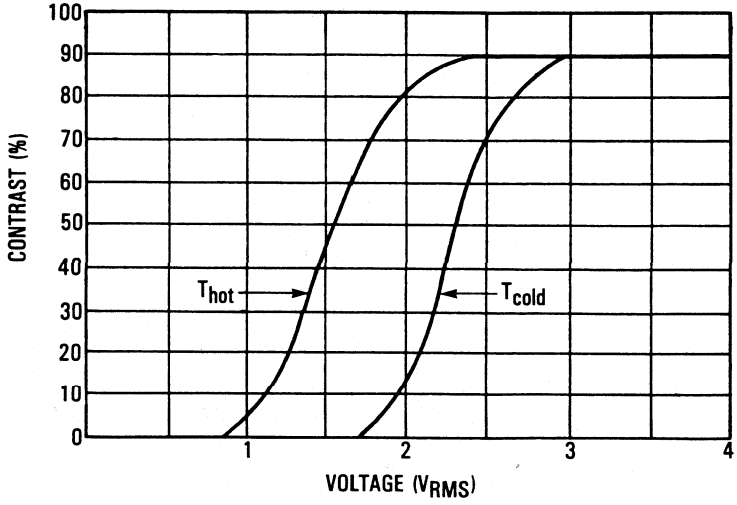


Figure 4. Temperature Effects on Contrast vs Voltage

AN-535
Application Note

PHASE-LOCKED LOOP DESIGN FUNDAMENTALS

INTRODUCTION

The purpose of this application note is to provide the electronic system designer with the necessary tools to design and evaluate Phase Locked Loops (PLL) configured with integrated circuits. The majority of all PLL design problems can be approached using the Laplace transform technique. Therefore, a brief review of Laplace is included to establish a common reference with the reader. Since the scope of this article is practical in nature all theoretical derivations have been omitted hoping to simplify and clarify the content. A bibliography is included for those who desire to pursue the theoretical aspect.

PARAMETER DEFINITION

The Laplace Transform permits the representation of the time response f(t) of a system in the complex domain F(s). This response is twofold in nature in that it contains both the transient and steady state solutions. Thus, all operating conditions are considered and evaluated. The Laplace transform is valid only for positive real time linear parameters; thus, its use must be justified for the PLL which includes both linear and nonlinear functions. This justification is presented in Chapter Three of Phase Lock Techniques by Gardner.[1]

The parameters in Figure 1 are defined and will be used throughout the text.

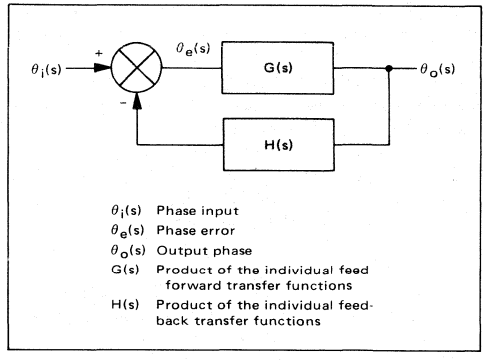


FIGURE 1 – Feedback System

Using servo theory, the following relationships can be obtained.[2]

$$\theta_e(s) = \frac{1}{1 + G(s)\,H(s)}\ \theta_i(s) \qquad (1)$$

$$\theta_o(s) = \frac{G(s)}{1 + G(s)\,H(s)}\ \theta_i(s) \qquad (2)$$

These parameters relate to the functions of a PLL as shown in Figure 2.

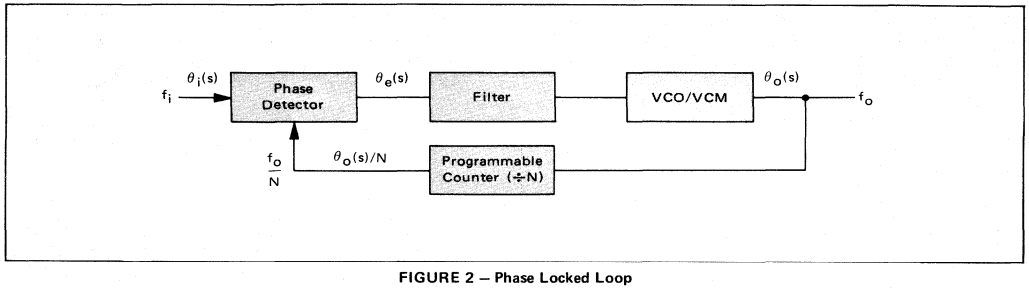


FIGURE 2 – Phase Locked Loop

The phase detector produces a voltage proportional to the phase difference between the signals θ_i and θ_o/N. This voltage upon filtering is used as the control signal for the VCO/VCM (VCM - Voltage Controlled Multivibrator).

Since the VCO/VCM produces a frequency proportional to its input voltage, any time variant signal appearing on the control signal will frequency modulate the VCO/VCM. The output frequency is

$$f_o = N f_i \tag{3}$$

during phase lock. The phase detector, filter, and VCO/VCM compose the feed forward path with the feedback path containing the programmable divider. Removal of the programmable counter produces unity gain in the feedback path (N = 1). As a result, the output frequency is then equal to that of the input.

Various types and orders of loops can be constructed depending upon the configuration of the overall loop transfer function. Identification and examples of these loops are contained in the following two sections.

TYPE – ORDER

These two terms are used somewhat indiscriminately in published literature, and to date there has not been an established standard. However, the most common usage will be identified and used in this article.

The type of a system refers to the number of poles of the loop transfer function G(s) H(s) located at the origin. Example:

$$\text{let} \quad G(s)\,H(s) = \frac{10}{s(s+10)} \tag{4}$$

This is a type one system since there is only one pole at the origin.

The order of a system refers to the highest degree of the polynomial expression

$$1 + G(s)\,H(s) = 0 \triangleq \text{C.E.} \tag{5}$$

which is termed the Characteristic Equation (C.E.). The roots of the characteristic equation become the closed loop poles of the overall transfer function.
Example:

$$G(s)\,H(s) = \frac{10}{s(s+10)} \tag{6}$$

then

$$1 + G(s)\,H(s) = 1 + \frac{10}{s(s+10)} = 0 \tag{7}$$

therefore

$$\text{C.E.} = s(s+10) + 10 \tag{8}$$

$$\text{C.E.} = s^2 + 10s + 10 \tag{9}$$

which is a second order polynomial. Thus, for the given G(s) H(s), we obtain a type 1 second order system.

ERROR CONSTANTS

Various inputs can be applied to a system. Typically these include step position, velocity, and acceleration. The response of type 1, 2, and 3 systems will be examined with the various inputs.

$\theta_e(s)$ represents the phase error that exists in the phase detector between the incoming reference signal $\theta_i(s)$ and the feedback $\theta_o(s)/N$. In evaluating a system, $\theta_e(s)$ must be examined in order to determine if the steady state and transient characteristics are optimum and/or satisfactory. The transient response is a function of loop stability and is covered in the next section. The steady state evaluation can be simplified with the use of the final value theorem associated with Laplace. This theorem permits finding the steady state system error $\theta_e(s)$ resulting from the input $\theta_i(s)$ without transforming back to the time domain.[3]

Simply stated

$$\lim_{t \to \infty} [\theta(t)] = \lim_{s \to o} [s\,\theta_e(s)] \tag{10}$$

Where

$$\theta_e(s) = \frac{1}{1 + G(s)\,H(s)}\ \theta_i(s) \tag{11}$$

The input signal $\theta_i(s)$ is characterized as follows:

$$\text{Step position:} \quad \theta_i(t) = C_p \quad t \geqslant 0 \tag{12}$$

$$\text{Or, in Laplace notation:} \quad \theta_i(s) = \frac{C_p}{s} \tag{13}$$

where C_p is the magnitude of the phase step in radians. This corresponds to shifting the phase of the incoming reference signal by C_p radians:

$$\text{Step velocity:} \quad \theta_i(t) = C_v t \quad t \geqslant 0 \tag{14}$$

$$\text{Or, in Laplace notation:} \quad \theta_i(s) = \frac{C_v}{s^2} \tag{15}$$

where C_v is the magnitude of the rate of change of phase in radians per second. This corresponds to inputing a frequency that is different than the feedback portion of the VCO frequency. Thus, C_v is the frequency difference in radians per second seen at the phase detector.

$$\text{Step acceleration:} \quad \theta_i(t) = C_a t^2 \quad t \geqslant 0 \tag{16}$$

$$\text{Or, in Laplace notation:} \quad \theta_i(s) = \frac{2\,C_a}{s^3} \tag{17}$$

C_a is the magnitude of the frequency rate of change in radians per second per second. This is characterized by a time variant frequency input.

Typical loop G(s) H(s) transfer functions for types 1, 2, and 3 are:

$$\text{Type 1} \quad G(s)\,H(s) = \frac{K}{s(s+a)} \tag{18}$$

$$\text{Type 2}\quad G(s)\,H(s) = \frac{K(s+a)}{s^2} \tag{19}$$

$$\text{Type 3}\quad G(s)\,H(s) = \frac{K(s+a)(s+b)}{s^3} \tag{20}$$

The final value of the phase error for a type 1 system with a step phase input is found by using Equations 11 and 13.

$$\theta_e(s) = \left(\frac{1}{1+\frac{K}{s(s+a)}}\right)\left(\frac{C_p}{s}\right)$$

$$= \frac{(s+a)C_p}{(s^2+as+K)} \tag{21}$$

$$\theta_e(t=\infty) = \lim_{s\to o}\left[s\left(\frac{s+a}{s^2+as+K}\right)C_p\right] = 0 \tag{22}$$

Thus the final value of the phase error is zero when a step position (phase) is applied.

Similarly applying the three inputs into type 1, 2 and 3 systems and utilizing the final value theorem, the following table can be constructed showing the respective steady state phase errors.

TABLE I — Steady State Phase Errors for Various System Types

	Type 1	Type 2	Type 3
Step Position	Zero	Zero	Zero
Step Velocity	Constant	Zero	Zero
Step Acceleration	Continually Increasing	Constant	Zero

A zero phase error identifies phase coherence between the two input signals at the phase detector.

A constant phase error identifies a phase differential between the two input signals at the phase detector. The magnitude of this differential phase error is proportional to the loop gain and the magnitude of the input step.

A continually increasing phase error identifies a time rate change of phase. This is an unlocked condition for the phase loop.

Using Table I the system type can be determined for specific inputs. For instance, if it is desired for a PLL to track a reference frequency (step velocity) with zero phase error, a minimum of type 2 is required.

STABILITY

The root locus technique of determining the position of system poles and zeroes in the s-plane is often used to graphically visualize the system stability. The graph or plot illustrates how the closed loop poles (roots of the characteristic equation) vary with loop gain. For stability all poles must lie in the left half of the s-plane. The relationship of the system poles and zeroes then determine the degree of stability. The root locus contour can be determined by using the following guidelines.[2]

Rule 1 - The root locus begins at the poles of G(s) H(s) (K = 0) and ends at the zeroes of G(s) H(s) (K = ∞). Where K is loop gain.

Rule 2 - The number of root loci branches is equal to the number of poles or number of zeroes, whichever is greater. The number of zeroes at infinity is the difference between the number of finite poles and finite zeroes of G(s) H(s).

Rule 3 - The root locus contour is bounded by asymptotes whose angular position is given by

$$\frac{(2n+1)}{\#P - \#Z}\pi;\ n = 0, 1, 2, \ldots \tag{23}$$

Where #P (#Z) is the number of poles (zeroes).

Rule 4 - The intersection of the asymptotes is positioned at the center of gravity C. G.

$$C.G. = \frac{\Sigma P - \Sigma Z}{\#P - \#Z} \tag{24}$$

Where ΣP (ΣZ) denotes the summation of the poles (zeroes).

Rule 5 - On a given section of the real axis, root loci may be found in the section only if the #P + #Z to the right is odd.

Rule 6 - Breakaway points from negative real axis is given by:

$$\frac{dK}{ds} = 0 \tag{25}$$

Again where K is the loop gain variable factored from the characteristic equation.

Example:

The root locus for a typical loop transfer function is found as follows:

$$G(s)\,H(s) = \frac{K}{s(s+4)} \tag{26}$$

The root locus has two branches (Rule 2) which begin at s = 0 and s = −4 and ends at the two zeroes located at infinity (Rule 1). The asymptotes can be found according to Rule 3. Since there are two poles and no zeroes the equation becomes:

$$\frac{2n+1}{2}\pi = \begin{cases} \frac{\pi}{2}, & \text{for } n = 0 \\ \frac{3\pi}{2}, & \text{for } n = 1 \end{cases} \tag{27}$$

The position of the intersection according to the Rule 4 is:

$$s = \frac{\Sigma P - \Sigma Z}{\#P - \#Z} = \frac{(-4-0)-(0)}{2-0}$$

$$s = -2 \qquad (28)$$

The breakaway point as defined by Rule 6 can be found by first writing the characteristic equation.

$$C.E. = 1 + G(s)\,H(s) = 0$$

$$= 1 + \frac{K}{s(s+4)} = s^2 + 4s + K = 0 \qquad (29)$$

Now solving for K yields

$$K = -s^2 - 4s \qquad (30)$$

Taking the derivative with respect to s and setting it equal to zero then determines the breakaway point.

$$\frac{dK}{ds} = \frac{d}{ds}(-s^2 - 4s) \qquad (31)$$

$$\frac{dK}{ds} = -2s - 4 = 0 \qquad (32)$$

or

$$s = -2 \qquad (33)$$

is the point of departure. Using this information, the root locus can be plotted as in Figure 3.

This second order characteristic equation given by Equation 29 has been normalized to a standard form[2]

$$s^2 + 2\zeta\omega_n s + \omega^2_n \qquad (34)$$

where the damping ratio $\zeta = \text{Cos}\,\phi$ $(0^o \leqslant \phi \leqslant 90^o)$ and ω_n is the natural frequency as shown in Figure 3.

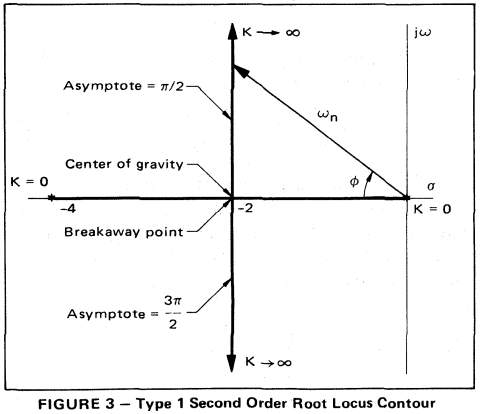


FIGURE 3 – Type 1 Second Order Root Locus Contour

The response of this type 1, second order system to a step input is shown in Figure 4. These curves represent the phase response to a step position (phase) input for various damping ratios. The output frequency response as a function of time to a step velocity (frequency) input is also characterized by the same set of figures.

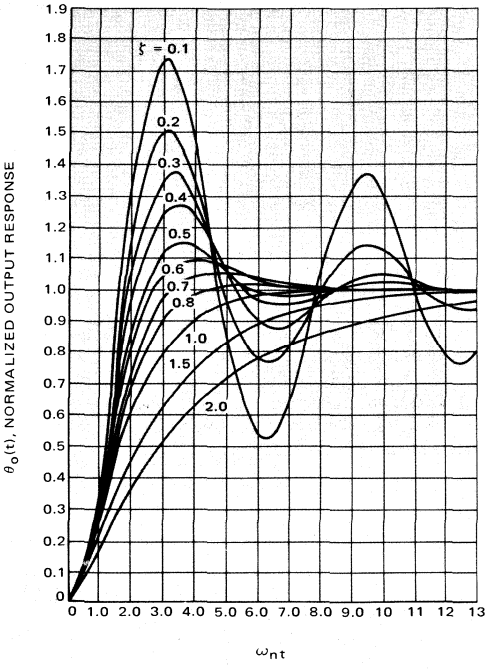


FIGURE 4 – Type 1 Second Order Step Response

The overshoot and stability as a function of the damping ratio ζ is illustrated by the various plots. Each response is plotted as a function of the normalized time $\omega_n t$. For a given ζ and a lock-up time t, the ω_n required to achieve the desired results can be determined. Example:

Assume $\zeta = 0.5$
error $< 10\%$
for $t > 1$ ms

From $\zeta = 0.5$ curve the error is less than 10% of final value for all time greater than $\omega_n t = 4.5$. The required ω_n can then be found by:

$$\omega_n t = 4.5 \qquad (35)$$

or

$$\omega_n = \frac{4.5}{t} = \frac{4.5}{0.001} = 4.5 \text{ k rad/s} \qquad (36)$$

ζ is typically selected between 0.5 and 1 to yield optimum overshoot and noise performance.
Example:

Another common loop transfer function takes the form

$$G(s)\,H(s) = \frac{(s + a)k}{s^2} \qquad (37)$$

This is a type 2 second order system. A zero is added to provide stability. (Without the zero the poles would move along the $j\omega$ axis as a function of gain and the system would at all times be oscillatory in nature.) The root locus shown in Figure 5 has two branches beginning at the origin with one asymptote located at 180 degrees. The center of gravity is s = a; however, with only one asymptote there is no intersection at this point. The root locus lies on a circle centered at s = -a and continues on all portions of the negative real axis to left of the zero. The breakaway point is s = -2a.

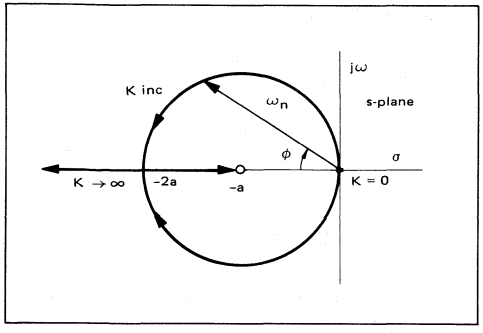


FIGURE 5 – Type 2 Second Order Root Locus Contour

The respective phase or output frequency response of this type 2 second order system to a step position (phase) or velocity (frequency) input is shown in Figure 6. As illustrated in the previous example the required ω_n can be determined by the use of the graph when ζ and the lock up time are given.

BANDWIDTH

The -3 dB bandwidth of the PLL is given by

$$\omega_{-3\ dB} = \omega_n\left(1 - 2\zeta^2 + \sqrt{2 - 4\zeta^2 + 4\zeta^4}\right)^{1/2} \qquad (38)$$

for a type 1 second order[4] system, and by

$$\omega_{-3\ dB} = \omega_n\left(1 + 2\zeta^2 + \sqrt{2 + 4\zeta^2 + 4\zeta^4}\right)^{1/2} \qquad (39)$$

for a type 2 second order[1] system.

PHASE-LOCKED LOOP DESIGN EXAMPLE

The design of a PLL typically involves determining the type of loop required, selecting the proper bandwidth, and establishing the desired stability. A fundamental approach

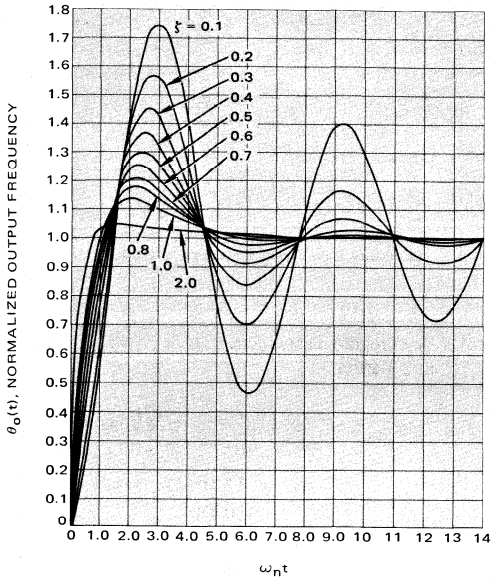


FIGURE 6 – Type 2 Second Order Step Response

to these design constraints is now illustrated. It is desired for the system to have the following specifications:

Output frequency	2.0 MHz to 3.0 MHz
Frequency steps	100 kHz
Phase coherent frequency output	–
Lock-up time between channels	1 ms
Overshoot	< 20%

NOTE: These specifications characterize a system function similar to a variable time base generator or a frequency synthesizer.

From the given specifications the circuit parameters shown in Figure 7 can now be determined.
The devices used to configure the PLL are:

Frequency-Phase Detector	MC4044/4344
Voltage Controlled Multivibrator (VCM)	MC4024/4324
Programmable Counter	MC4016/4316

The forward and feedback transfer functions are given by:

$$G(s) = K_p K_f K_o \qquad H(s) = K_n \qquad (40)$$

where $K_n = 1/N$ (41)

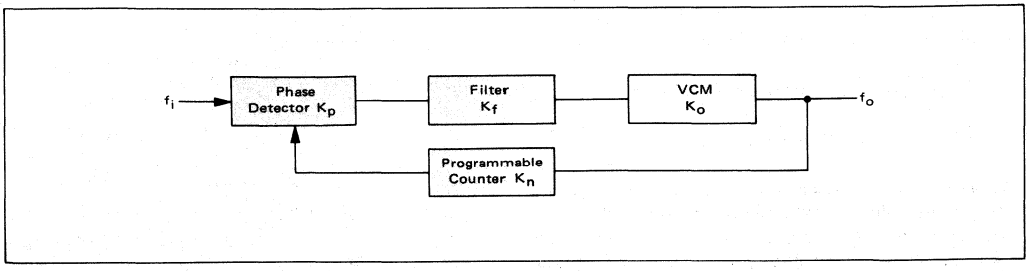


FIGURE 7 – Phase Locked Loop Circuit Parameters

The programmable counter divide ratio K_n can be found from Equation 3.

$$N_{min} = \frac{f_{o\,min}}{f_i} = \frac{f_{o\,min}}{f_{step}} = \frac{2\text{ MHz}}{100\text{ kHz}} = 20 \qquad (42)$$

$$N_{max} = \frac{f_{o\,max}}{f_{step}} = \frac{3\text{ MHz}}{100\text{ kHz}} = 30 \qquad (43)$$

$$K_n = \frac{1}{20} \text{ to } \frac{1}{30} \qquad (44)$$

A type 2 system is required to produce a phase coherent output relative to the input (see Table I). The root locus contour is shown in Figure 5 and the system step response is illustrated by Figure 6.

The operating range of the MC4024/4324 VCM must cover 2 MHz to 3 MHz. Selecting the VCM control capacitor according to the rules contained on the data sheet yields C = 100 pF. The desired operating range is then centered within the total range of the device. The input voltage versus output frequency is shown in Figure 8.

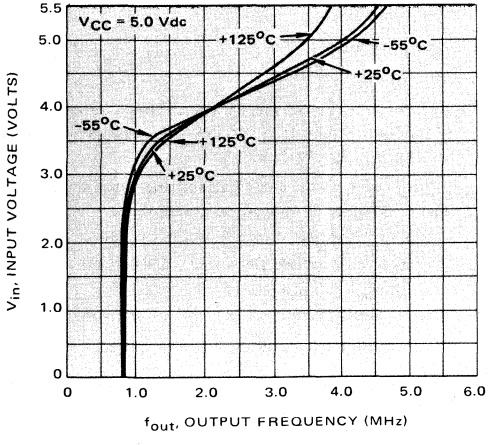


FIGURE 8 – MC4324 Input Voltage versus Output Frequency (100 pF Feedback Capacitor)

The transfer function of the VCM is given by

$$K_O = \frac{K_V}{s} \qquad (45)$$

Where K_V is the sensitivity in radians per second per volt. From the curve in Figure 8, K_V is found by taking the reciprocal of the slope.

$$K_V = \frac{4\text{ MHz} - 1.5\text{ MHz}}{5\text{ V} - 3.6\text{ V}}\ 2\pi \text{ rad/s/V}$$

$$K_V = 11.2 \text{ X } 10^6 \text{ rad/s/V} \qquad (46)$$

Thus

$$K_O = \frac{11.2 \text{ X } 10^6}{s} \text{ rad/s/V} \qquad (47)$$

The s in the denominator converts the frequency characteristics of the VCM to phase, i.e., phase is the integral of frequency.

The gain constant for the MC4044/4344 phase detector is found by [5]

$$K_p = \frac{\text{DF High - UF Low}}{2(2\pi)} = \frac{2.3\text{ V} - 0.9\text{ V}}{4\pi} = 0.111\text{ V/rad} \qquad (48)$$

Since a type 2 system is required (phase coherent output) the loop transfer function must take the form of Equation 19. The parameters thus far determined include K_p, K_O, K_n leaving only K_f as the variable for design. Writing the loop transfer function and relating it to Equation 19

$$G(s)\,H(s) = \frac{K_p\,K_V\,K_n\,K_f}{s} = \frac{K(s+a)}{s^2} \qquad (49)$$

Thus K_f must take the form

$$K_f = \frac{s+a}{s} \qquad (50)$$

in order to provide all the necessary poles and zeroes for

the required G(s) H(s). The circuit shown in Figure 9 yields the desired results.

K_f is expressed by

$$K_f = \frac{R_2Cs + 1}{R_1Cs} \quad \text{for large A} \qquad (51)$$

where A is voltage gain of the amplifier.

R_1, R_2, and C are then the variables used to establish the overall loop characteristics.

The MC4044/4344 provides the active circuitry required to configure the filter K_f. An additional low current high β buffering device or FET can be used to boost the input impedance thus minimizing the leakage current from the capacitor C between sample updates. As a result longer sample periods are achievable.

Since the gain of the active filter circuitry in the MC4044/4344 is not infinite, a gain correction factor K_c must be applied to K_f in order to properly characterize the function. K_c is found experimentally to be $K_c = 0.5$.

$$K_{fc} = K_f K_c = 0.5 \left(\frac{R_2Cs + 1}{R_1Cs}\right) \qquad (52)$$

(For large gain, Equation 51 applies.)

The PLL circuit diagram is shown in Figure 10 and its Laplace representation in Figure 11.

The loop transfer function is

$$G(s)\,H(s) = K_p K_{fc} K_o K_n \qquad (53)$$

$$G(s)\,H(s) = K_p (0.5) \left(\frac{R_2Cs+1}{R_1Cs}\right)\left(\frac{K_v}{s}\right)\left(\frac{1}{N}\right) \qquad (54)$$

The characteristic equation takes the form

$$C.E. = 1 + G(s)\,H(s) = 0$$

$$= s^2 + \frac{0.5 K_p K_v R_2}{R_1 N} s + \frac{0.5 K_p K_v}{R_1 CN} \qquad (55)$$

Relating Equation 55 to the standard form given by Equation 34

$$s^2 + \frac{0.5 K_p K_v R_2}{R_1 N} s + \frac{0.5 K_p K_v}{R_1 CN}$$

$$= s^2 + 2\zeta\omega_n s + \omega_n^2 \qquad (56)$$

Equating like coefficients yields

$$\frac{0.5 K_p K_v}{R_1 CN} = \omega_n^2 \qquad (57)$$

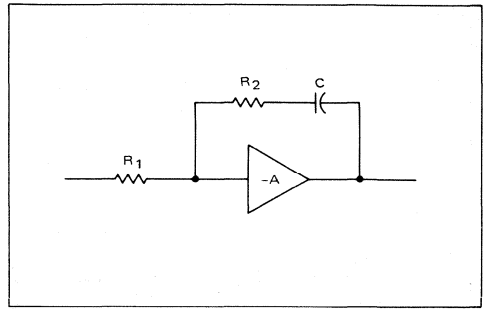


FIGURE 9 – Active Filter Design

and $$\frac{0.5 K_p K_v R_2}{R_1 N} = 2\zeta\omega_n \qquad (58)$$

With the use of an active filter whose open loop gain (A) is large ($K_c = 1$), Equations 57 and 58 become

$$\frac{K_p K_v}{R_1 CN} = \omega_n^2 \qquad (59)$$

$$\frac{K_p K_v R_2}{R_1 N} = 2\zeta\omega_n \qquad (60)$$

The percent overshoot and settling time are now used to determine ω_n. From Figure 6 it is seen that a damping ratio $\zeta = 0.8$ will produce a peak overshoot less than 20% and will settle to within 5% at $\omega_n t = 4.5$. The required lock-up time is 1 ms.

$$\omega_n = \frac{4.5}{t} = \frac{4.5}{0.001} = 4.5 \text{ k rad/s} \qquad (61)$$

Rewriting Equation 57

$$R_1 C = \frac{0.5 K_p K_v}{\omega_n^2 N} \qquad (62)$$

$$= \frac{(0.5)\,(0.111)\,(11.2 \times 10^6)}{(4500)^2\,(30)}$$

$$R_1 C = 0.00102$$

(Maximum overshoot occurs at N_{max} which is minimum loop gain)

Let $C = 0.5\ \mu F$

Then $$R_1 = \frac{0.00102}{0.5 \times 10^{-6}} = 2.04\ k\Omega$$

Use $R_1 = 2\ k\Omega$

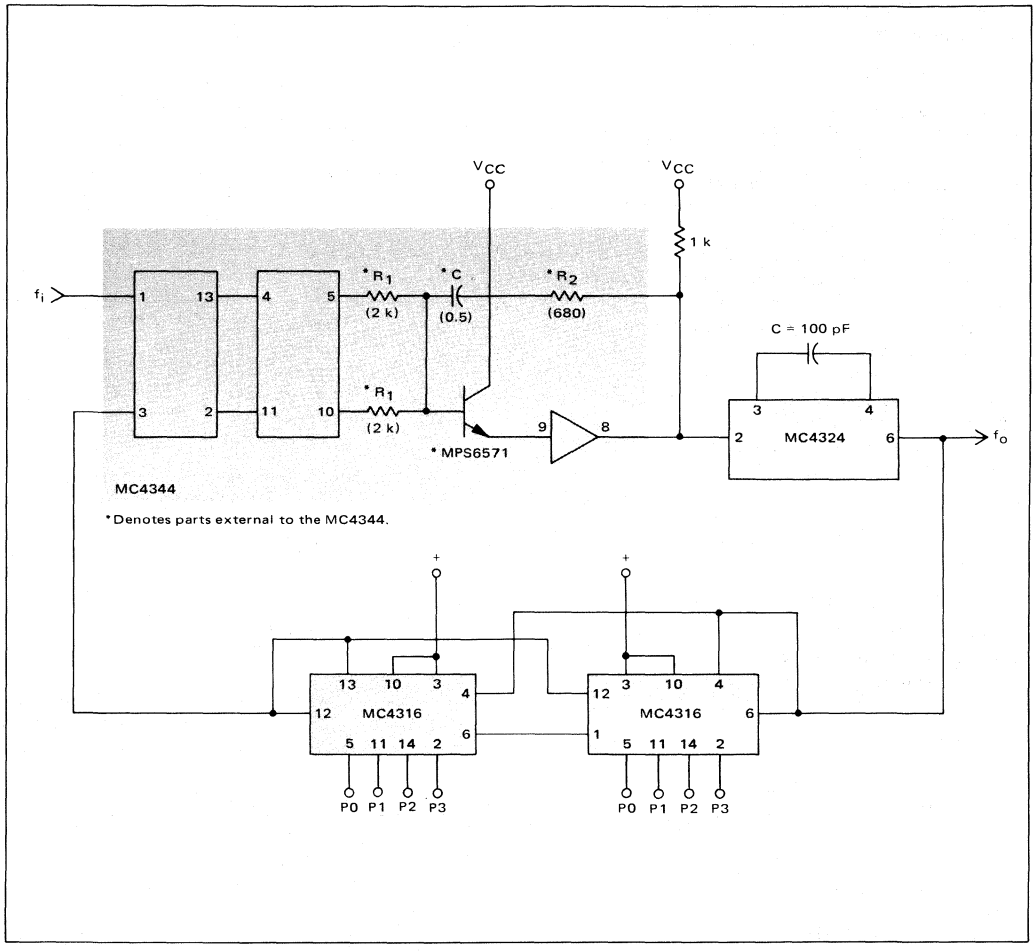


FIGURE 10 – Circuit Diagram of Type 2 Phase Locked Loop

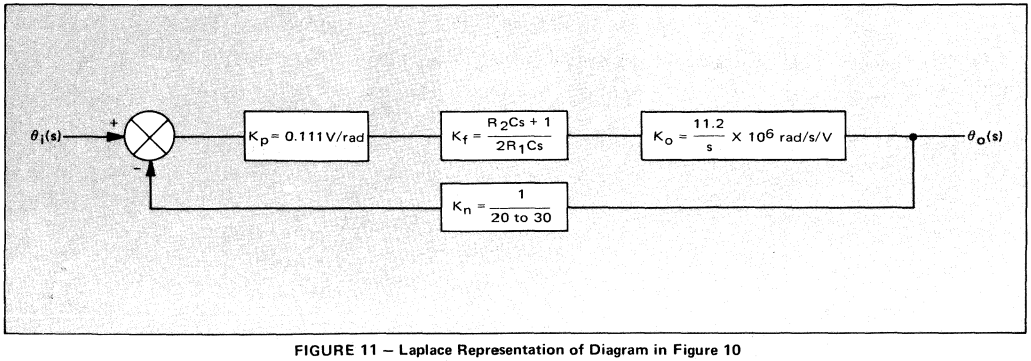


FIGURE 11 – Laplace Representation of Diagram in Figure 10

R_1 is typically selected greater than 1 kΩ.

Solving for R_2 in Equation 58

$$R_2 = \frac{2\zeta\,\omega_n R_1 N}{K_p K_v (0.5)} = \frac{2\zeta}{C\,\omega_n} \qquad (63)$$

$$= \frac{2(0.8)}{(0.5 \times 10^{-6})(4.5\ \text{k})}$$

$$= 711\ \Omega$$

use $R_2 = 680\ \Omega$

All circuit parameters have now been determined and the PLL can be properly configured.

Since the loop gain is a function of the divide ratio K_n, the closed loop poles will vary is position as K_n varies. The root locus shown in Figure 12 illustrates the closed loop pole variation.

The loop was designed for the programmable counter N = 30. The system response for N = 20 exhibits a wider bandwidth and larger damping factor, thus reducing both lock-up time and percent overshoot (see Figure 14).

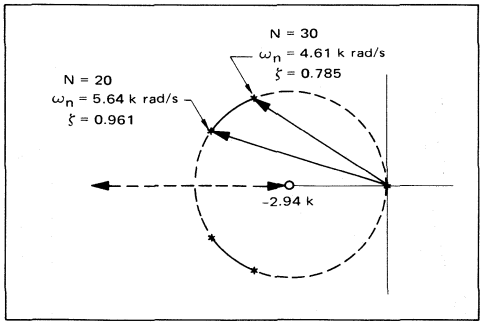


FIGURE 12 – Root Locus Variation

NOTE: The type 2 second order loop was illustrated as a design example because it provides excellent performance for both type 1 and 2 applications. Even in systems that do not require phase coherency a type 2 loop still offers an optimum design.

EXPERIMENTAL RESULTS

Figure 13 shows the theoretical transient frequency response of the previously designed system. The curve N = 30 illustrates the frequency response when the programmable counter is stepped from 29 to 30 thus producing a change in the output frequency from 2.9 MHz to 3.0 MHz. An overshoot of 18% is obtained and the output frequency is within 5 kHz of the final value one millisecond after the applied step. The curve N = 20 illustrates the output frequency change as the programmable counter is stepped from 21 to 20.

Since the output frequency is proportional to the VCM control voltage, the PLL frequency response can be observed with an oscilloscope by monitoring pin 2 of the VCM. The average frequency response as calculated by the Laplace method is found experimentally by smoothing this voltage at pin 2 with a simple RC filter whose time constant is long compared to the phase detector sampling rate but short compared to the PLL response time. With the programmable counter set at 29 the quiescent control voltage at pin 2 is approximately 4.37 volts. Upon changing the counter divide ratio to 30 the control voltage increases to 4.43 volts as shown in Figure 14. A similar transient occurs when stepping the programmable counter from 21 to 20. Figure 14 illustrates that the experimental results obtained from the configured system follows the predicted results shown in Figure 13. Linearity is maintained for phase errors less than 2π, i.e. there is no cycle slippage at the phase detector.

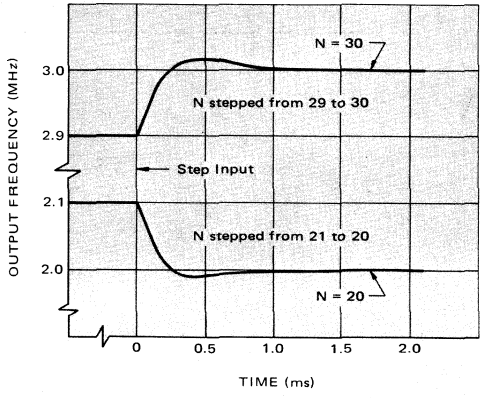


FIGURE 13 – Frequency-Time Response

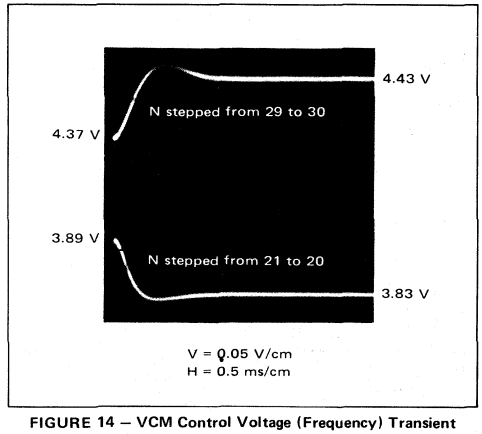


FIGURE 14 – VCM Control Voltage (Frequency) Transient

*THE PARAMETERS LISTED BELOW APPLY TO THE FOLLOWING PLOT

PHASE DETECTOR GAIN CONSTANT	P1 = 0.111 VOLTS PER RADIAN
VCM GAIN CONSTANT	V1 = 1.12 E+7 RAD PER VOLT
FILTER INPUT RESISTOR	R1 = 3900 OHMS ($R1_C$ = 2 k)
FILTER FEEDBACK RESISTOR	R2 = 680 OHMS
FILTER CAPACITOR	C1 = 0.5 MICROFARADS
DIVIDER VALUE	N1-N2 = 29 - 30
REFERENCE FREQUENCY	F1 = 100000 CPS
OUTPUT FREQUENCY CHANGE	F5 = 100000 CPS

P2 = 0.111	C2 = 0.5
V2 = 1.12 E+7	N3 - N4 = 21 - 20
R3 = 3900 ($R1_C$ = 2 k)	F2 (F6) = 100000 (100000)
R4 = 680	

PLOT OF FUNCTIONS

(NOTE: Y(T) IS PLOTTED '+', Z(T) IS '*', AND '0' IS COMMON)

FOR T: TOP = 0 BOTTOM = 0.0015 INCREMENT = 0.00005
FOR FCTS: LEFT = 0 RIGHT = 0.12 INCREMENT = 0.002

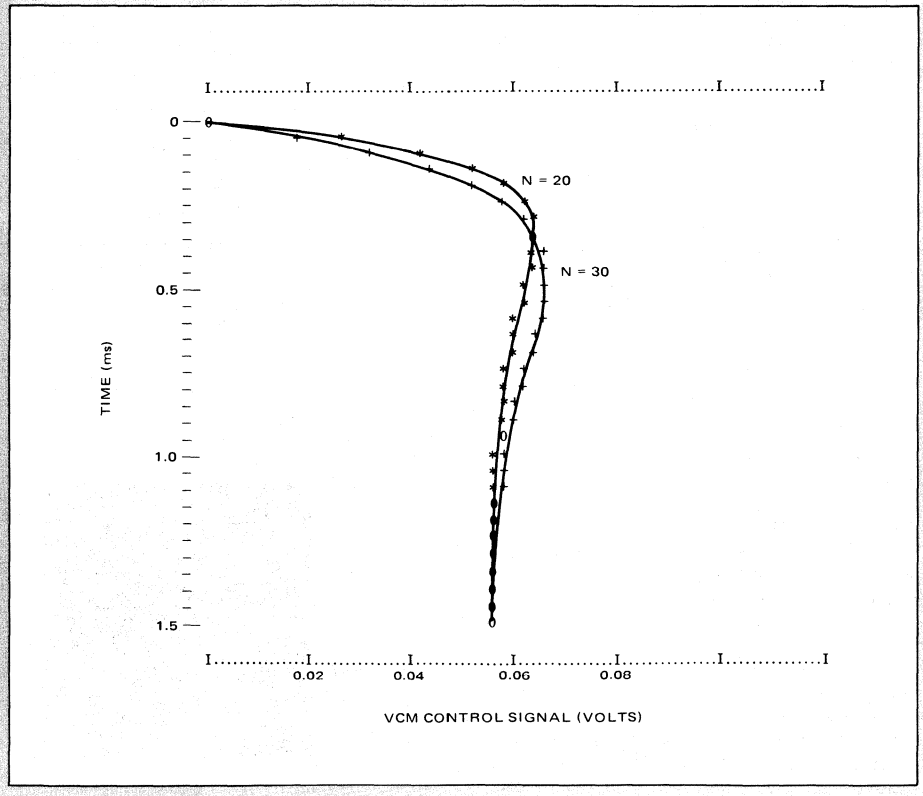


FIGURE 15 – VCM Control Signal Transient

Figure 15 is a theoretical plot of the VCM control voltage transient as calculated by a computer program. The computer program is written with the parameters of Equations 58 and 59 (type 2) as the input variables and is valid for all damping ratios of $\zeta \leq 1.0$. The program prints or plots the control voltage transient versus time for desired settings of the programmable counter. The lock-up time can then be readily determined as the various parameters are varied. (If stepping from a higher divide ratio to a lower one the transient will be negative.) Figures 14 and 15 also exhibit a close correlation between the experimental and analytical results.

SUMMARY

This application note describes the basic control system techniques required for phase-locked loop design. Criteria for the selection of the optimum type of loop and methods for establishing the desired performance characteristics are presented. A design example is illustrated in a step-by-step approach along with the comparison of the experimental and analytical results.

BIBLIOGRAPHY

1. Topic: Type Two System Analysis
Gardner, F. M., Phase Lock Techniques, Wiley, New York, Second Edition, 1967
2. Topic: Root Locus Techniques
Kuo, B. C., Automatic Control Systems, Prentice-Hall, Inc., New Jersey, 1962
3. Topic: Laplace Techniques
McCollum, P. and Brown, B., Laplace Transform Tables and Theorems, Holt, New York, 1965
4. Topic: Type One System Analysis
Truxal, J.G., Automatic Feedback Control System Synthesis, McGraw-Hill, New York, 1955
5. Topic: Phase Detector Gain Constant
DeLaune, Jon, MTTL and MECL Avionics Digital Frequency Synthesizer, AN532

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

AN-827
Application Note

THE TECHNIQUE OF DIRECT PROGRAMMING BY USING A TWO-MODULUS PRESCALER

Prepared by
PLL Applications

INTRODUCTION

The MC12009, MC12011, or MC12013 can be used as part of a variable modulus (divisor) prescaling subsystem used in certain Digital Phase-Locked Loops (PLL).

More often than not, the feedback loop of any PLL contains a counter-divider. Many methods are available for building a divider, but not all are simple, economical, or convenient in a particular application.

The technique and system described here offer a new approach to the construction of a phase-locked loop divider. In addition to using either the MC12009, MC12011, or the MC12013 variable modulus prescaler, this system requires an MC12014 Counter Control Logic Function, together with suitable programmable counters (e.g., MC4016s or SN74LS716s). Data sheets for these additional devices should be consulted for their particular functional descriptions.

DESIGN CONSIDERATIONS

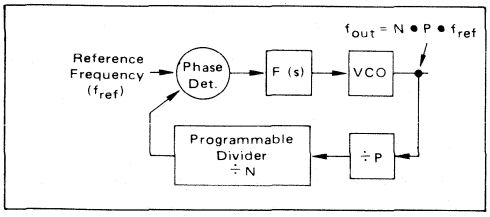
The disadvantage of using a fixed modulus (÷ P) for frequency division in high-frequency phase-locked loops (PLL) is that it requires dividing the desired reference frequency by P also (desired reference frequency equals channel spacing).

The MC12009/11/13 are especially designed for use with a technique called "variable modulus prescaling". This technique allows a simple MECL two-modulus prescaler to be controlled by a relatively slow MTTL programmer counter. The use of this technique permits direct high-frequency prescaling without any sacrifice in resolution since it is no longer necessary to divide the reference frequency by the modulus of the high-frequency prescaler.

The theory of "variable modulus prescaling" may be explained by considering the system shown in Figure 1. For the loop shown:

$$f_{out} = N \bullet P \bullet f_{ref} \quad (1)$$

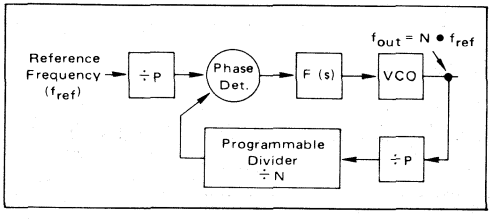
FIGURE 1 – FREQUENCY SYNTHESIS BY PRESCALING



where P is fixed and N is variable. For a change of 1 in N, the output frequency changes by $P \bullet f_{ref}$. If f_{ref} equals the desired channel spacing, then only every P channel may be programmed using this method. A problem remains: how to program intermediate channels.

One solution to this problem is shown in Figure 2.

FIGURE 2 – FREQUENCY SYNTHESIS BY PRESCALING



A ÷ P is placed in series with the desired channel spacing (frequency) to give a new reference frequency: channel spacing/P.

Another solution is found by considering the defining equation (1) for f_{out} of Figure 1. From the equation it may be seen that only every P channel can be programmed simply, because N is always an integer. To obtain intermediate channels, P must be multiplied by an integer plus a fraction. This fraction would be of the form: A/P. If N is defined to be an integer number, N_P, plus a fraction, A/P, N may be expressed as:

$$N = N_P + A/P.$$

Substituting this expression for N in equation 1 gives:

$$f_{out} = (N_P + A/P) \bullet P \bullet f_{ref} \quad (2)$$

or:

$$f_{out} = (N_P P + A) \bullet f_{ref} \quad (3)$$

$$f_{out} = N_P \bullet P \bullet f_{ref} + A \bullet f_{ref}. \quad (4)$$

Equation 4 shows that all channels can be obtained directly if N can take on fractional values. Since it is difficult to multiply by a fractional number, equation 4 must be synthesized by some other means.

Taking equation 3 and adding ±AP to the coefficient of f_{ref}, the equation becomes:

$$f_{out} = (N_P \bullet P + A + A \bullet P - A \bullet P) f_{ref}. \quad (5)$$

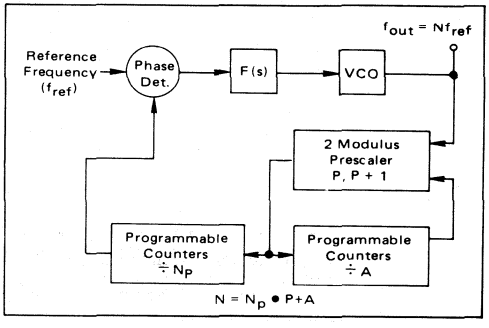
Collecting terms and factoring gives:

$$f_{out} = [(N_P - A) P + A (P + 1)] f_{ref} \quad (6)$$

From equation 6 it becomes apparent that the fractional part of N can be synthesized by using a two-modulus counter (P and P + 1) and dividing by the upper modulus, A times, and the lower modulus (N_P - A) times.

This equation (6) suggests the circuit configuration in Figure 3. The A counter shown must be the type that

FIGURE 3 – FREQUENCY SYNTHESIS BY TWO MODULUS PRESCALING



counts from the programmed state (A) to the enable state, and remains in this state until divide by N_P is completed in the programmable counter.

In operation, the prescaler divides by P + 1, A times. For every P + 1 pulse into the prescaler, both the A counter and N_P counter are decremented by 1. The prescaler divides by P + 1 until the A counter reaches the zero state. At the end of (P + 1) • A pulses, the state of the N_P counter equals (N_P - A). The modulus of the prescaler then changes to P. The variable modulus counter divides by P until the remaining count, (N_P - A) in the N_P counter, is decremented to zero. Finally, when this is completed, the A and N_P counters are reset and the cycle repeats.

To further understand this prescaling technique, consider the case with P = 10. Equation 6 becomes:

$$f_{out} = (A + 10 N_P) \bullet f_{ref} \quad (7)$$

If N_P consists of 2 decades of counters then:

$$N_P = 10 N_{P1} + N_{P0}$$

(N_{P1} is the most significant digit),

and equation 7 becomes:

FIGURE 4 – DIRECT PROGRAMMING UTILIZING TWO-MODULUS PRESCALER

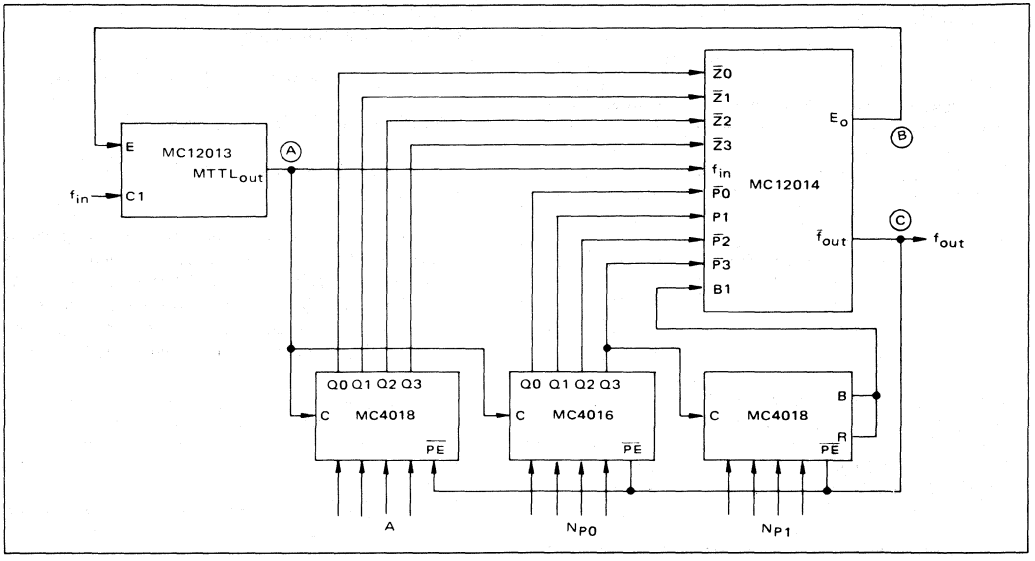


FIGURE 5 – WAVEFORMS FOR DIVIDE BY 43

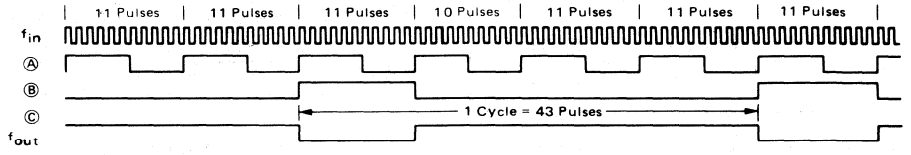


FIGURE 6 – WAVEFORMS FOR DIVIDE BY 42

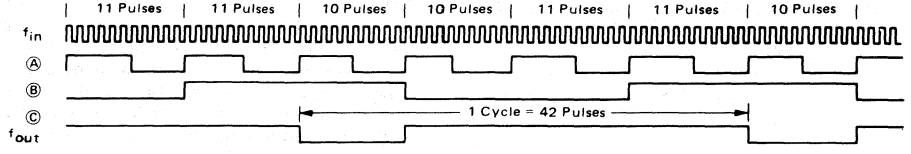
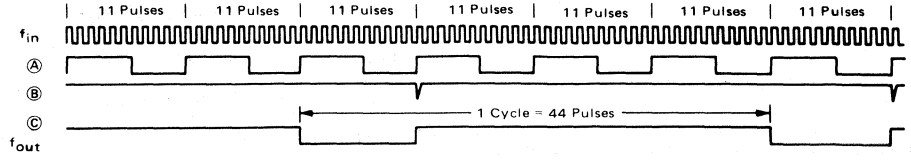


FIGURE 7 – WAVEFORMS FOR DIVIDE BY 44



0

$$f_{out} = (100\,N_{P1} + 10\,N_{P0} + A)\,f_{ref}.$$

To do variable modulus prescaling using the variable modulus prescalers (MC12009/11/13) and programmable divide by N counters (MC4016, MC4018) one additional part is required: the MC12014 (Counter Control Logic).

In variable modulus prescaling the MC12014 serves a dual purpose: it detects the terminal (zero) count of the A counter, to switch the modulus of the MC12013; and it extends the maximum operating frequency of the programmable counters to above 25 MHz. (See the MC12014 data sheet for a detailed description of the Counter Control Logic).

Figure 4 shows the method of interconnecting the MC12013, MC12014, and MC4016 (or MC4018) for variable modulus prescaling. To understand the operation of the circuit shown in Figure 4, consider division by 43. Division by 43 is done by programming $N_{P1} = 0$, $N_{P0} = 4$, and $A = 3$.

Waveforms for various points in the circuit are shown in Figure 5 for this division. From the waveforms it may be seen that the two-modulus prescaler starts in the divide by 11 mode, and the first input pulse causes point A to go high. This positive transition decrements the Np counter to 3, and counter A to 2.

After 11 pulses, point Ⓐ again goes high; the Np counter decrements to 2 and the A counter to 1. The "2" contained in the Np counter enables the inputs to the frequency extender portion of the MC12014. After 11 more pulses point Ⓐ goes high again.

With this position transition at Ⓐ, the output (f_{out}) of the MC12014 goes low, the Np counter goes to 1, and the A counter goes to 0. The zero state of the A counter is detected by the MC12014, causing point Ⓑ to go to 1 and changing the modulus of the MC12013 to 10 at the start of the cycle.

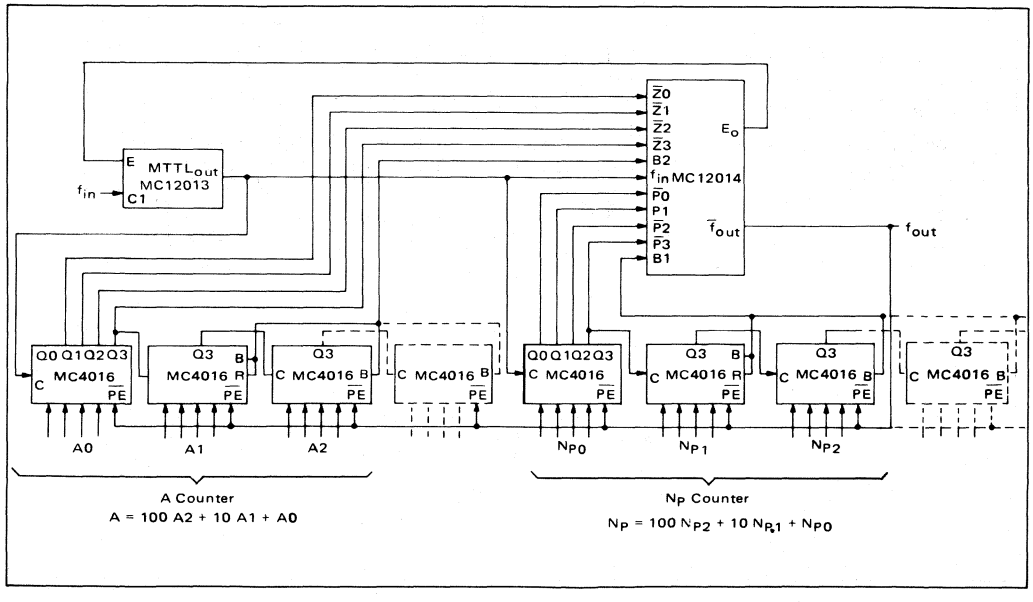
When f_{out} goes low, the programmable counters are reset to the programmed number. After 11 pulses (the enable went high after the start of the cycle and therefore doesn't change the modulus until the next cycle), point Ⓐ makes another positive transition. This positive transition causes f_{out} to return high, release the preset on the counter, and generates a pulse to clear the latch (return point Ⓑ to 0).

After 10 pulses the cycle begins again (point Ⓑ was high prior to point Ⓐ going high). The number of input pulses that have occured during this entire operation is: 11 + 11 + 11 + 10 = 43. Figures 6 and 7 show the waveforms for divide by 42 and divide by 44 respectively.

The variable modulus prescaling technique may be used in any application as long as the number in the Np counter is greater than or equal to the number in the A counter. Failure to observe this rule will result in erroneous results. (For example, for the system shown in Figure 4 if the number 45 is programmed, the circuit actually will divide by 44. This is not a serious restriction since Np is greater than A in most applications).

It is important to note that the A counter has been composed of only one counter for discussion only; where required, the A counter may be made as large as needed by cascading several programmable counters. Figure 8 shows the method of interconnecting counters. Operation is previously described. The number of stages in the A counter should not exceed the number of stages for the

FIGURE 8 -- METHOD OF INTERCONNECTING COUNTERS



N_P counters. As many counters as desired may be cascaded, as long as fan-in and fan-out rules for each part are observed.

The theory of "variable modulus prescaling" developed above, examined a case in which the upper modulus of the two-modulus prescaler was 1 greater than the lower modulus. However, the technique described is by no means limited to this one special case. There are applications in which it is desirable to use moduli other than P/(P + 1).

It can be shown that for a general case in which the moduli of the two-modulus prescaler are P and P + M, equation 6 becomes:

$$f_{out} = [(N_P - A)\,P + A\,(P + M)] \bullet f_{ref}$$

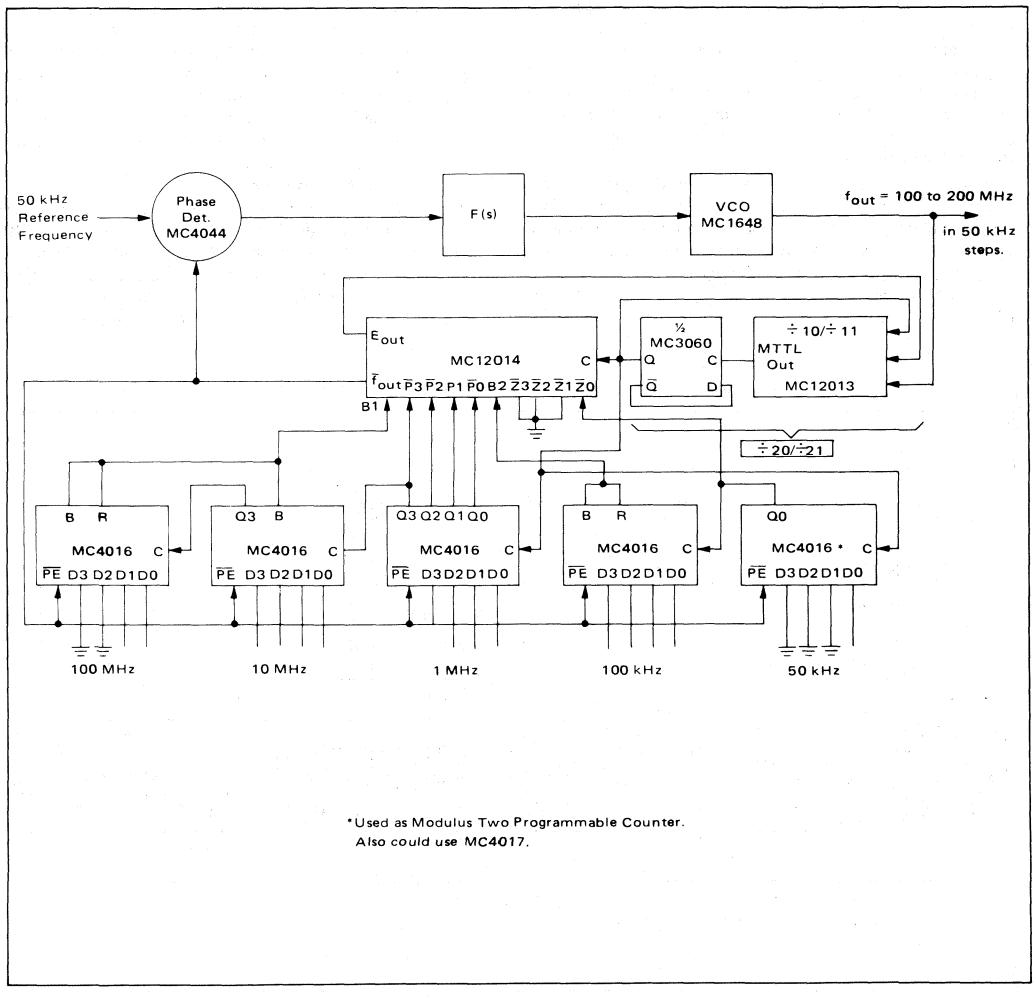
or

$$f_{out} = [N_P \bullet P + M \bullet A] \bullet f_{ref}. \qquad (8)$$

From equation 8 it may be seen that the upper modulus of the two-modulus prescaler has no effect on the N_P counter, and that the number programmed in the A counter is simply multiplied by M.

There is no one procedure which will always yield the best counter configuration for all possible applications. Each designer will develop his own special design for the counter portion of his PLL system.

FIGURE 9 – DIRECT PROGRAMMING 100-200 MHz SYNTHESIZER IN 50 kHz STEPS



*Used as Modulus Two Programmable Counter. Also could use MC4017.

AN969

Operation of the MC145159 PLL Frequency Synthesizer with Analog Phase Detector

INTRODUCTION

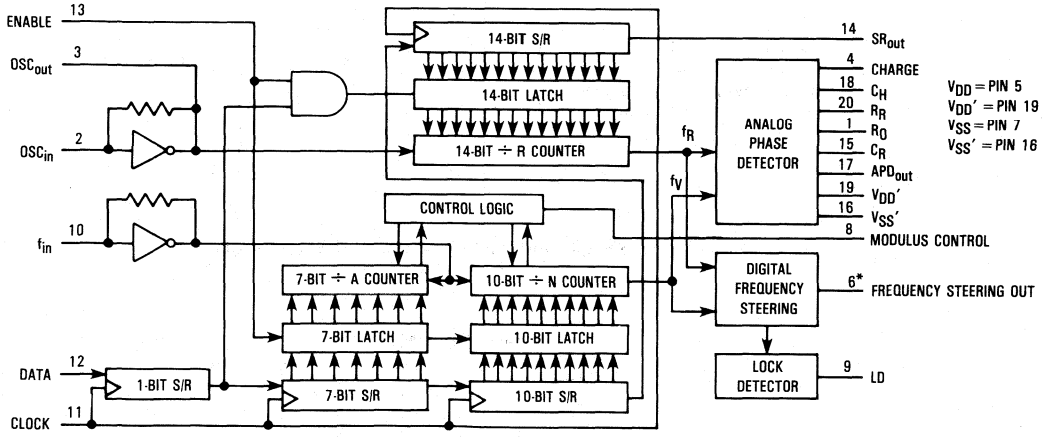
The MC145159 is a phase-locked loop frequency synthesizer with an analog, or more specifically a sample-and-hold, phase detector. The output of this phase detector (APD_{out}) is used as a fine error signal. The synthesizer also contains a digital frequency steering phase comparator for coarse adjustment of loop frequency, separate power supply pins for the analog phase detector, a lock detect output, and on-chip logic for control of a dual-modulus prescaler. (See Figure 1.)

Other features of the MC145159 are a 14-bit reference counter, as well as a 10-bit divide-by-N counter and a 7-bit divide-by-A counter. All three counters are programmed via a serial data stream which is compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs. The device also has on-chip circuitry to support an external crystal. OSC_{in} may also serve as an input for an externally-generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels), dc coupling may be used.

With the features listed above, the MC145159 finds general purpose applications in such areas as 2-way radios, cellular radiotelephones, and avionics equipment.

As stated earlier, the MC145159 has a sample-and-hold phase detector. As opposed to standard digital phase comparators with fixed gain, the gain of the sample-and-hold phase comparator is programmable. Four external components, two resistors and two capacitors, help set the gain and drive levels of the phase detector. Higher gain is achievable with the MC145159 phase detector versus digital phase detectors.

Because a high degree of filtering compromises overall loop performance, phase detectors which provide an error signal that is as clean as possible prior to filtering are extremely advantageous. One obvious benefit of the sample-and-hold phase comparator is that its output is analog, and therefore already resembles the required control voltage necessary to drive the loop's voltage-controlled oscillator (VCO), thereby minimizing filtering requirements. Ideally, this control voltage is a perfectly clean signal with no undesired perturbations. Any of these disturbances cause unwanted modulation on the VCOs output signal. For high performance radio equipment, the sidebands resulting from this modulation must be very low. The analog output reduces VCO modulation sidebands and also allows for wider loop bandwidths than are normally possible with digital phase detector outputs.



*NOTE: Pin 6 is not and cannot be used as a digital phase detector output.

Figure 1. Logic Diagram

TRADITIONAL SAMPLE-AND-HOLD PHASE DETECTORS

Before examining the method by which the MC145159 performs a sample-and-hold function, the theory of operation of traditional sample-and-hold phase detectors will be reviewed.

The reference signal (divided-down OSC_{in} signal) and current source are used to establish the sawtooth voltage on the ramp capacitor, C_R. (See Figures 2 and 3.) C_R is charged by the current source and quickly discharged by a switch that is controlled by the reference signal. In this way, the period of the sawtooth voltage is equal to the period of the reference signal. The divided-down VCO signal is used to sample the sawtooth voltage by closing a sampling switch for a window of time and letting the hold capacitor, C_H, charge to the sampled voltage. Neglecting leakage current, the charge established on C_H at the end of the sample time remains constant until the next sample. If for some reason the VCO frequency begins to rise above the desired value, the phase of the sampling pulse falls back and sampling is done at a lower sawtooth voltage. This action, in effect, lowers the control voltage to slow down the VCO and keep the divided-down VCO frequency locked to the reference frequency. Likewise, if the VCO frequency falls below the desired value, the phase of the sampling pulse advances and sampling is done at a higher sawtooth voltage. This action raises the control voltage which speeds up the VCO to keep the divided-down VCO frequency locked to the reference frequency.

One serious side effect of this scheme is that an undesired ripple voltage occurs on C_H. This rippling is caused by the ramp waveform charging from level V_A to level V_B during the sample window. Upon opening of the sampling switch, C_H is charged to V_B and remains at V_B until the switch is closed again and voltage V_A is applied to the hold capacitor. Therefore, the hold capacitor is charged to V_B and discharged to V_A while in a locked condition. In effect, a ripple-free lock voltage cannot be established on C_H. The magnitude of this ripple is a function of the ramp charging slope, sample window time, and hold capacitor charge/discharge times.

To mask out the rippling effect, one solution is to follow C_H by a second sampling switch and hold capacitor combination along with the necessary control signals. However, this additional circuitry introduces more switching transients and consumes more chip and/or board space.

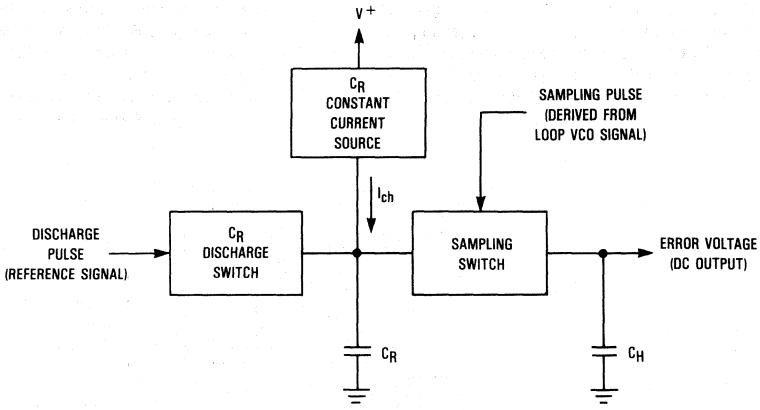


Figure 2. Traditional Sample-And-Hold Phase Detector Block Diagram

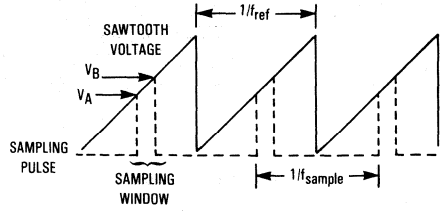


Figure 3. Traditional Sample-And-Hold Phase Detector Timing Diagram

OPERATION OF THE MC145159

THEORY

The MC145159 uses a new, patented design approach for sample-and-hold phase detectors called ramp clamping, which results in improved performance over the traditional approach. Ramp clamping minimizes the need for a second hold capacitor, and in most applications only one hold capacitor is needed. When the loop is in frequency lock, the rising edge of f_R (divided-down OSC_{in} signal) activates a constant current source to initiate charging of the ramp capacitor. (See Figures 4 and 5.) The slope of this ramp waveform is also known as the phase detector gain. The ramp voltage continues to build, at a rate determined by R_R, C_R, and V_{DD}', until the rising edge of f_V (divided-down VCO signal) terminates the charge signal, thereby establishing a constant voltage on C_R. After a predetermined delay (equal to two clock cycles of f_{in}) this ramp voltage is sampled onto the hold capacitor during a sample window lasting four periods of f_{in}. C_H is then isolated from C_R and, after a delay of two clock cycles of f_{in}, C_R is discharged. This cycle repeats every f_R period. The f_V edge relative to the f_R edge in time therefore determines how long the ramp charges before being clamped and sampled onto C_H. This establishes the hold voltage necessary to maintain loop lock. The voltage on C_H feeds an N-channel source follower, the output of which (APD_{out}) controls an external VCO.

When the loop is out of frequency lock, that is when f_R and f_V are not in a one-to-one relationship over a 2π window with respect to f_R, the Frequency Steering Output (FSO) becomes active. As a general rule, f_R and f_V must differ by 2% for the FSO to become active. However, as the reference frequency decreases, the frequency steering sensitivity increases. If the divided-down VCO frequency, f_V, is lower than the divided-down oscillator frequency, f_R, ($f_V < f_R$) then FSO pulses high. If $f_V > f_R$, then FSO pulses low. The FSO pulse width is approximately equal to the period of time between two f_V pulses if $f_V > f_R$, or two f_R pulses if $f_R > f_V$. FSOs repetition rate is equal to the difference frequency between f_R and f_V. When $f_V = f_R$ over a 2π window with respect to f_R, then the FSO remains in a high-impedance state and phase lock is maintained by the analog phase detector output. (See Figure 6.) By combining APD_{out} and FSO, the required low-noise VCO control voltage is provided by APD_{out} while the FSO provides a coarse error signal to achieve fast frequency lock.

The ramp clamp approach to phase detector design, which is implemented on the MC145159, offers significant advantages over the traditional method of sample-and-hold phase comparators. In traditional sample-and-hold detectors, ramp slewing during the sample window causes rippling on the hold capacitor. Therefore, a second hold capacitor and sampling switch may be needed. The ramp clamp technique however, alleviates the need for a second hold capacitor and all of its related circuitry. This becomes very significant in the production of monolithic integrated circuits due to the savings in chip area that result.

Another benefit of ramp clamping is that the ramp amplitude is not allowed to go beyond the value reached when sampling occurs. The traditional method permits the ramp capacitor to charge all the way up to the positive supply voltage value; in most cases well after sampling has occurred. This extends the ramp amplitude beyond that allowed with the ramp clamp approach. A lower ramp pulse results in less ripple in the output error signal caused by parasitic ramp feed-through. With ramp clamping, the ramp amplitude is limited to only that value necessary to keep the loop locked and, more importantly, it provides a constant voltage to the hold capacitor during the entire sample window.

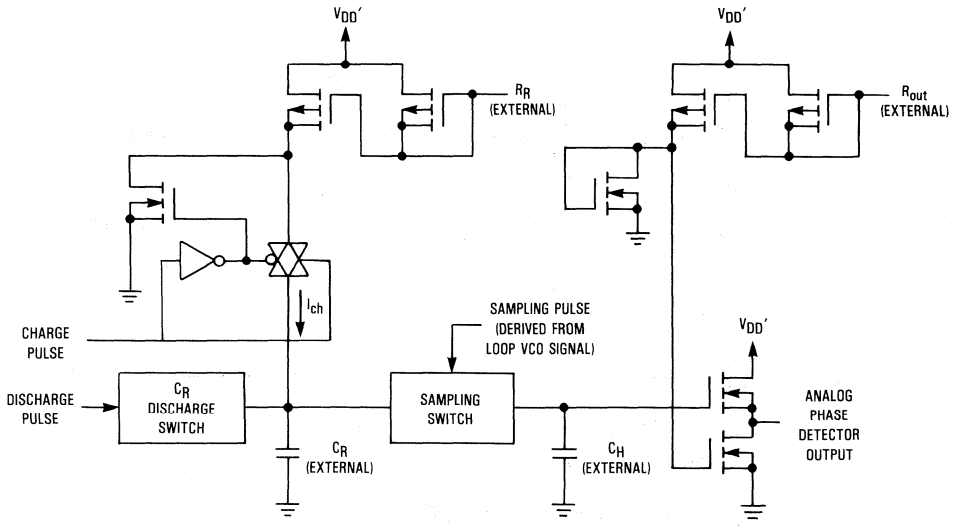


Figure 4. Analog Phase Detector Logic Detail

A word of caution exists for the analog phase detector power supply pins, V_{DD}' and V_{SS}'. These two pins are provided to help isolate the analog section from noise coming from the digital sections of this device and also noise from the surrounding circuitry. Ensure that V_{DD}' and V_{DD} are at the same voltage potential at all times. Likewise, V_{SS}' and V_{SS} must be at the same potential at all times. Otherwise, damage to the MC145159 may occur due to latch up.

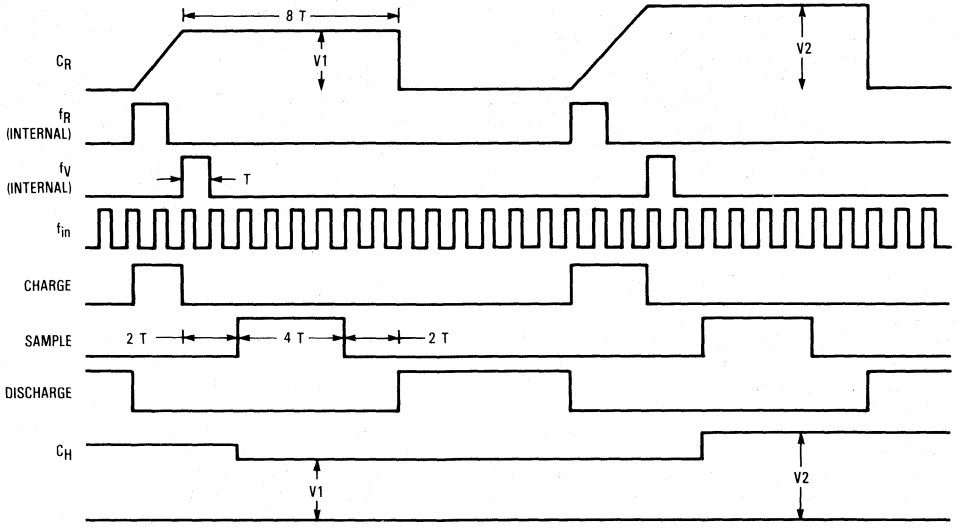
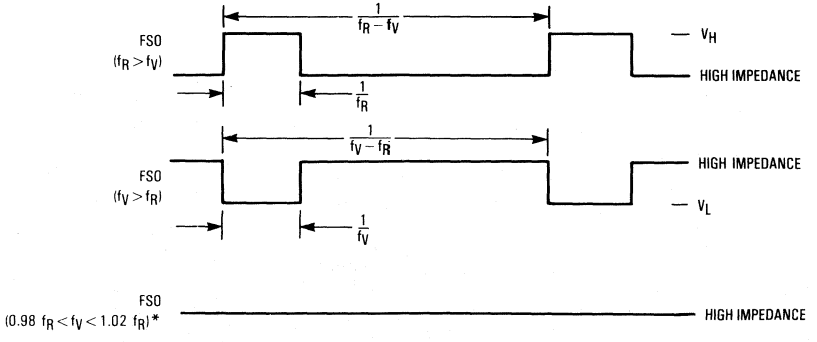


Figure 5. Analog Phase Detector Timing Diagram (N = 17)



NOTE: $f_R = \frac{f_{OSC}}{R}$, $f_V = \frac{f_{in}}{N}$. The R and N counter outputs are not externally available.

*The FSO sensitivity limits are not guarantees, but are design aids.

Figure 6. Frequency Steering Output Timing Diagram

PHASE DETECTOR GAIN

As stated earlier, the gain of the analog phase detector on the MC145159 is programmable. The gain is set by V_{DD}' and two external components; the ramp resistor, R_R, and the ramp capacitor, C_R. The user must therefore determine the optimal value of gain for his or her system.

To select the optimal gain for the phase detector, let us assume a PLL system with a reference frequency of 10 kHz. (See Figure 7a.) With this frequency going into the phase detector, consecutive f_R pulses occur 100 μs apart. Assuming that the Frequency Steering Out pin has already pulled the system into frequency lock and turned off, the Analog Phase Detector Output is in complete control. Therefore, the rising edges of f_R and f_V can be nearly 100 μs apart. Because f_R initiates the ramp waveform and f_V terminates the charging cycle, the ramp should be at most 100 μs, or 2π radians wide. Moreover, the ramp should be capable of charging from V_{SS}' to V_{DD}' during this time. The design equation for phase detector gain given in the data sheet is stated as:

$$K_\phi = \frac{I_{charge}}{2\pi\ f_R\ C_R} \quad [V/rad]$$

Substituting in for K_ϕ and f_R and selecting a value for C_R, one can solve for I_{charge}. From I_{charge}, the value of ramp resistance, R_R, is taken from Figure 8.

In this example, the gain of the phase detector is $V_{DD}'/2\pi$ [V/rad]. Larger values of gain can certainly be used. In fact, higher gain results in faster lock times. (See Figure 7b.) There is, however, an upper limit to the amount of gain selected. Higher gain is achieved by increasing V_{DD}' or reducing R_R or C_R (or some combination thereof). Increasing phase detector gain by reducing the size of the ramp capacitor leads to increased noise induced into the ramp, and consequently, hold capacitors.

On the other hand, too little gain results in the ramp capacitor taking slightly longer to reach the required error voltage level,

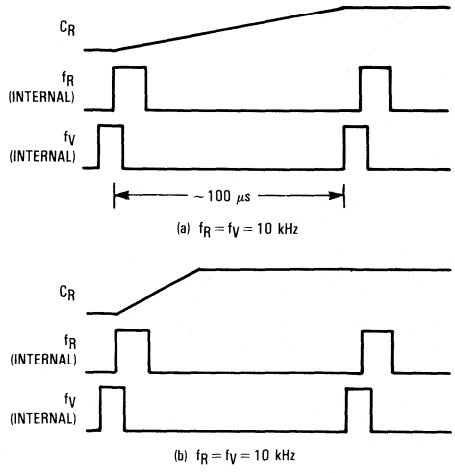


Figure 7. Determining the Gain of the Analog Phase Detector

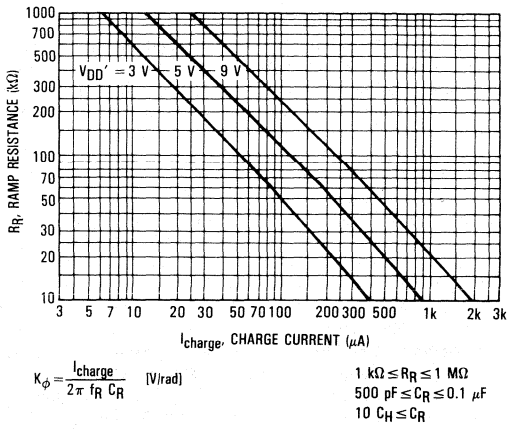


Figure 8. Charge Current versus Ramp Resistance

thereby widening the ramp waveform. This increased area under the curve represents more energy being transferred to the hold capacitor. The result is an increased potential to modulate the control voltage, yielding higher sidebands on the VCO output. Therefore, each system must be carefully analyzed and optimized for the gain/noise tradeoff.

The analog phase detector of the MC145159 can track changes in its input over a 2π range with respect to f_R. The digital frequency steering portion of the device produces error signals over a wide range of input frequency differences.

OUTPUT BIAS CURRENT RESISTOR

Included on the MC145159 is a pin dedicated for use with an external component, called the output bias current resistor. A resistor connected from this pin (R_O) to V_{SS}' biases the output N-channel transistor, thereby setting a current sink on the analog phase detector output. With larger values of output resistance, the analog output bias current decreases (See Figure 9.)

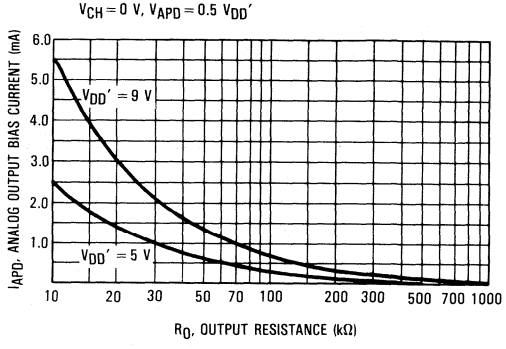


Figure 9. APD_{out} Bias Current versus Output Resistance

METHOD OF PROGRAMMING THE COUNTERS

The MC145159 contains three fully-programmable counters. The R, N, and A counters are programmed by a serial data bit stream. (See Figure 10.) Perusing the logic diagram of the device gives insight as to how the counters are loaded with data. (See Figure 1.)

First, the desired values for R, N, and A must be converted to binary form with the proper amount of bit positions. Note that the R counter is 14 bits long, the N counter 10 bits long, and the A counter 7 bits long. To load the data, the Enable pin must be taken low to isolate the counters from changes that occur in the shift registers. With Enable low, data is then loaded into the shift registers on the rising edge of the clock input. Care must be taken to ensure that Data, Clock, and Enable voltage levels and rise, fall, setup, hold, and recovery times are not violated. The divide-by-R word is loaded first with its most-significant bit as the first bit entered. The divide-by-N word follows immediately, again with its most-significant bit as the first bit entered. Next is word A, similarly with its most-significant bit entering first. The last bit of the string is the control bit. A logic one for the control bit allows all the counters to be loaded with shift register information when Enable is taken high. A logic zero entered as the control bit inhibits a reference counter latch load. Therefore, only the N and A counters are loaded when Enable is taken high.

Finally, after all the data is properly loaded into the shift registers and the control bit is at the desired logic state, Enable is taken high to program the counters. After satisfying the minimum input pulse width for Enable, that pin must then be taken low to isolate the counters from outside disturbances.

For example, suppose system requirements dictate that the R, N, and A counters be programmed with 40, 200, and 72, respectively. The steps to load the counters are outlined below.

R = 40 (14 bits)

0 0 0 0 0 0 0 0 1 0 1 0 0 0
MSB LSB

N = 200 (10 bits)

0 0 1 1 0 0 1 0 0 0
MSB LSB

A = 72 (7 bits)

1 0 0 1 0 0 0
MSB LSB

	Action	Comment
1.	Take Enable low ($<0.3\ V_{DD}$)	Isolate the counters
2.	Shift in eight 0s	Start loading R word
3.	Shift in one 1	
4.	Shift in one 0	
5.	Shift in one 1	
6.	Shift in five 0s	R word entered; start loading N word
7.	Shift in two 1s	
8.	Shift in two 0s	
9.	Shift in one 1	
10.	Shift in three 0s	N word entered
11.	Shift in one 1	Start loading A word
12.	Shift in two 0s	
13.	Shift in one 1	
14.	Shift in three 0s	A word entered
15.	Shift in one 1	Control bit high
16.	Take Enable high ($>0.7\ V_{DD}$)	Load the three counters
17.	Take Enable low ($<0.3\ V_{DD}$)	Isolate the counters

Now that the counters are loaded with the correct information and the system is working properly, changing the output frequency is desired. New values of N and A are chosen while keeping R the same. (R is only used in this case to set up the system resolution.) The same method can be used to program the N and A counters while simply ignoring the R counter. Take Enable low, shift in the appropriate binary data for N and A, shift in a control bit of logic zero to isolate the R counter form the Enable line, and pulse high the Enable input.

For example, suppose the new values for N and A are 178 and 13, respectively. The steps to load the counters are outlined below.

N = 178 (10 bits)

0 0 1 0 1 1 0 0 1 0
MSB LSB

A = 13 (7 bits)

0 0 0 1 1 0 1
MSB LSB

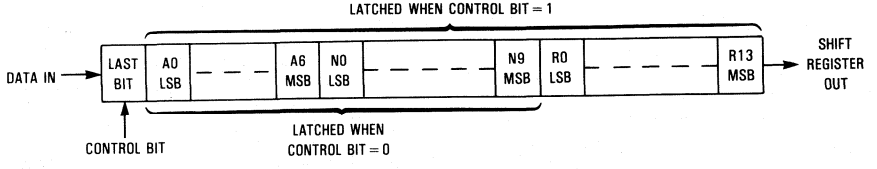


Figure 10. Data Entry Format

Action	Comment
1. Take Enable low	Isolate the counters
2. Shift in two 0s	Start loading N word
3. Shift in one 1	
4. Shift in one 0	
5. Shift in two 1s	
6. Shift in two 0s	
7. Shift in one 1	
8. Shift in four 0s	N word entered; start loading A word
9. Shift in two 1s	
10. Shift in one 0	
11. Shift in one 1	A word entered
12. Shift in one 0	Control bit low
13. Take Enable high	Load the two counters
14. Take Enable low	Isolate the counters

As is evident, the two prior routines are serial in nature. A microprocessor is therefore best suited to program the counters. Also, note that the counter outputs are not available on the MC145159 for checking correct counter operation. However, a shift register output, SR_{out}, is available. (See Figure 1.) Therefore, the same microprocessor that programs the counters can also be used to verify the contents of the shift registers to ensure that the correct data has been loaded. Enable must be held low while verifying shift register contents to avoid affecting the counters.

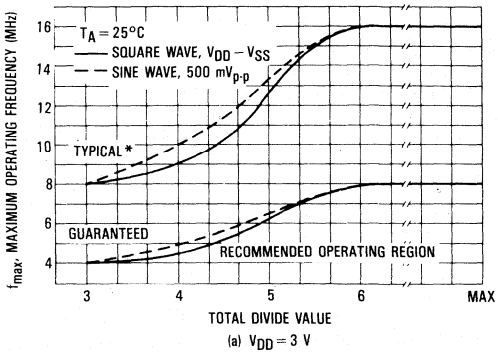
Although the MC145159 has on-chip logic for control of an external dual modulus prescaler, the device is capable of performing in a single modulus mode simply by leaving the modulus control output unconnected. In this case, the 10-bit divide-by-N counter performs the loop divide-by-N function. The A counter must still be loaded with data, but that data is a don't care. However, loading the A counter with all 0s is strongly recommended. In that way, the modulus control output is stuck high and cannot cause any possible interference by switching periodically.

f_{in}, OSC_{in} LIMITS

Although not stated on the data sheet, the f_{in} and OSC_{in} limits for the MC145159 are about the same as the rest of the silicon-gate MC1451XX family of frequency synthesizers. (See Figures 11 and 12.) One limit is 15 MHz for a supply voltage of 5 V and a divide value of six or greater for the N and R counters. Refer to the graphs for frequency limits of the MC145159 counters at other supply voltages.

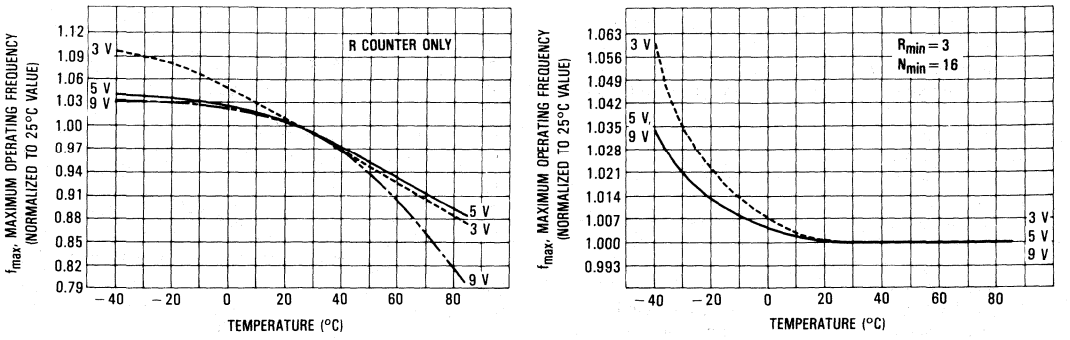
The analog phase detector component values play a small role in determining the input frequency limits at the input to the phase detector. For high reference frequencies, a large value of I_{charge} is most likely required. Make certain that component values are in specified ranges. For best results, the following limits are recommended. (Low-leakage polystyrene or Mylar capacitors are recommended for C_R and C_H.)

$$1\ k\Omega \le R_R \le 1\ M\Omega$$
$$500\ pF \le C_R \le 0.1\ \mu F$$
$$10\ C_H \le C_R$$
$$10\ k\Omega \le R_O \le 1\ M\Omega$$



*Data labelled "Typical" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

Figure 11. OSC_{in} and f_{in} Maximum Frequency versus Total Divide Value ($R_{min} = 3$, $N_{min} = 16$)



(a) TOTAL DIVIDE VALUE = 3, 4, OR 5

(b) TOTAL DIVIDE VALUE ≥ 6

Figure 12. OSC_{in} and f_{in} Maximum Frequency versus Temperature for Sine and Square Wave Inputs

DUAL-MODULUS PRESCALING CONSTRAINTS

The MC145159 contains all the necessary logic for control of an external dual-modulus prescaler. Dual-modulus prescaling is a solution to some of the shortcomings associated with single-modulus prescaling. Inherent in the design of synthesizers using single-modulus prescaling is the fact that the value of the reference frequency into the phase detector is multiplied by the prescale value P, as well as by the counter value, N. (See Figure 13.) This results in a loss of system resolution because any unitary change of N results in the output frequency of the VCO changing by the reference frequency times P, which may be undesired.

Dual-modulus prescaling is a solution to this problem. It allows VCO step sizes equal to the value of the phase detector reference frequency to be obtained. This technique utilizes an additional A counter and a special prescaler which divides by any one of two values, depending upon the state of its control line. (See Figure 14.) In dual-modulus prescaling, the lower speed counters are uniquely configured. Special control logic is necessary to select the divide value, P or P + 1, in the prescaler for the required amount of time.

The modulus control signal is low at the beginning of a count cycle, enabling the prescaler to divide by P + 1, until the A counter has counted down to zero. At this time, modulus control goes high, enabling the prescaler to divide by P, until the N counter counts down the rest of the way to zero; N minus A additional counts.

$$N_{tot} = (P + 1)A + P(N - A)$$

$$= NP + A$$

Modulus Control is then set back low, the counters preset to their respective programmed values, and the sequence is repeated.

This provides for a total programmable divide value of (N times P) + A. To have a range of total divide values in sequence, the A counter is programmed from zero through P − 1 for a particular value N in the N counter. N is then incremented by 1 and the A counter is sequenced from zero to P − 1 again.

Certain constraints apply when using dual-modulus prescaling: 1) N is greater than or equal to A always applies; 2) the value of P must be large enough so that the maximum frequency of the VCO divided by P must not exceed the frequency capability of the N and A counters; also, 3) P times the period of the maximum VCO frequency must be greater than the sum of the prop delay through the dual-modulus prescaler plus the prescaler setup or release time relative to its control signal plus the propagation delay of frequency in (f_{in}) to Modulus Control.

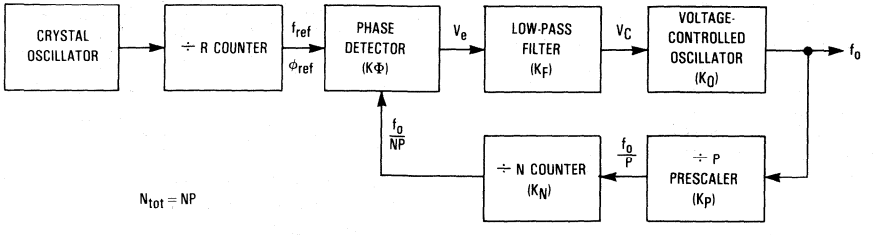


Figure 13. Single-Modulus Prescaling

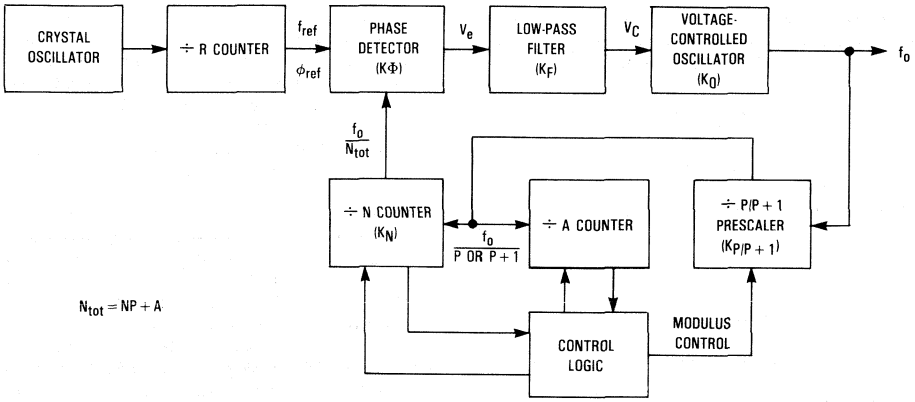


Figure 14. Dual-Modulus Prescaling

FREQUENCY SYNTHESIZER EXAMPLE

Suppose the MC145159 is to be used in a system which operates from 118.000 to 135.975 MHz in 25 kHz steps, i.e., aircraft communication transceivers. (See Figure 15.) A prescaler is needed to divide down the maximum VCO output frequency to a frequency that the MC145159 can handle (15 MHz maximum at $V_{DD} = 5$ V). A minimum prescale value of 10 is required. However, if a divide-by-10 single-modulus prescaler is used, the reference frequency would have to be adjusted to 2.5 kHz in order to maintain the 25 kHz step size. Therefore, dual-modulus prescaling is desired and the MC12016 divide-by-40/41 prescaler is selected due to an input frequency capability of 225 MHz and the ability to divide down the VCO frequency to well under 15 MHz.

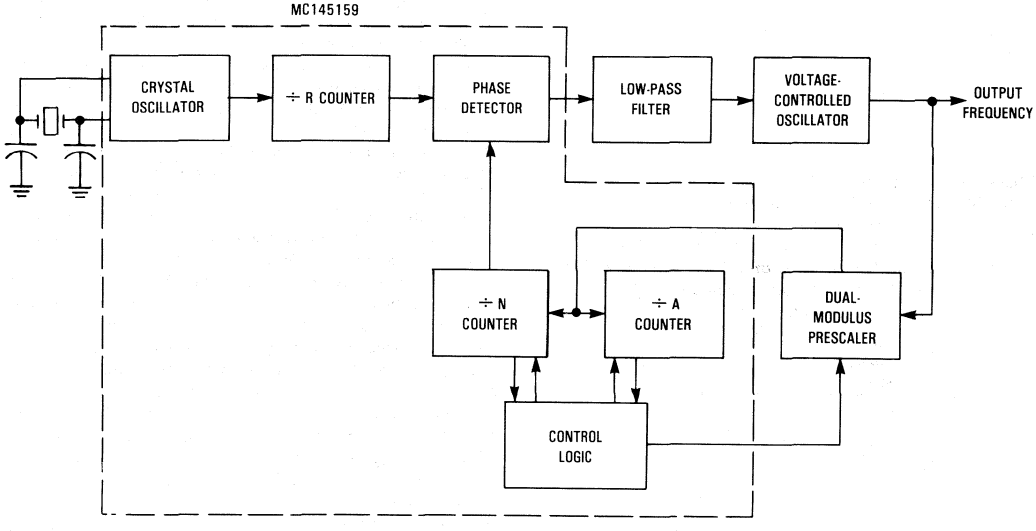


Figure 15. Typical System Application

AN980

VHF Narrowband FM Receiver Design Using the MC3362 and the MC3363 Dual Conversion Receivers

Prepared by: Bipolar Analog Applications

Motorola has developed a series of low power narrowband FM dual conversion receivers in monolithic silicon integrated circuits. The MC3362 and the MC3363 are manufactured in Motorola's MOSAIC process technology. This process develops NPN transistors with f_T = 4 + GHz, which allows the MC3362 and the MC3363 to have excellent very high frequency (VHF) operation with low power drain. They are ideal for application in cordless phones, narrowband voice and data receivers, CB and amateur band radios, radio frequency (RF) security devices and other applications through 200 MHz.

Features of the MC3362/3 Receiver ICs:

- Broadband RF input frequency capability (to 200 MHz using internal oscillator, over 450 MHz using external oscillator)
- Single supply operation from V_{CC} = 2 to 7 Vdc
- Low power consumption (I_{CC} = 3 mA typical at V_{CC} = 2 Vdc)
- Internally biased NPN RF transistor amplifier (MC3363)
- Complete dual conversion circuitry — first mixer and oscillator included
- First local oscillator (LO) includes buffered output and varactor diode to allow phase locked-loop (PLL) frequency synthesis for multichannel operation.
- Buffered second local oscillator output available for PLL reference input (MC3362)
- Multistage limiter and quadrature detection circuitry included
- RSSI (Received Signal Strength Indicator) with Carrier Detect logic included
- Built-in data slicing comparator detects zero crossings of FSK data transmission
- Inverting operational amplifier included for audio muting or active filtering (MC3363)

SCOPE

This application note contains functional descriptions and applications information pertaining to the various functional blocks of the MC3362/3 receiver circuits. Four receiver application circuits are shown. A single channel receiver and a 10 channel frequency synthesized receiver designed for the 49 MHz cordless telephone band are shown. A 256 channel "2 Meter" (144–148 MHz) amateur band receiver is also shown, including an appropriate PLL frequency synthesizer design to control the receiver's local oscillator. Finally, a low cost application featuring the MC3362 as a single chip manually tunable 162 MHz weatherband receiver is shown. A directory of external component manufacturers is included as an appendix.

COMPARISON OF THE MC3362 AND THE MC3363

Figures 1A and 1B show the system block diagrams of MC3362 and MC3363, respectively. The MC3362 and the MC3363 are made from the same die, but a final metal mask difference allows different features to be made available on each. Data pertaining to the common functional blocks are identical on both circuits.

The MC3363 is a complete VHF dual conversion FM receiver including RF amplifier, two mixers and oscillators, limiting IF amplifier and quadrature detection circuitry, received signal strength indicator (RSSI) circuitry, squelch circuitry and a data shaping comparator for detecting FM frequency shift keyed (FSK) data transmissions. Receivers using the MC3363 alone can achieve better than 0.3 μV input sensitivity for 12 dB SINAD, from a 50 Ω source. The MC3363 comes in a 28-lead plastic wide SOIC package only.

The MC3362 is optimized for cordless telephone applications and as such does not contain the RF preamplifier or squelch circuitry. In addition, the second local oscillator contains a buffered output so that it can serve as the system frequency reference in applications where a 10.240 MHz or 10.245 MHz reference is needed. In general, the MC3362 can be substituted for the MC3363 where:

- A receiver with sensitivity of 0.7 μV at the input for 12 dB SINAD is adequate.
- An external RF preamplifier with AGC is desired (such as MOSFET's 3N211 and MPF211).
- Receiver squelch is not needed.
- Surface mount technology cannot be used. The MC3362 is available in two 24-lead plastic packages (DIP and wide SOIC surface mount).

0

MOSAIC is a trademark of Motorola, Inc.

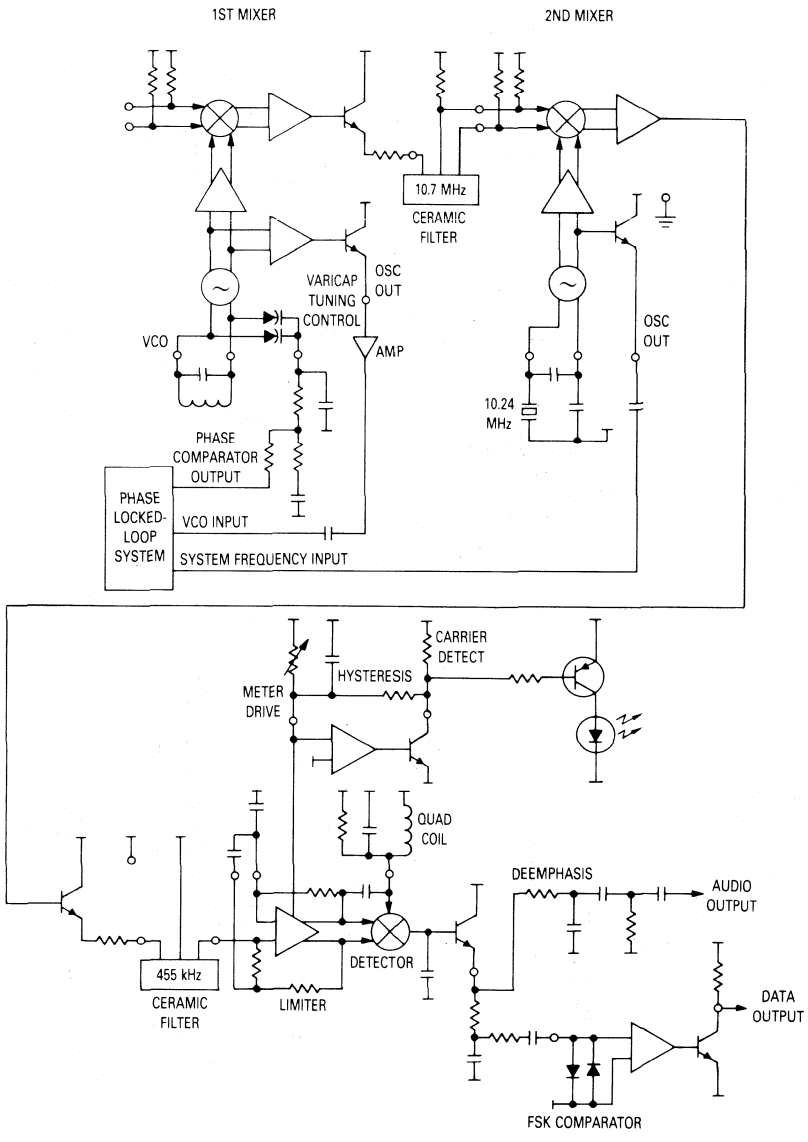
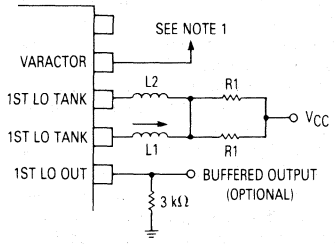
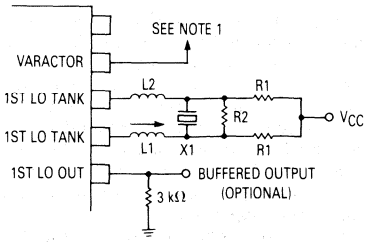


Figure 1A. MC3362 Internal Block Diagram

Initial Alignment of LC Tank



Final Configuration



NOTES:

1. The varactor control pin controls the net capacitance across the local oscillator tank pins. The net capacitance will be approximately 20–25 pF when this pin is left open and 10–15 pF when connected to V_{CC}, depending upon strays and the V_{CC} value used. If the V_{CC} supply is regulated, connect the varactor control pin to V_{CC}; otherwise, bypass via a 0.01 μF capacitor to ground.
2. Connect the oscillator as shown in the left hand drawing (Initial Alignment) and adjust L1 so that the tank resonates approximately 2–3 MHz below the crystal frequency. The frequency should be checked by examining the buffered output using a high impedance probe or by some sort of inductive pickup which will not push the oscillator off frequency. The frequency should be:

$$f_{LO} \approx \frac{1}{2\pi\sqrt{(L1 + L2)\,C_{varactor}}}$$

3. Break the L1–L2 connection and add X1 and R2. Verify that the LO operates at the desired frequency by applying an RF input of 10.7 MHz above or below the crystal frequency and checking for receiver quieting. Make sure that there is proper LO amplitude. Also there should be approximately 200 mVpp seen at either LO tank pin. The buffered LO output should yield 200–600 mVpp depending on the V_{CC} value used.
4. The R2 resistor must be included or else the oscillator will latch.
5. This method has been proven effective up to 65 MHz using 3rd overtone crystals, but has proven unreliable at higher frequencies (usually using 5th and 7th overtone types). For higher frequency operation on a single channel, a signal can be injected into the local oscillator port. (See the "First Mixer and Oscillator" section.)
6. Component values: The R1 resistors should be 10 to 50 kΩ and are included in order to add some current and gain to the local oscillator. L1 should equal L2 in nominal value and a fixed value might be used but startup with different crystals might be degraded. R2 should be 300 to 1500 Ω. X1 should be 3rd overtone, series mode resonant (no load capacitance specified).

Figure 2. Running the MC3362/3 First Local Oscillator on a Single Channel Under Crystal Control

The open circuit conversion voltage gain of the first mixer is typically 24 dB, flat to 7 MHz. Internal rolloff is provided above 7 MHz to suppress RF and LO signals and spurious products sent on to the second mixer. The gain at 10.7 MHz is typically 18 dB. The output circuit is an emitter follower which is impedance-matched to 330 ohms to drive 10.7 MHz ceramic filters which typically have 330 ohm input and output impedances. For applications which require a high impedance crystal filters, impedance matching will likely need to be added at the first mixer's output to preserve the filter's response.

First Local Oscillator and Varactor Diodes

Associated with the first mixer is the first local oscillator (LO). It is a complete voltage controlled oscillator and only requires an external LC tank circuit (no external varactor diode). For multichannel applications, the oscillator includes varactor tuning and a buffered output suitable for interfacing to a PLL frequency synthesizer. This is the approach used in the receivers of Figures 10 and 11. The maximum oscillation frequency obtained has been approximately 190 MHz, achieved by injecting extra current into the oscillator. To inject current into the local oscillator, connect pull-up resistors of 10–50 kΩ from V_{CC} to each LO tank pin. The LO buffered output varies from 400 mVpp to 1100 mVpp with supply voltage and the output waveform appears best with R_{pd} = 3 kΩ, as shown in Figure 3.

There are internal varactor diodes which have capacitance which appears across the local oscillator tank pins. The internal capacitance can range from 10 to 25 pF depending on the control voltage applied to the varactor control pin (MC3362 Pin 23, MC3363 Pin 27). The capacitance is maximum when the voltage applied is at the minimum (0.7 V) value. Applying voltages greater than V_{CC} and lower than 0.7 V to the varactor control pin can cause the oscillator to stop.

The first local oscillator can be crystal controlled to run on a single channel. The procedure of Figure 2 shows how to do this for applications through 65 MHz. The receiver of Figure 10 uses this approach.

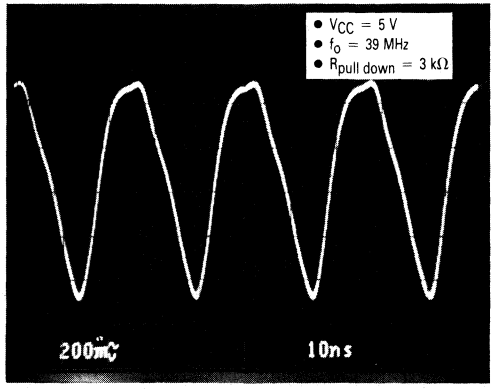


Figure 3. First Local Oscillator Buffered Output

A third application of the local oscillator is to drive it from an external source. This is recommended for applications from 75 MHz to 200 MHz and beyond which do not require PLL frequency synthesis. The inputs are differential and they must be driven using a wideband RF transformer or balun. The input voltage seen at either tank pin should be roughly 100 mVrms to ensure proper operation of the mixer and care should be taken so that any inductance present at the LO tank pins does not resonate with the internal varactor capacitance (a small valued resistor of 50–100 Ω should ensure this does not occur). Using this approach, no loss in mixer gain is seen until the RF and LO inputs are taken over 450 MHz. The RF and LO inputs should be run with a 10.7 MHz difference in frequency to accommodate the first IF bandwidth, so image frequency considerations (preselector filter quality) may limit the maximum RF input frequency to less than 450 MHz.

Second Mixer and Second Local Oscillator

After the 10.7 MHz IF signal is filtered using a ceramic filter, it is applied to the second mixer input. The second mixer is also doubly balanced to reduce spurious responses and typically is used to convert the 10.7 MHz IF down to 455 kHz for application to the limiting amplifier and detection circuitry. In the typical low cost application, the mixer is driven single-endedly from a ceramic filter, with one of the mixer inputs bypassed directly to the V_{CC} supply. The open circuit conversion voltage gain is typically 25 dB. For applications which require a high impedance crystal filter, impedance matching will likely need to be added at the second mixer input to preserve the filter response. The second mixer output is rolled off above 500 kHz, to reduce spurious response and idle noise.

The second local oscillator is a Colpitts type which is typically run under crystal control. The crystal used is specified for fundamental mode operation, calibrated for parallel resonance with a load capacitance of 30–40 pF. The typical waveform seen at the base is shown in Figure 4. The oscillator can be run at 10.240 MHz or 10.245 MHz, depending on the first local oscillator frequency desired.

The MC3362 second local oscillator has a buffered output available which can be used to drive the reference frequency input of a PLL synthesizer or a prescaler. An external local oscillator signal can be injected into the local oscillator's base, with the emitter pin left open. The signal should be sinusoidal and should be approximately 300 mVpp to 500 mVpp in level.

The output admittance of the second mixer at 500 kHz is 1500 Ω in parallel with 50 pF; that is, Rp = 1500 Ω and Cp = 50 pF. The series equivalent impedance is Rs = 1420 Ω and Cs = 1065 pF. This impedance matches the typical input impedance of standard 455 kHz ceramic filters, which have 1500–2000 Ω typical input and output impedances.

Limiting IF Amplifier and Quadrature Detector

The 455 kHz IF signal is applied to the limiting IF amplifier, where it is amplified and limited before application to the quadrature detection circuitry. The limiting IF amplifier input has an input impedance of approximately 1.5 kΩ, which provides good power transfer from 1.5 kΩ ceramic filters. The limiting IF circuitry has 10 μV input sensitivity for −3 dB limiting, flat to 1 MHz. In order to preserve overall power supply current drain, the limiting IF and the receiver in general are not designed for wideband applications.

The coupling capacitor from limiter output to quadrature tank and detector input is provided internally and its value is 5 pF. The 455 kHz oscillator circuit is typically built around an LC tank circuit, with Cp = 180 pF, Lp = 680 μH. **Typical ceramic resonators can not be driven from the quadrature tank pin.** A waveform like that of Figure 5 should appear at the quadrature tank pin during periods of full receiver quieting and no modulation.

Meter Drive (RSSI)

The amplitude of the RF input signal at the appropriate frequency is monitored by meter drive circuitry. This circuitry detects the amount of limiting in the limiting IF amplifier and produces a linear change in current (nominally 0.1 μA) at the meter drive pin for each decibel of change in the RF input. The meter drive circuitry is fairly

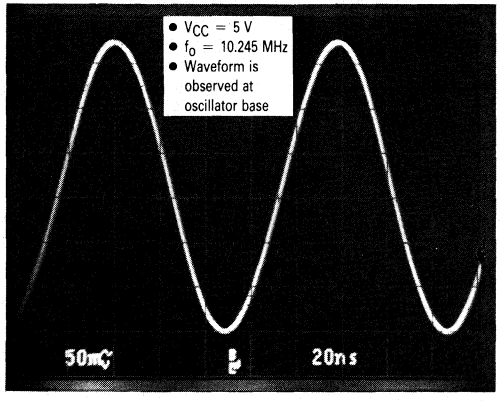


Figure 4. Second Local Oscillator Waveform

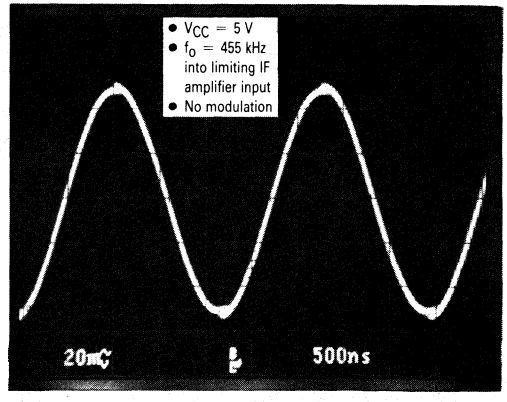


Figure 5. Quadrature Tank Pin Waveform Under Strong Received Signal Condition

linear for input signal levels over a 60 dB range. This output can be used as a meter drive or Received Signal Strength Indicator (RSSI) and needs to be bufffered. In order to provide a linear, wide ranging RSSI output voltage, three things must be accomplished:

1. The Meter Drive pin (MC3362 Pin 10, MC3363 Pin 12) should be clamped to within $V_{BE}/2$ (approximately 300 mV) of the MC3362/3 supply voltage, or loading of the Meter Drive's current source will occur. **The carrier detect output is disabled (high output) when the Meter Drive pin is clamped in this manner.** There are diodes present at the Meter Drive pin which can interfere with the Meter Drive. (See Figure 6 for a schematic representation.) With these diodes present the voltage swing possible at the Meter Drive pin is limited to a diode drop above and below the V_{CC} supply.
2. Some type of current to voltage conversion must take place. The RSSI output is typically 4 to 12 μA.
3. Negative feedback must be provided in the output buffer to counteract buffer amplifier gain variations. Some method of output level adjustment may be desirable.

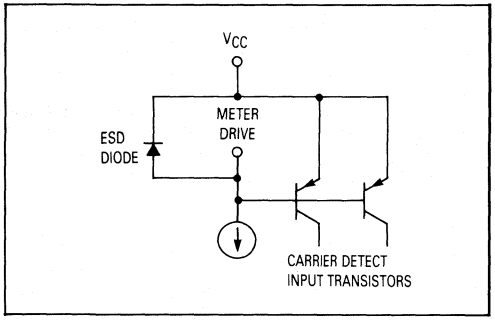


Figure 6. Schematic Representation of Meter Drive "Parasitic Circuits"

Carrier Detect

Another configuration for the meter drive and carrier detect circuitry, is to program the carrier detect output using a resistor from the meter drive pin to the V_{CC} supply. The carrier detect pin is an open collector output so a pull-up resistor is required. The carrier detect is active low, meaning that an RF input above the programmed trip level will yield a low output (<0.1 V) at the carrier detect pin. When the RF input is below the trip level (or is detuned) the carrier detect pin will be at the supply voltage. The trip level is set by the resistor value used between the meter drive pin and supply. A resistor of 130 kΩ sets the trip level to approximately −110 dBm at the first mixer's input, which is roughly the 12 dB SINAD point of the receivers with no external RF amplification. It should be noted that the meter drive current will not have the same linear 0.1 μA/dB current-input level relationship as when the meter drive is buffered as discussed above, so an analog RSSI output is not really achievable when Carrier Detect is used.

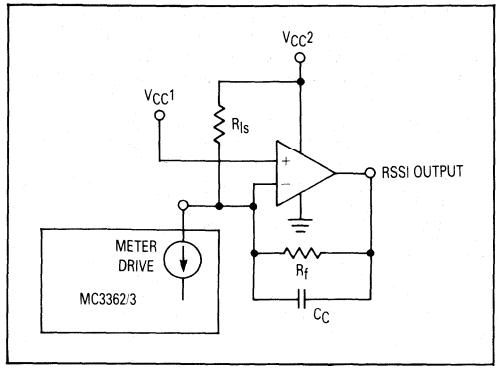


Figure 7. Sample RSSI Buffer

- Recommend MC33171 as the operational amplifier. The MC33171 is a low-power single supply single op amp with offset adjustment capability.
- $V_{CC}1$ = MC3363 supply (2 V to 7 V)
- $V_{OUT} = V_{CC}1 + I_{meter}(R_f)$
- $V_{CC}2$ = Op amp supply. Make this high enough to stay within the op amp's common mode input range — equal to $V_{CC}1$ + 2.2 V for the MC33171. This voltage also must be high enough to provide the maximum V_{OUT} desired.
- R_{IS} can be added to level shift the output, and is optional. The output voltage will be adjusted downward by a factor of $(V_{CC}1 - V_{CC}2)(R_f/R_{IS})$.
- Compensation capacitor C_C is added to ensure stability and will limit the circuit's response time.
- This circuit is not recommended for general purpose AM detection.

Muting (MC3363 only)

Audio muting can be provided in two ways. The carrier detect output can be DC coupled to the MC3363 muting op amp input (Pin 15) and the op amp output can serve to mute the audio. That is, the op amp output (Pin 19) serves as a switch to ground in the audio signal path. When the carrier level decreases below the carrier detect trip point, the carrier detect pin will go to V_{CC} and the op amp output will go into saturation, muting the audio. This yields a simple squelch with minimum external components and is shown in Figures 10 and 14.

Another way to mute the audio on MC3363 is to use the op amp as an active filter for detecting noise above the audio passband. The recovered audio is fed through the active filter, rectified, integrated and compared to a reference level. When the level rises above the reference, a squelch gate is triggered. The data slicing comparator on the MC3363 might be used as a squelch gate. This noise triggered squelch would be executed similarly to the squelch in MC3357/59/61 FM IF applications. (See the MC3359 data sheet for details.) This type of squelch frees the Meter Drive circuit to provide a linear output as noted under "Meter Drive (RSSI)" above.

Data Recovery

Both receivers contain a data slicing comparator which provides data shaping and limiting of frequency-shift keyed (FSK) serial data transmissions. The data slicer is a non-inverting type, with the negative input terminal biased internally to $V_{CC}/2$. Typically the data slicer is AC coupled to the recovered audio pin via a 0.01 μF to 0.1 μF capacitor. Larger coupling capacitors can cause distortion of the detected output and this is seen as negative slew rate limiting in Figures 8 and 9. A pull down resistor from the detector output pin to V_{EE} will reduce this effect if objectionable. The comparator output is an open collector so a pull-up resistor is required.

Comparator hysteresis is available by connecting the comparator output and input using a high-valued resistor. This helps maintain data integrity as the recovered audio becomes noisy, or for long bit strings of one polarity. Resistor values below 120 kΩ are not recommended as the comparator input signal will not be able to overcome the large hysteresis induced. Figure 8A shows data jitter resulting from noisy demodulated data signal. The improvement seen when hysteresis was added is shown in Figure 8B.

The maximum usable FSK data rate for any narrowband FM system is typically 1200 baud subject to IF and quadrature bandwidth and adjacent channel spacing limitations. The approximate bandwidth required to generate or receive a frequency modulated signal is:

BW $\approx$ 2 (f_{mod} + f_{dev}) kHz, where f_{mod} is the modulating frequency and f_{dev} is the frequency deviation.

This is known as Carson's Rule and is fairly accurate. Any modulating signal which exceeds the available IF bandwidth will be attenuated and/or distorted. For proper recovery of square waves including the leading and trailing edges approximately the 7th harmonic should be present. For a 1200 baud (600 Hz) square wave with f_{dev} = 3 kHz, f_{mod} = 4.2 kHz (7th harmonic of 600 Hz square wave), the bandwidth needed is: BW $\approx$ 2(4.2 + 3) kHz = 14.4 kHz = $\pm$7.2 kHz, which is acceptable in narrowband FM channels. Figures 9A and 9B show the effect of trying to pass a 9600 baud modulated carrier through a narrowband channel, with resulting degradation of recovered data.

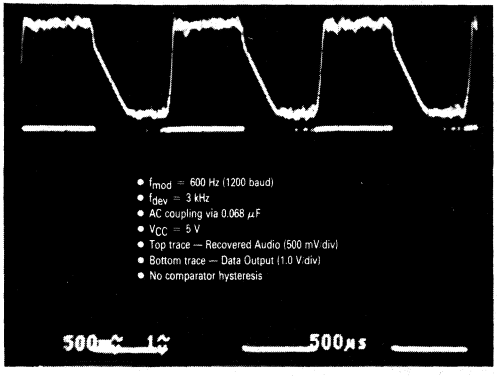


Figure 8A. Noisy Recovered Data Signal Causes Data Jitter

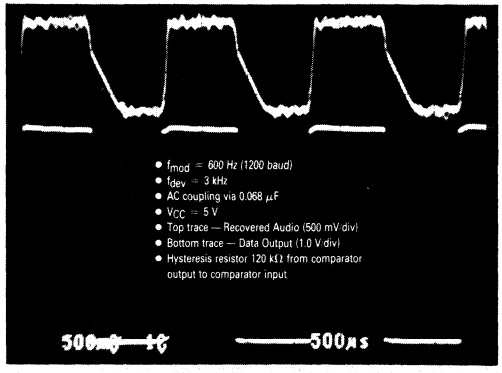


Figure 8B. Improvement in Data Jitter Through Addition of Hysteresis

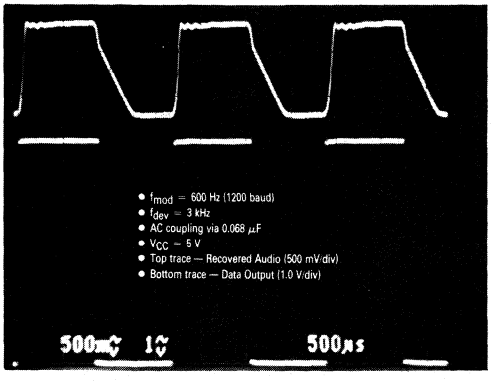


Figure 9A. FSK Data Recovery at 1200 Baud

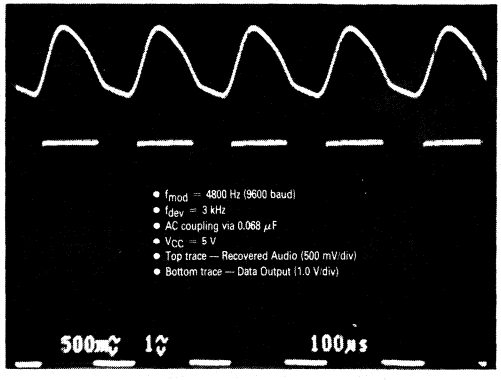


Figure 9B. Distortion of Recovered Audio with 9600 Baud Modulation

10

For narrowband RF modems where 300 baud is adequate, an audio frequency shift keyed (AFSK) approach is recommended. In this application two audio tones (for Logic "0" and Logic "1") are modulated onto an RF carrier and transmitted to the receiver, which reproduces the audio tone sequence. The audio tones can be generated at the transmitter and decoded after the receiver by the MC145442/3 single chip 300 baud modems.

BREADBOARDING

Do not attempt to build a high frequency radio circuit using a wirewrap or plug-in prototype board. While the MC3362 and the MC3363 are "tame" as high gain receivers go, high frequency layout techniques are critical to obtaining optimal receiver performance. This means (typically) a one- or two-sided copper clad board with adequate ground plane connected to V_{EE} potential. **It is also important that all V_{CC} interconnections are made using copper traces on the board. Do not use "free floating" point to point wiring for the V_{CC} interconnections!** In general, keep all lead lengths as short as possible, with an emphasis on minimizing the highest frequency path-lengths. Decoupling capacitors should be placed close to the IC. If these techniques are not followed then the receiver sensitivity and noise quieting will suffer, and oscillations can occur.

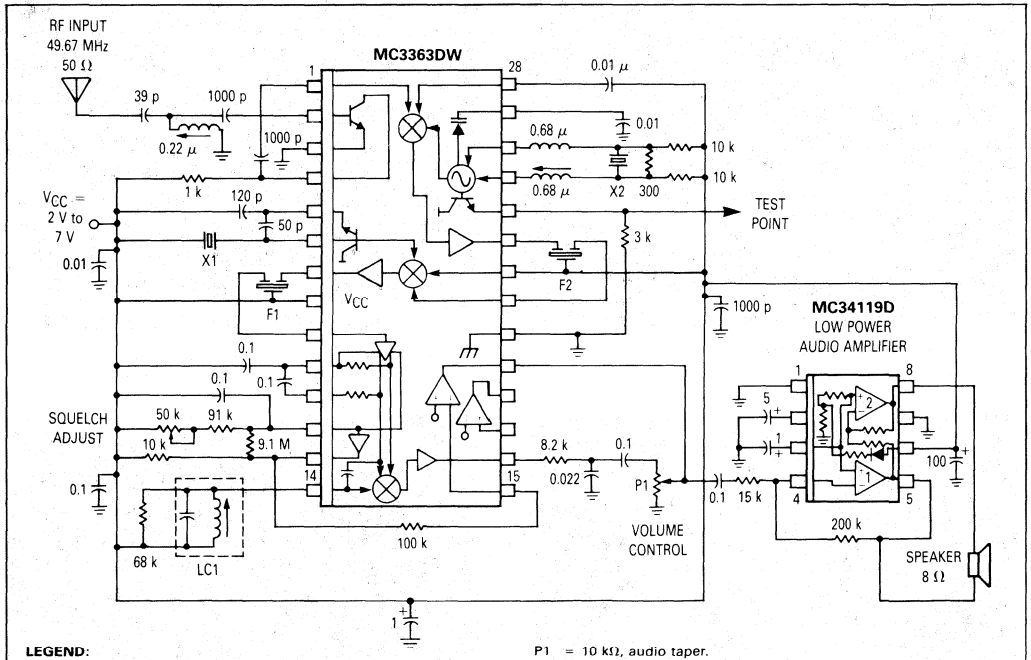
APPLICATIONS CIRCUITS

Single Channel VHF FM Narrowband Receiver

The first application shown is of a complete single channel VHF receiver operating at 49.67 MHz. This application includes a suitable circuit for running the first local oscillator under crystal control on a single channel, which is particularly useful for dedicated remote control links and low cost two-way radios through 75 MHz. The circuit contains a simple carrier level based squelch circuit and audio amplification.

The 49.67 MHz receiver frequency is within the 49 MHz USA cordless telephone band. Radios built for this band may qualify under FCC Code of Federal Regulations Title 47, Part 15, for use by unlicensed operators. It is important to know the federal regulations concerning a particular frequency channel or band of channels before a receiver circuit is design **(see the notes on FEDERAL REGULATIONS, RECOMMENDED STANDARDS above).**

Figure 10 shows the complete receiver schematic. The LC network shown is used to match the input impedance



LEGEND:

X1 = 10.245 MHz, fundamental mode, load capacity 32 pF.

F1 = 455 kHz ceramic filter, R_{in} = R_{out} = 1.5 kΩ to 2 kΩ. Part numbers are muRata CFU455X or CFW455X — suffix denotes bandwidth.

LC1 = 455 kHz quadrature tank circuit. Part numbers are Toko RMC2A6597 HM or 5SVLC-0637BGT (smaller). Ceramic discriminators cannot be used with the MC3362/3, as their input impedance is too low.

P1 = 10 kΩ, audio taper.

F2 = 10.7 MHz ceramic filter, R_{in} = R_{out} = 330 Ω. Part numbers are muRata SFE10.7MJ-A, SFA10.7MF5, or SFE10.7MS2-A.

X2 = 38.97 MHz, 3rd overtone, series mode (no load capacity specified).

All capacitors in microfarads, inductors in Henries and resistors in Ohms unless otherwise specified.

Figure 10. Single Channel FM VHF Receiver at 49.67 MHz

of the RF amplifier to 50 Ω at this frequency. The amplifier collector load is a single resistor for simplicity and in order to enhance stability. The method of Figure 2 was used to develop the crystal controlled oscillator circuit at 38.97 MHz. The RC integrator rolls off the audio above 2 kHz in order to minimize unwanted noise output. This enhances receiver sensitivity and provides proper audio deemphasis. The receiver, without the audio amplifier, has 6.2 mA current drain at V_{CC} = 5 V for a total dissipation of 31 mW. Using a 455 kHz filter with a 6 dB bandwidth of ±10 kHz the receiver has a 12 dB SINAD point of 0.28 μV, modulation acceptance of 10.4 kHz and distortion below 1.2% with f_{mod} = 1 kHz and modulation deviation f_{dev} = 3 kHz. The maximum (S+N)/N ratio obtained is 60 dB.

The MC34119 audio amplifier adds 3 mA quiescent current drain at 5 V, can deliver 250 mW into an 8 Ω speaker and has differential outputs which eliminate the need for the typical large audio coupling capacitor. It also has a chip disable input which provides muting and power conservation.

Ten Channel Frequency Synthesized Cordless Telephone Receiver

A demonstration receiver circuit has been built featuring the MC3362 and the MC145160 dual phase locked loop (DPLL). This receiver features frequency synthesis to cover the ten channels allocated in the USA for cordless telephone (CT) receivers in the 46 MHz (handset) and 49 MHz (base station) frequency ranges. The MC14516X series DPLL's feature two complete loops which control both the transmitter output and receiver first LO frequencies.

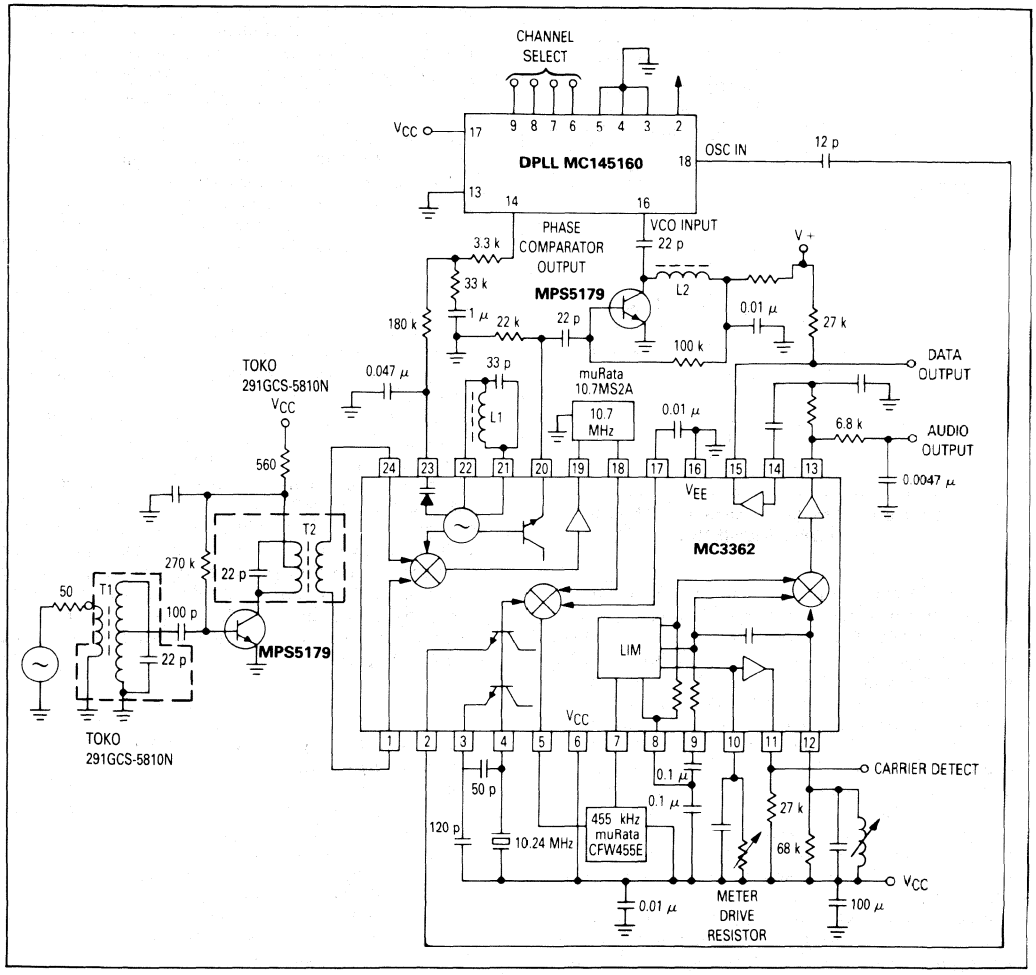


Figure 11. Ten Channel Frequency Synthesized Receiver

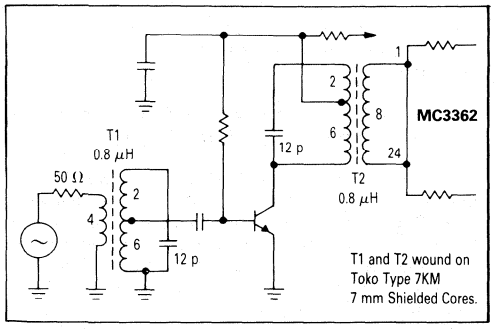


Figure 12. Information on T1 and T2 of Figure 11

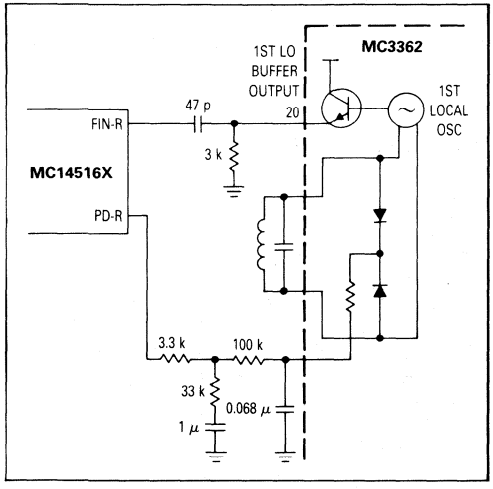


Figure 13. Simple Interface of MC3362/3 To DPLL MC14516X

Figure 11 shows the complete schematic diagram. A simple RF transistor amplifier is included to overcome antenna and RF preselector losses. The output of the VCO buffer is amplified by an external transistor amplifier so that the VCO signal strength is large enough to drive the receiver input pin (Fin-R) of the DPLL properly. Gain of the VCO is set at approximately 400 kHz using the LC values shown. The SB (Pin 3) of the MC145160 is grounded to disable the transmit loop to simplify development of the circuit and reduce power consumption. The DC voltage at the varactor control input of the MC3362 (Pin 23) is adjusted to $V_{CC}/2$. The system reference frequency of 10.240 MHz is generated in the MC3362 second LO and fed into the Osc-In (Pin 18) of the MC145160.

With a supply voltage of V_{CC} = 3 V and modulating signal f_{mod} = 1 kHz, f_{dev} = 3 kHz the receiver yields an input sensitivity of 0.6 μV for 20 dB noise quieting and 0.2 μV for 12 dB SINAD from a 50 Ω source. The audio distortion is less than 3 percent. The minimum noise floor is less than 80 μV and the maximum (S + N)/N ratio is 53 dB.

There is a simpler way to interface the MC3362/3 to the MC145160 DPLL as shown in Figure 13. The VCO signal (about 400 mVpp with V_{CC} = 3 V using a pull-down resistor of 3 kΩ from the MC3362 Pin 20 to V_{EE}) is fed directly into the Fin-R input (Pin 16) of the MC145160. With this configuration, the noise floor is raised to 245 μV, 10 dB higher than the circuit of Figure 11.

256 Channel Frequency Synthesized Two Meter Amateur Band Receiver

A more traditional PLL frequency synthesizer approach is needed to provide frequency flexibility and to allow the MC3362/3 receivers to operate in the VHF "high band" (130 MHz to 172 MHz). A receiver is shown which covers the entire Two Meter (referring to radio wavelength) amateur radio band from 144 MHz to 148 MHz in 256 channels spaced at 20 kHz. The complete receiver and PLL frequency synthesizer are shown in Figures 14 and 15. The receiver achieved the same specifications as the 49.67 MHz MC3363 receiver discussed above.

The MC3363 receiver was chosen because squelch and good sensitivity with minimum component count were desired. To obtain good operation of MC3363 VCO above 75 MHz, the first local oscillator must be running well. To ensure this, the V_{CC} supply voltage is kept above 3 V which increases the current in the local oscillator circuitry. Extra current is also injected into the local oscillator via pull-up resistors of 10 kΩ from each of the local oscillator tank pins to the V_{CC} supply. With the components of Figure 14, the receiver VCO had an average gain of 1.5 MHz/V.

The VCO output is amplified and fed into an MC12017 dual modulus prescaler which drives the input of the PLL frequency synthesizer. The MC145152-2 PLL frequency synthesizer was chosen for its ease of use and parallel input format. The MC33171 bipolar operational amplifier was chosen as the active integrator (loop filter) because of its low power drain, offset adjustment capability and ability to operate from a single supply voltage. The design equations and assumptions used to determine loop filter components are shown below. The MC145152-2 data sheet and other sources go into much more detail on PLL theory and performance.

Calculations of Loop Filter For VCO PLL Frequency Synthesis

Assumptions:

f_o = 135.3 MHz (local oscillator center frequency)
f_s = 20 kHz (channel spacing)
f_b = 0.01 f_s (loop bandwidth)
f_{rc} = 20 f_b (filter cutoff frequency)
§ = 0.707 (loop damping factor)
V_{DD} = 5 V (PLL supply voltage)
K_{VCO} = 9.4 x 10^6 rad/V (VCO gain, measured on MC3363 receiver)
C1 = 0.1 μF (active integrator component)

Results:

$f_b = 0.01\ f_s = 0.01\ (20\ kHz) = 200\ Hz$

$f_{rc} = 20\ f_b = 20\ (200) = 4\ kHz$

$K_\phi = V_{DD} / 2\pi = 0.796$ (phase detector gain)

$$\frac{w_n = 2\pi f_b}{\{2\S^2 + 1 + [(2\S^2 + 1)^2 + 1]^{0.5}\}^{0.5}} = \left(\frac{1257}{2.06}\right) = 610\ rad/sec$$

$N_t = f_o / f_s = 135.3\ MHz / 20\ kHz = 6765$

$R_1 = K_\phi K_{VCO} / (C1\ w_n^2\ N_t) = 29.7\ k\Omega \approx 30\ k\Omega$

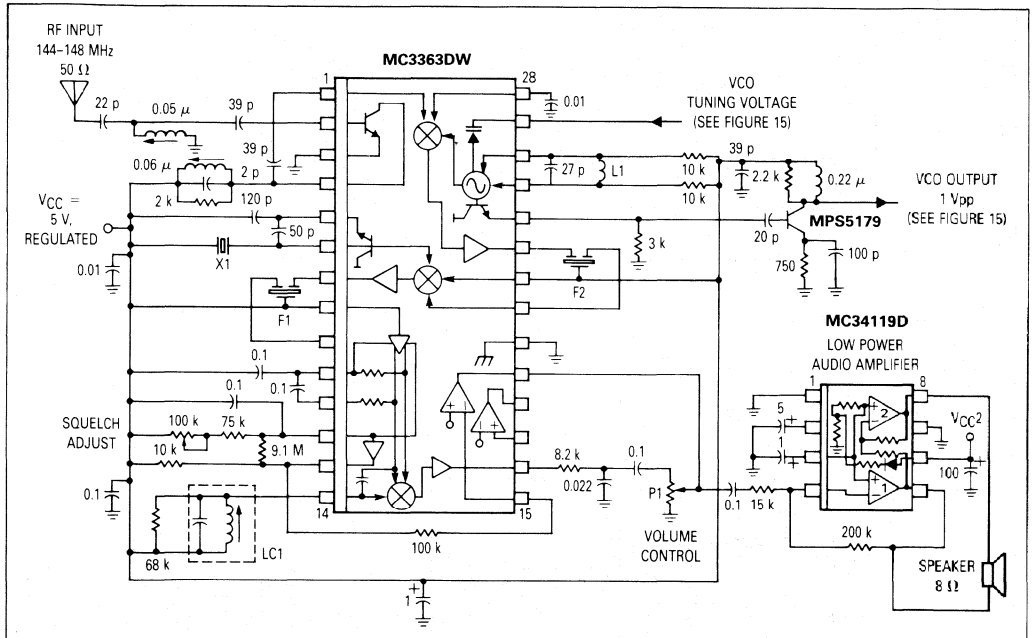
$R_2 = 2\ \S \div (w_n\ C1) = 23.2\ k\Omega \approx 24\ k\Omega$

$C_C = 4 \div (2\ R_1 f_{rc}) \approx 0.017\ \mu F$

With an 8 bit parallel input format several possible switch settings and resultant counter values and receiver frequencies are shown in Table 2 below (Note: $N_t = NP + A$, where P = 64 for the MC12017).

Table 2. PLL Frequency Synthesizer Switch Settings and Frequencies

Switches	N	P	A	N_t	f_{VCO} (MHz) = $N_t f_s$	f_{rx} (MHz) = f_{VCO} + 10.7 MHz
00000000	104	64	0	6656	133.12	143.82
00000001	104	64	1	6657	133.32	143.84
01000000	105	64	0	6720	134.40	145.10
01111111	105	64	63	6783	135.66	146.36
10000000	106	64	0	6784	135.68	146.38
10001101	106	64	13	6797	135.94	146.64
10011100	106	64	28	6812	136.24	146.94
11010001	107	64	17	6865	137.30	148.00
11111111	107	64	63	6911	138.22	148.92



LEGEND:

X1 = 10.245 MHz, fundamental mode, load capacity 32 pF.

F1 = 455 kHz ceramic filter, $R_{in} = R_{out} = 1.5\ k\Omega$ to 2 kΩ. Part numbers are muRata CFU455X or CFW455X — suffix denotes bandwidth.

LC1 = 455 kHz quadrature tank circuit. Part numbers are Toko 7MC-8128Z or 5SVLC-0637BGT (smaller). Ceramic discriminators cannot be used with the MC3362/3, as their input impedance is too low.

P1 = 10 kΩ, audio taper.

F2 = 10.7 MHz ceramic filter, $R_{in} = R_{out} = 330\ \Omega$. Part numbers are muRata SFE10.7MJ-A, SFA10.7MF5, or SFE10.7MS2-A.

L1 = 3 Turns #18 AWG, 0.25" diam., 0.125" spacing, air wound.

$V_{CC}2$ = 2–12 V, must be well decoupled from the V_{CC} source for the MC3363.

All capacitors in microfarads, inductors in Henries and resistors in Ohms unless otherwise specified.

Figure 14. 2 Meter Frequency Synthesized FM Receiver

Single Chip Weatherband Receiver

An application of the MC3362 as a simple receiver tuned to the NOAA Weatherband (162.4 MHz to 162.55 MHz) is shown in Figure 16. The RF input is applied directly to the mixer input, using a simple "L network" to provide impedance matching of the mixer input to 50 Ω. The system sensitivity for 12 dB SINAD is 0.67 μV at the input from a 50 Ω source in this application, which is as good as most inexpensive weather cubes and the dual conversion design allows for excellent image protection to be provided.

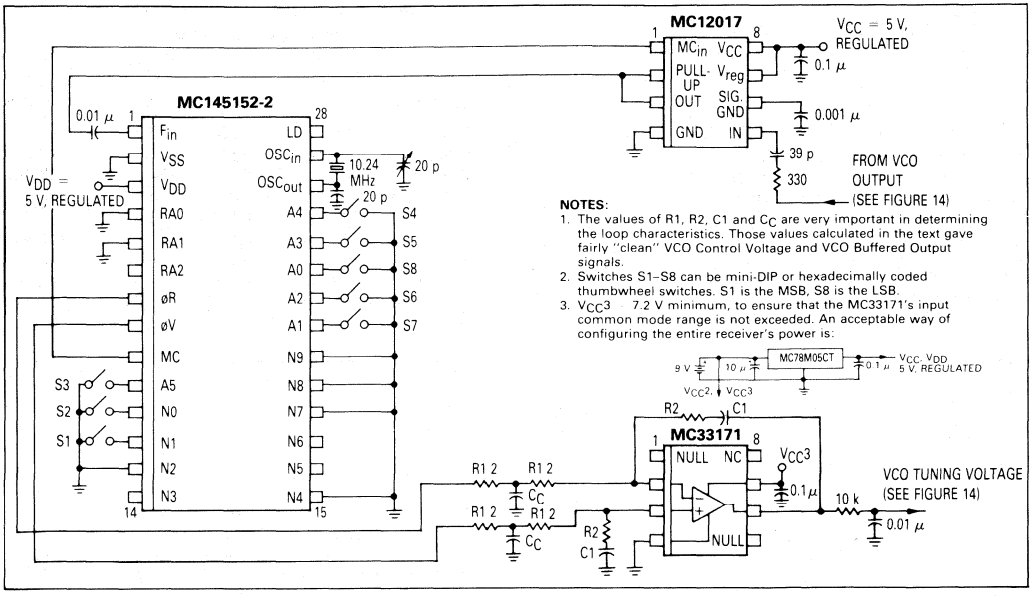


Figure 15. 256 Channel VCO Control Using PLL Frequency Synthesizer

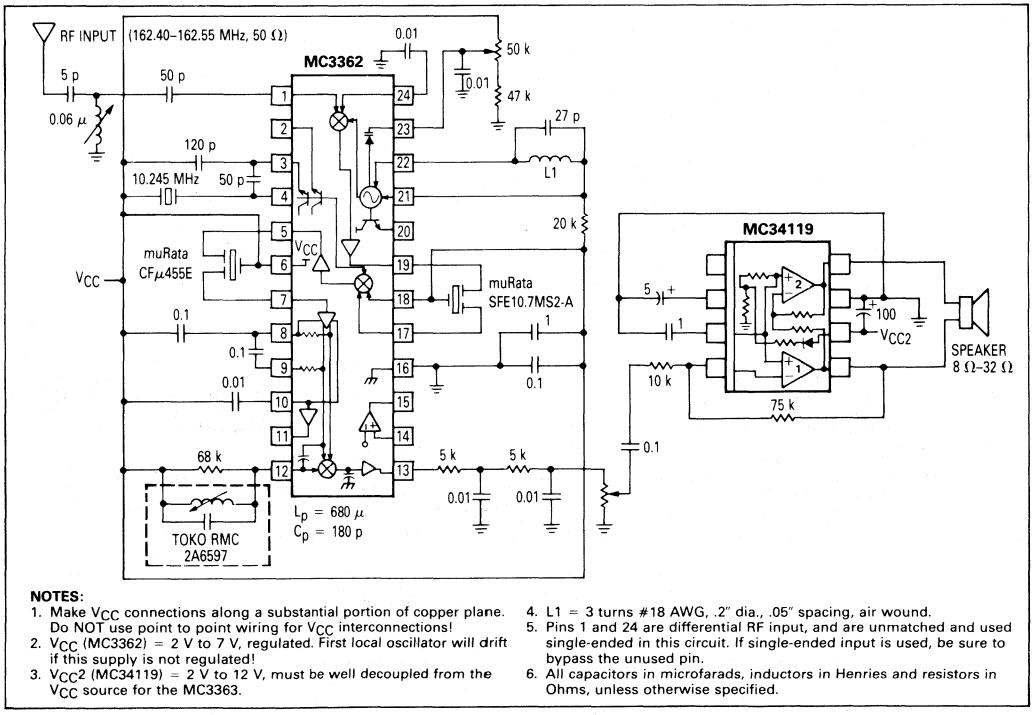


Figure 16. MC3362 Application as a Tunable Weather Band Receiver

The first local oscillator is free-running in this application and the receiver is manually tunable over a range of ±1 MHz. The oscillator's frequency and tuning range are determined by the external tank circuit values chosen. Keep in mind that the internal varactor diodes add 10–25 pF of capacity across the tank pins, depending on the varactor control voltage applied.

This circuit is easily built to vefify receiver characteristics on the lab bench, but as shown is not suited for mass production. The local oscillator temperature stability is not nearly adequate in this free-running configuration and microphonic pickup is difficult to avoid. Before a narrowband receiver is production-ready, the first local oscillator must be stable to within approximately ±100 Hz. The "First Mixer and Oscillator" section provides notes on driving the first mixer using an external oscillator signal above 50 MHz. The MC2833 FM transmitter IC might serve as the local oscillator source up to 200 MHz.

SUMMARY

The high degree of integration and MOSAIC process used in the MC3362/3 receivers give the radio designer new levels of space and power economy, while providing high performance and considerable design flexibility. The receivers shown and alternate configurations discussed should interest designers of cordless phones, VHF two way radios, remote control receivers, wireless data links and home security systems.

APPENDIX — DIRECTORY OF COMPONENT MANUFACTURERS

muRata-Erie 2200 Lake Park Drive Smyrna, GA 30080	(404) 436-1300 ceramic filters
Toko America Inc. 1250 Feehanville Drive Mount Prospect, IL 60056 **Distributor — Digikey** **Distributor — Inductor Supply**	(708) 297-0070 quadrature coils coils, transformers (800) 344-4539 (800) 854-1881 (800) 472-8421 (California)
Coilcraft 1102 Silver Lake Road Cary, IL 60013	(708) 639-6400 coils
California Crystal Laboratories	(800) 333-9825 crystals
Fox Electronics	(813) 693-0099 crystals
International Crystals	(405) 236-3741 crystals
Standard Crystal Corporation	(818) 443-2121 crystals

Note: Design-in kits including printed circuit boards are available from analog marketing. Call (602) 897-3820

Motorola does not endorse the vendors listed.
This is a partial vendor list and no liability is assumed
for omissions or errors in address, product line or other information.

AR254 #1

Analyze, don't estimate, phase-lock-loop

performance of type-2, third-order systems. You can do the job with a programmable-calculator in 48 steps, or less.

Phase-lock loops certainly have many uses, especially in frequency synthesizers, but exact mathematical calculation of their transfer functions is difficult. This is particularly true for type-2, third-order systems (Fig. 1), which don't produce steady-state phase errors for step-position or velocity signal inputs. However, a small programmable calculator, the HP-25, easily —and exactly—determines the complete loop transfer function in 48 steps. In addition, the program data reveals the noise reduction you can expect for the loop's voltage-controlled oscillator (VCO), as well as the loop's stability.

Most other design approaches must resort to second-order loop approximations to simplify calculations; a more exact method manually would take too long.

Unlike a type-1 loop, a type-2 loop has two *true* integrators within the loop—a VCO and an integrator/filter after the phase detector. Replacing the integrator/filter with a passive-RC, low-pass filter results in the more common type-1 response, which doesn't have the phase coherence for step and velocity inputs between the two signal inputs to the phase comparator that the type-2 has.

Moreover, a third-order loop—the order is usually determined by the transfer function of the integrator/filter ($F_{(s)}$)—can reduce VCO noise substantially, without increasing reference-frequency sidebands in the output signal. These sidebands hamper simpler loop-circuit performance.

The transfer function of a generalized phase-lock loop can be represented as follows (Fig. 2):

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{G_{(s)}}{1 + G_{(s)}H_{(s)}} \quad (1)$$

where, from Fig. 1

$$G_{(s)} = (K_p)(F_{(s)})(K_v/s) \quad (2)$$

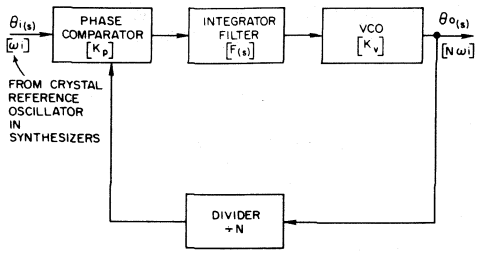
and

$$H_{(s)} = 1/N. \quad (3)$$

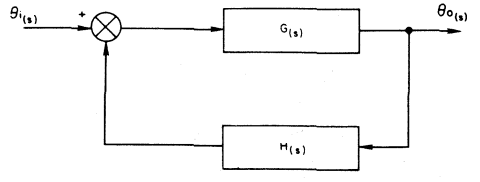
The phase comparator transfer function is K_p and N is a digital counter/divider factor.

A typical integrator/filter built around an op amp (Fig. 3) has a transfer function determined by the amplifier-circuit's closed-loop gain,

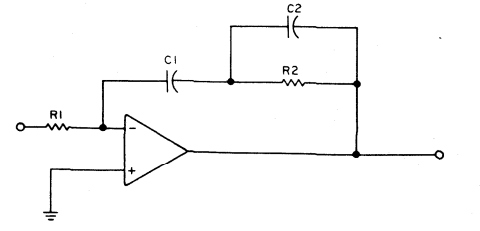
$$A_{CL} = -\frac{Z_f}{Z_1},$$



1. **A type-2 phase-lock loop** has two true integrators—the integrator/filter (F_s) and the VCO (K_v). Replacing the integrator/filter with a passive-RC network converts the circuit to a type-1 system.



2. **The phase-lock loop's generalized open-loop transfer function,** $G_{(s)}$ $H_{(s)}$, has a third-order denominator—from which the circuit's name is derived.



3. **An integrator/filter circuit** can be built with a wideband op amp and RC feedback network.

Andrzej B. Przedpelski, Vice President of Development, A.R.F. Products Inc., 2559 75th St., Boulder, CO 80301.

Table 1. Third order type-2 PLL

Display Line	Display Code	Key Entry	Remarks	Registers
00				R_0
01	1573	(g)π		
02	61	x		
03	02	2		R_1 T_1
04	61	x		
05	2307	STO 7		
06	2403	RCL 3		R_2 T_2
07	61	x		
08	01	1		
09	1509	(g)→P		R_3 T_3
10	2304	STO 4		
11	22	R↓		
12	2402	RCL 2		R_4
13	2407	RCL 7		
14	61	x		
15	32	CHS		R_5 $\frac{K_p K_v}{N}$
16	01	1		
17	32	CHS		
18	1509	(g)→P		R_6
19	2404	RCL 4		
20	71	÷		
21	2405	RCL 5		R_7
22	61	x		
23	2401	RCL 1		
24	71	÷		
25	2407	RCL 7		
26	1502	(g) x^2		
27	71	÷		
28	2304	STO 4		
29	1408	(f) log		
30	02	2		
31	00	0	$\|G_{j\omega}H_{j\omega}\|$	
32	61	x		
33	74	R/S		
34	22	R↓		
35	21	x≷y		
36	41	—	$\angle\theta$	
37	74	R/S		
38	2404	RCL 4		
39	1409	(f)→R		
40	01	1		
41	51	+		
42	1509	(g)→P		
43	1522	(g)1/x		
44	1408	(f) log		
45	02	2		
46	00	0	e/en	
47	61	x		
48	1300	GTO 00		
49				

where $Z_1 = R_1$ (4)

Z_f = impedance of feedback network

The transform of the feedback network is

$$Z_f(s) = \frac{s(C_1+C_2)+\frac{1}{R_2}}{sC_1(sC_2+\frac{1}{R_2})}, \quad (5)$$

and the integrator/filter transfer function is then

$$F_{(s)} = -\frac{s(C_1+C_2)+\frac{1}{R_2}}{C_1R_1(sC_2+\frac{1}{R_2})}, \quad (6)$$

Multiply Eq. 6 by R_2/R_2, then

$$F_{(s)} = -\frac{s(C_1R_2+C_2R_2)+1}{sC_1R_1(sC_2R_2+1)} \quad (7)$$

or

$$F_{(s)} = -\frac{sT_2+1}{sT_1(sT_3+1)}, \quad (8)$$

where $T_1 = R_1C_1$

$T_2 = R_2(C_1 + C_2)$

$T_3 = R_2C_2$

The open-loop transfer function of Fig. 2 is $G_{(s)}H_{(s)}$; therefore, from Eqs. 2, 3 and 8

$$G_{(s)}H_{(s)} = \frac{s(T_2)(K_vK_p) + K_vK_p}{s^3NT_1T_3 + s^2NT_1} \quad (9)$$

Note the third-order denominator, from which the circuit's name—third-order-loop—is derived. Note also the deletion of the minus sign: the circuit configuration (a phase inverter) provides the negative feedback. Both K_p and K_v are positive.

If you substitute jω for s in Eq. 9, you can get the equation for plotting the magnitude and phase of the circuit's open-loop gain as a function of frequency:

$$G_{(j\omega)}H_{(j\omega)} = -\frac{j\omega(T_2)(K_vK_p) + K_vK_p}{j\omega^3NT_1T_3 + \omega^2NT_1}. \quad (10)$$

Step	Instructions	Input Data/ Units	Keys			Output Data/ Units
1	Enter program					
2	Store T_1	R_1	ENTER			
		C_1	X	STO	1	
	T_2	C_1	ENTER			
		C_2	+			
		R_2	X	STO	2	
	T_3	R_2	ENTER			
		C_2	X	STO	3	
	(Kp Kv)/N	K_p	ENTER			
		K_v	X			
		N	=	STO	5	
3	Calculate	F	(f)	PRGM	R/S	$G_{j\omega}H_{j\omega}$ $\angle\theta$ (e/en)
			R/S			
			R/S			
4	Repeat step 3 for other values of frequency, F					

Table 2. Calculated loop response

Frequency Hz	Open-loop response dB	Open-loop response ∠θ	Loop response to VCO noise dB
100	116.01	−179.94	−116.01
1000	76.01	−179.44	−76.01
10,000	36.06	−174.44	−35.92
94,650	0*	−139.85	3.27
100,000	−0.71	−138.58	3.30**
1,000,000	−26.25	−139.59	0.32
10,000,000	−63.21	−174.68	0.01

*Unity-gain point **Maximum overshoot

A servo-loop damping factor that appears in lower-order loops is not defined in third-order loops. Instead you determine stability by the phase margin between −180° and the phase at a frequency where the gain is unity in the open-loop gain function, $G_{j\omega}H_{j\omega}$. The larger the phase margin, the more stable the system. A phase margin of about 45° produces an adequately damped loop. More than 45° means greater stability and, of course, the system may oscillate when the margin approaches zero.

Feedback also reduces noise

Not only does feedback determine the system's stability, but it also delineates its noise-output characteristics. When running free, the VCO is considerably *more "noisy" than is the circuit's reference crystal* oscillator. But the circuit's feedback loop substantially reduces the VCO's output-noise spectrum, especially, at low frequencies. This particular reduction is fortunate, because the VCO's noise output has 1/f characteristics: high-frequency noise tends to fall off without outside help, but the low frequency needs the help.

An approximate expression for the loop's output phase noise is

$$\sqrt{[(|e/e_n|)(e_v)]^2 + [(N)(e_x)]^2}, \qquad (11)$$

where e_x = crystal-oscillator noise.
e_v = VCO noise.
(e/e_n) = loop's response to VCO noise.

And the loop's response to the VCO noise is

$$(e/e_n) = \frac{1}{1 + G_{(s)}H_{(s)}}. \qquad (12)$$

Although $G_{(s)}H_{(s)}$ determined from Eq. 9 is complex, only the magnitude of (e/e_n) from Eq. 12 is used in Eq. 11. Note: The greater the open-loop transfer function, $G_{(s)}H_{(s)}$, the smaller the (e/e_n), and the lower the loop's output noise. However, note also that the reference crystal oscillator's noise contribution is multiplied by the divider constant, N, though, hopefully, the crystal-oscillator noise is low.

In addition, you can get a check on the system's stability by plotting the loop's response to VCO noise (e/e_n), obtained from Eq. 12, versus frequency. You'll find that the curve has a high-pass response with a 12-dB/octave slope. For best stability, any overshoot at the cutoff frequency should be less than 6 dB. Of course, lower overshoot represents higher stability.

Clearly, the loop's mathematical analysis depends mainly upon calculation of $G_{(j\omega)}H_{(j\omega)}$ in Eq. 10.

Now comes the program

To make the calculator program simpler, rewrite Eq. 10 as follows:

$$G_{(j\omega)}H_{(j\omega)} = \frac{K_vK_p}{NT_1\omega^2}\left[\frac{-j\omega T_2 - 1}{j\omega T_3 + 1}\right] \qquad (13)$$

Table 1 contains the program that solves Eq. 13. It provides both the magnitude and phase angle, ∠θ, of the open-loop response, $G_{(j\omega)}H_{(j\omega)}$, given T_1, T_2, T_3, K_pK_v/N and frequency, $f(\omega=2\pi f)$. The open-loop response magnitude is given in dB and its phase in degrees. Also, the magnitude of the loop's VCO noise response (Eq. 12) is given in dB. If answers in dB aren't required, however, seven steps can be eliminated.

To see how the program works, consider a 960-MHz transmitter recently proposed for a Navy application. It calls for a phase-lock loop with the following characteristics to generate the 960 MHz:

$N = 64$
$R_1 = 10{,}000\ \Omega$
$C_1 = 4700 \times 10^{-12}$ F
$R_2 = 330\ \Omega$
$C_2 = 470 \times 10^{-12}$ F
$K_p = 0.25$ V/rad
$K_v = 3 \times 10^9$ (rad/s)/V

The stable crystal-oscillator reference frequency used is 15 MHz. The frequency divider and phase comparator are built with ECL logic. From the circuit component values and transfer constants we obtain:

$T_1 = 4.7 \times 10^{-5}$ s
$T_2 = 1.706 \times 10^{-6}$ s
$T_3 = 1.551 \times 10^{-7}$ s
$(K_vK_p)/N = 11.72 \times 10^6$/s

The calculator program provided the results in Table 2. Note that the phase margin at unity gain corresponding to 94,650 Hz is 40.15°; thus the loop is fairly stable. Further, the loop's response to VCO noise shows a maximum overshoot of 3.30 dB at 100,000 Hz, which confirms the loop's stability (less than 6-dB overshoot). If the phase margin is too small or you want overdamped loop operation, the program allows you to check the effects of parameter changes and get the performance you want, quickly. However, keep all additional circuit poles above the area of interest, since they reduce phase margin and stability. In addition, don't ignore the effects of stray capacitances. And use a high-gain op amp with a wide frequency response and a VCO with a wide modulation bandwidth. ■■

Bibliography

Dorf, R. C., *Modern Control Systems*, Addison-Wesley Publishing Co., Reading, MA, 1967.

Gardner, F. M., *Phaselock Techniques*, John Wiley & Sons, Inc., NY, 1977.

Phase-Locked Loop Data Book, Motorola Semiconductor Products, Inc., Second Edition, August, 1973.

Stout, D. F., and Kaufman, M., *Handbook of Operational Circuit Design*, McGraw-Hill Book Co., NY, 1976.

AR254 #2

Optimize phase-lock loops to meet your needs—or determine why you can't

The time constants of a PLL's integrator/filter are the keys to controlling a loop's performance. In the integrator/filter, you can trade off circuit parameters most easily to meet your needs. The other loop components (Fig. 1) have simple, real-valued transfer functions (K_v, K_p, N) that can't be changed as easily. But the integrator/filter's transfer function (F_s), detailed in Fig. 1c is the source of the high-order complex function in the following equation for open-loop gain:

$$G(j\omega)\,H(j\omega) = \frac{K_v K_p}{NT_1\omega^2}\left[\frac{-j\omega T_2 - 1}{j\omega T_3 + 1}\right], \qquad (1)$$

where

T_1, T_2, T_3 = time constants defined in Fig. 1c, seconds

K_p = phase-detector gain constant, volts/radian

K_v = voltage-controlled-oscillator (VCO) sensitivity, radians/second/volt

N = frequency devisor

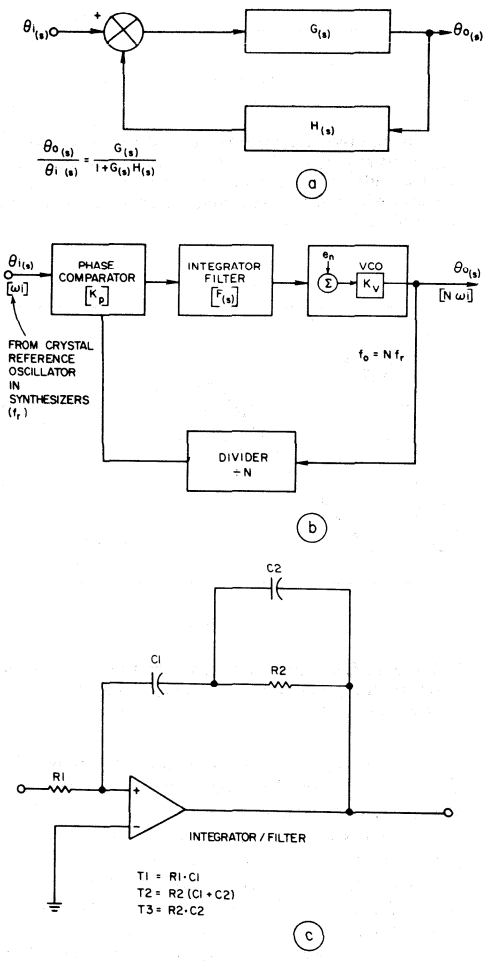
$\omega = (2\pi f)$ frequency, radians

Usually, K_p, K_v and N are given, but you can choose T_1, T_2 and T_3 to give you the loop performance you want. Generally, of course, you want the loop to be stable, to attenuate the reference frequency and to reduce VCO noise. But stability, being an absolute necessity, gets priority. The other two requirements, unfortunately, are inversely dependent and must be traded off against each other.

A damping factor to control stability as in simpler second-order loops can't be readily defined in the third-order loop of Fig. 1. Instead, the phase margin

In ED No. 10, May 10, 1978, p. 120, A. B. Przedpelski advised: "Analyze, don't estimate, phase-lock-loop performance." He showed how to calculate the performance of a given type-2, third-order PLL system with a 48-step program for an HP-25 programmable calculator. This article will show you how to optimize such a PLL to your requirements. But you will discover that you may not be able to get all requirements simultaneously. Compromises may be necessary.

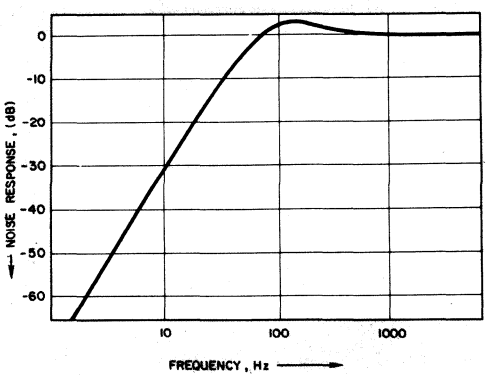
Andrzej B. Przedpelski, Vice President of Development, A.R.F. Products Inc., 2559 75th St., Boulder, CO 80301.



1. **A phase-lock loop** (a) with two integrators (b) is classified type 2. And the order—third, in this case—is established by the characteristics of the integrator/filter (c). Time constants T_1, T_2 and T_3 determine the integrator/filter's detailed performance.

Display Line	Display Code	Key Entry	Remarks	Registers
00				R_0
01	2407	RCL 7		
02	1406	(f) tan		
03	32	CHS		R_1
04	2407	RCL 7		
05	1405	(f) cos		
06	1522	(g) 1/x		R_2
07	51	+		
08	2406	RCL 6		
09	1573	(g) π		R_3
10	61	x		
11	02	2		
12	61	x		R_4
13	2304	STO 4		
14	71	÷		
15	2303	STO 3	3	R_5 $\frac{KpKv}{N}$
16	74	R/S		
17	2404	RCL 4		
18	1502	(g) x^2		R_6 f_o
19	61	x		
20	1522	(g) 1/x		
21	2302	STO 2	T_2	R_7 ϕ
22	74	R/S		
23	2404	RCL 4		
24	61	x		
25	01	1		
26	1509	(g)→P		
27	2403	RCL 3		
28	2404	RCL 4		
29	61	x		
30	01	1		
31	1509	(g)→P		
32	21	x≷y		
33	22	R↓		
34	71	÷		
35	2404	RCL 4		
36	1502	(g) x^2		
37	71	÷		
38	2405	RCL 5		
39	61	x		
40	2301	STO 1	T_1	
41	1300	GTO 00		

Step	Instructions	Input Data/ Units	Keys			Output Data/Units
1	Enter program					
2	Store	f_o	STO	6		
		ϕ	STO	7		
		K_p	ENTER			
		K_v	X			
		N	:	STO	5	
3	Calculate		(f)	PRGM	R/S	T_3
			R/S			T_2
			R/S			T_1
3	Recall (if desired)		RCL	1		T_1
			RCL	2		T_2
			RCL	3		T_3
			RCL	4		o



5. **The noise-response calculation** corresponding to Fig. 4 shows that VCO noise is attenuated below about 70 Hz.

article and plotted in Figs. 4 and 5. The curves confirm that the design is stable with a maximum phase margin of 45° at a frequency where the open-loop gain is about unity. And the VCO noise-reduction curve shows a moderate 3.2-dB overshoot with noise frequencies below about 70 Hz in the attenuation region.

Still, adjustments may be desired. For instance, if you want more reference-frequency (f_r) attenuation, the G (jω) H (jω) curve can be shifted to the left. Move f_o one decade (to about 10 Hz) and you'll increase the f_r attenuation by 40 dB. Or, if noise frequencies above 70 Hz are bothersome, you can shift the G (jω) H (jω) curve to the right by increasing f_o.

If you still aren't satisfied, you can change the phase margin. Reduce the margin and you improve both f_r and VCO-noise attenuation—but then you lose some stability.■■

Bibliography

Dorf, C., *Modern Control Systems*, Addison-Wesley Publishing Co., Reading, MA, 1967.

Gardner, F.M., *Phaselock Techniques*, John Wiley & Sons, Inc., New York, NY, 1966.

Phase-Locked-Loop Systems Data Book, Motorola Semiconductor Products, Inc., Second Edition, August, 1973.

Przedpelski, A.B., "Analyze, Don't Estimate, Phase-Lock-Loop Performance of Type-2, Third-Order Systems," *Electronic Design*, May, 1978.

Stout, D.F., and Kaufman, M., *Handbook of Operational Circuit Design*, McGraw-Hill Book Company, New York, NY, 1976.

AR254 #3

Suppress phase-lock-loop sidebands without introducing instability

Phase-lock loops: Part Three

The first two parts of this series showed how to analyze and then optimize type-2, third-order PLL systems and provided simple calculator programs for an HP-25 to do the otherwise tedious computations.[1,2] *This article takes you a step further and shows how to suppress sidebands, especially undesired when the PLL is used in frequency-synthesis systems.*

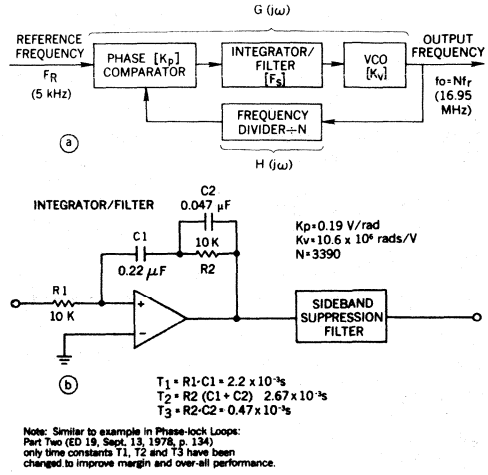
Frequency synthesis, a major application of the phase-lock loop (PLL), always involves PLL-performance compromise: keeping loop bandwidth as wide as possible to reduce acquisition time and voltage-controlled oscillator noise, and at the same time suppressing reference-frequency sidebands that can pass through wide bandwidths (Fig. 1).

Fortunately, the reference frequency is considerably above the required loop bandwidth in most cases, which alleviates the sideband problem to some extent. But for heavy suppression of undesired sidebands, extra filtering is necessary. However, it must be done carefully so as not to introduce loop instability. Three filtering circuits, none of which reduce bandwidth or VCO-noise attenuation can help solve the problem. In fact, an active LP-filtering technique, the most versatile and efficient of the three, is programmed on an HP-25 to speed the design.

All methods assume that the PLL, a type-2 third-order loop,[1] meets all requirements[2] except adequate reference-frequency sideband suppression. The three approaches include RC, active-notch and active-LP filtering. The PPL's phase margin serves as a measure of loop stability, since the damping-factor concept isn't applicable to third-order loops:[2] phase margins between 30° and 45° are minimum criteria for stable operation. And the filter's action in reducing the feedforward gain, G(jω), at the sideband frequencies is the criterion for the suppression effectiveness.

Since H(jω) is equal to 1/N, a constant, then the open-loop gain, G(jω)H(jω) in Eq. 1, can be used as a measure of this sideband-suppression effectiveness:

Andrzej B. Przedpelski, Vice President of Development, A.R.F. Products Inc., 2559 75th St., Boulder, CO 80301.



1. **A phase-lock-loop frequency synthesizer** (a) generates 16.95 MHz from a crystal-oscillator reference frequency of 5 kHz. To help suppress sidebands, a sideband-suppression filter is added in tandem with the output of the loop's original integrator/filter circuit (b).

Table 1. Filter suppression/phase margin tradeoffs

Circuit	Phase margin	Phase margin deterioration	First-sideband reduction	Second-sideband reduction
Original	44°	—	—	—
RC low-pass RC = 3 x 10^{-4}	32	12°	20 dB	26 dB
Notch filter Q = 10	44	0	∞*	0
Q = 1	43	1	∞*	1.5
Q = 0.1	31	13	∞*	16.5
Second-order active d = 0.707	34	10	28	40
d = 0.1	42	2	28	40

*Theoretical—actual value about 40 dB.

$$G(j\omega)H(j\omega) = \frac{K_v K_p}{NT_1\omega^2}\left[\frac{-j\omega T_2 - 1}{j\omega T_3 + 1}\right], \quad (1)$$

K_p = gain constant of the phase detector,
K_v = VCO sensitivity,

Table 2. Third-order PLL with two-pole low-pass filter

Display Line	Display Code	Key Entry	Remarks	Registers
00				R_0 ω_o
01	2400	RCL 0		
02	1502	(g) x^2		
03	2407	RCL 7		R_1 T_1
04	1502	(g) x^2		
05	41	—		
06	2304	STO 4		R_2 T_2
07	2403	RCL 3		
08	61	x		
09	2406	RCL 6		R_3 T_3
10	2400	RCL 0		
11	61	x		
12	51	+		R_4
13	2407	RCL 7		
14	61	x		R_5 $\frac{Kv\ Kp}{N}$
15	2404	RCL 4		
16	2406	RCL 6		
17	2403	RCL 3		
18	61	x		R_6 2d
19	2400	RCL 0		
20	61	x		
21	2407	RCL 7		R_7 ω
22	1502	(g) x^2		
23	61	x		
24	41	—		
25	32	CHS		
26	1509	(g)→P		
27	21	x⇄y		
28	2407	RCL 7		
29	2402	RCL 2		
30	61	x		
31	32	CHS		
32	01	1		
33	32	CHS		
34	1509	(g)→P		
35	22	R↓		
36	51	+	∠ Phase margin	
37	74	R/S		
38	22	R↓		
39	71	÷		
40	2405	RCL 5		
41	61	x		
42	2401	RCL 1		
43	71	÷		
44	2407	RCL 7		
45	1502	(g) x^2		
46	71	÷		
47	2400	RCL 0		
48	1502	(g) x^2		
49	61	x	|G S H S|	

Step	Instructions	Input Data/ Units	Keys			Output Data/ Units
1	Enter program					
2	Store	ω_o	STO	0		
		T_1	STO	1		
		T_2	STO	2		
		T_3	STO	3		
		Kv	ENTER			
		Kp	x			
		N	÷	STO	5	
		d	ENTER	2	x	
			STO	6		
3	Enter	ω	STO	7		
4	Calculate		(f)	PRGM	R/S	∠Phase margin |G(s) H(s)|
			R/S			
5	Repeat steps 3 and 4 for other values of frequency, ω					

N = counter divide ratio,
T_1, T_2, T_3= integrator/filter time constants.

Simple but limited

The simplest approach adds in series with the Integrator/Filter an RC low-pass section (Fig. 2a), whose cutoff frequency is larger than the upper end of the loop's bandwidth. For illustration, let the value of RC be 3×10^{-4} s for the frequency-synthesizer example outlined in Fig. 1. (A larger value would reduce sidebands more, but would also decrease the phase margin too much.) With a value of 3×10^{-4} s, the phase margin remains within a "safe" 30°-to-45°.

The open-loop transfer function then becomes:

$$G(j\omega)H(j\omega) = \frac{K_v K_p}{NT_1\omega^2}\left[\frac{-j\omega T_2 - 1}{j\omega(T_3+T_4)+1+\omega^2 T_3 T_4}\right], \quad (2)$$

where T_4 is the additional RC time constant.

Solving Eq. 1 at frequencies of 5 and 10 kHz shows that the first sideband (at 5 kHz) is reduced a respectable 20 dB and the second sideband (at 10 kHz) even more to 26 dB. But the phase margin also is reduced to a marginal 32° (Table 1).

However, an active RC notch filter[3] (Fig. 2) gives much more attenuation at the first sideband (5 kHz) and is more flexible in some applications. Its gain is

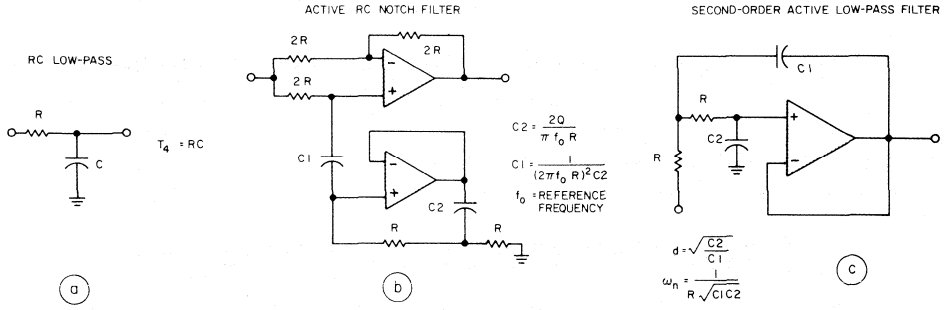
$$A(j\omega) = \frac{1}{j\omega\left[\frac{\omega_o}{Q(\omega^2-\omega_o^2)}\right]+1}, \quad (3)$$

where ω_o= the notch frequency ($2\pi f_o$),
Q= the circuit Q.

The open-loop transfer function, the product of Eqs. 1 and 3, is

$$G(j\omega)H(j\omega) = \frac{K_v K_p}{NT_1\omega^2} \times \left[\frac{-j\omega T_2 - 1}{j\omega\left(T_3 - \frac{\omega_o}{Q(\omega^2-\omega_o^2)}\right)+\omega^2 T_3\left(\frac{\omega_o}{Q(\omega^2-\omega_o^2)}\right)+1}\right], \quad (4)$$

Although the notch frequency ω_o must be fixed at the reference frequency, the value of Q can vary. Theoretically, the reference frequency receives infinite attenuation. Actually, only about 40 dB can be realized, even under ideal conditions. Evaluation of Eq. 4 for Q's of 10, 1 and 0.1 shows that high Q values produce negligible phase-margin deterioration, but



2. **Many filter configurations can be used** to suppress sidebands. The simplest is a low-pass RC circuit (a). Somewhat more flexible is an active RC notch filter (b). But of all filters, a second-order active low-pass filter (c) is most versatile, since two of its parameters are independently adjustable.

attenuation of the second harmonic of the reference frequency is small or zero (Table 1). At a Q of 0.1, however, the second harmonic is reduced 16.5 dB, but then the phase margin suffers.

Most versatile, however, is a second-order, active, low-pass filter with variable damping (Fig. 2c). Its gain (with "s" functions of its more familiar form replaced by $j\omega$) is:[3]

$$A(j\omega) = \frac{\omega_n^2}{-\omega^2+2dj\omega\omega_n+\omega_n^2}, \qquad (5)$$

where ω_n= the filter's natural pole frequency,
d= the filter's damping factor.

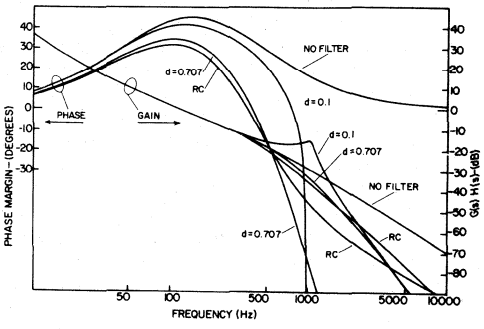
This time, multiplying Eqs. 1 and 5, the over-all open-loop transfer function becomes

$$G(j\omega)H(j\omega) = \frac{\omega_n^2 K_v K_p}{NT_1\omega^2} \times \left[\frac{-j\omega T_2-1}{j\omega[2d\omega_n+T_3(\omega_n^2-\omega)]+[\omega_n^2-\omega^2-2dT_3\omega_n\omega^2]}\right] \qquad (6)$$

If ω_n is chosen to be 6283 ($2\pi \times 1000$) at damping factors of 0.707 (Butterworth response) and 0.1 (16-dB peak Chebyshev), Eq. 6 gives the same sideband attenuation for both damping factors, but the high-ripple Chebyshev deteriorates the phase margin least (Table 1 and Fig. 3).

Since both the pole frequency and the damping factor can be varied in Eq. 5, the circuit it represents is most versatile. Therefore, Eq. 6 is programmed for easy solution on an HP-25 (Table 2) in 49 steps. However, for easier stability evaluation, the program solves directly for the phase margin—the difference between 180° and the open-loop transfer-function angle—rather than the phase angle itself.

Clearly, the simple RC circuit is least efficient. It gives the least sideband attenuation and the largest phase-margin deterioration. The notch filter, although theoretically capable of very high attenuation of the first sidebands only with very small phase-margin deterioration, generally requires component tolerances too critical for other than some special applications. The more complex, active, second-order low-pass filter, however, can be tailored to most applications—illustrating an often observed design phenomenon: the more complex the circuit the better the performance. Of course, then, more complex filter circuits than those used in the examples may offer even better solutions to sideband reduction. ■■



3. **A plot of open-loop gain and phase response** of the system in Fig. 1 compares sideband suppression at 5 and 10 kHz without an extra filter with that of a simple RC and an active, second-order filter.

References

1. Przedpelski, A.B., "Analyze, Don't Estimate, Phase-lock-loop Performance of Type-2, Third-order Systems," *Electronic Design*, May 10, 1978, p. 120.

2. Przedpelski, A.B., "Optimize Phase-lock Loops to Meet Your Needs," *Electronic Design*, Sept. 13, 1978, p. 134.

3. Stout, D.F., and Kaufman, M., *Operational Amplifier Circuit Design*, McGraw-Hill, NY, 1976.

AR254 #4

Calculate the noise spectral density and short-term frequency stability in a PLL with a programmable calculator, and vary the parameters to trade off the noise/functional performance requirements.

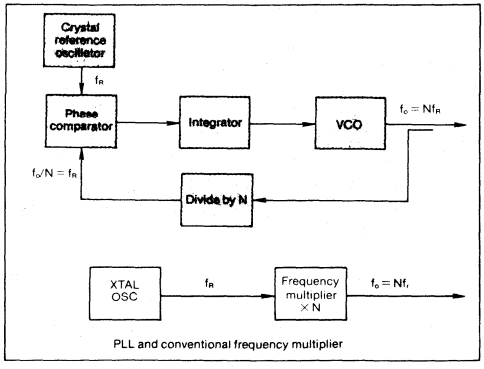
Programmable calculator computes PLL noise, stability

This article is the fourth by the author on phase-locked loops, starting with "Analyze, Don't Estimate, Phase-Lock-Loop Performance" (May 10, 1978, p. 120); then "Optimize Phase-Lock-Loops to Meet Your Needs" (Sept. 13, 1978, p. 134); followed by "Suppress Phase-Lock-Loop Sidebands without Introducing Instability" (Sept. 13, 1979, p. 142).

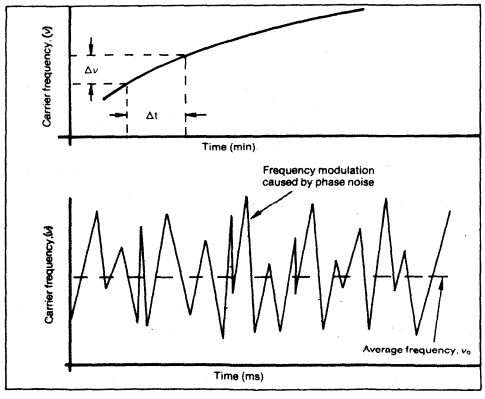
The circuit constants of a phase-lock loop can be optimized not only for performance requirements (acquisition time, sideband levels, step response, and stability, among others), but also for noise output and the resulting short-term (or "instantaneous") frequency stability. Because most other frequency-generation methods lack this versatile performance, and noise and stability control, phase-lock loops (PLLs) are preferable for frequency synthesis. Moreover, a programmable HP-19C (or 21C) calculator with the proper program makes the design tradeoffs between noise effects and functional performance requirements relatively easy to determine.

A properly designed frequency synthesizer derived from a PLL (Fig. 1, top) will offer a high degree of flexibility and long-term frequency stability. In a PLL, the frequency of the stable reference oscillator (say, a quartz-crystal circuit) can be multiplied by a precisely controlled factor over a very wide range. Although the PLL may seem more complicated than the conventional so-called frequency-multiplier circuit (Fig. 1, bottom), in practice, the PLL is more efficient, more compact, and considerably wider in bandwidth. All the advantages increase as the multiplication factor increases.

In most PLL frequency synthesizers, the primary concern is the functional performance—a problem that has been treated extensively.[1] Even the theoretical aspects of phase noise in low-noise signal sources have been extensively covered.[2,3,4] However,



1. Although the PLL frequency multiplier (top) looks more complex than the conventional multiplier (bottom), it is in fact more compact and more flexible, and can handle a much wider frequency range.



2. Short-term frequency stability can be far worse (bottom) than the long-term average of a PLL system (top).

Andrzej B. Przedpelski, Vice President of Development
A.R.F. Products, Inc.
2559 75 St., Boulder, CO 80301

PLL noise and stability

specific methods for calculating the noise and short-term frequency stability and details of the tradeoffs are generally not available, except for some recent work by the National Bureau of Standards on low-noise signal sources.[5,6,7]

Short-term (or "instantaneously" sampled) frequency stability, in the millisecond range, is particularly important for accuracy in position-finding applications, as in LORAN navigation and various radar and sonar Doppler systems. Even though frequency drift over a short time generally is less than the average long-term frequency drift, instantaneously measured samples show much wider variations in the frequency swings caused by phase noise in the signal source (Fig. 2).

The overall phase-noise, or spectral-density output, $S_{\phi(\omega)0}$, of a PLL[8] is found by

$$S_{\phi(\omega)0} = S_{\phi(\omega)VCO}\left|\frac{1}{1+G(\omega)H(\omega)}\right|^2 + S_{\phi(\omega)REF}\left|\frac{G(\omega)}{1+G(\omega)H(\omega)}\right|^2,$$

where $S_{\phi(\omega)VCO}$ is the open-loop spectral density of phase fluctuations in the PLL's voltage-controlled oscillator (VCO) and $S_{\phi(\omega)REF}$ is the equivalent spectral density of fluctuations in the reference oscillator. These phase fluctuations are measured in rad²/Hz, but generally plotted in dBc, which is 10 $\log_{10}$ $S_{\phi(\omega)}$. More commonly, however, vendor-supplied phase-noise data, designated $\mathcal{L}(\omega)$, and also measured in dBc, are for single-sideband noise. (The dBc designation is defined as 10 $\log_{10}$ of the ratio between the output from a spectrum analyzer with a 1-Hz bandwidth and the signal's carrier level.) Accordingly,

$$\mathcal{L}(\omega) = 10 \log_{10}(\tfrac{1}{2})S_{\phi(\omega)} \text{ (per rad}^2\text{)},$$

assuming that

$$\mathcal{L}(-\omega) = \mathcal{L}(\omega).$$

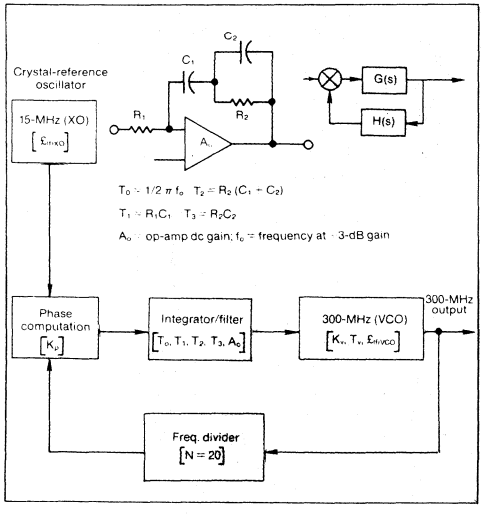
Therefore, to convert $\mathcal{L}(\omega)$ data to "straight" $S_{\phi(\omega)}$ data, add 3 dB to the $\mathcal{L}(\omega)$ data and take the antilog.

An HP-19C program (see "Noise in a 5th-order PLL") calculates this single-sideband noise, where $G(\omega)H(\omega)$ is the open-loop gain of the PLL.[1] The feedback path, $H(\omega)$, is simply 1/N; and $G(\omega)$ equals

$$\frac{(K_pK_v/\omega T_1)(jwT_2 + 1)}{j\left[\omega^2(\omega^2 \frac{T_o}{A_o} T_vT_3 - T_3 - T_v) + \frac{1}{A_oT_1}\right] + \omega(\omega^2T_vT_3 - 1)}$$

Optimized for functional performance, the following circuit constants are used for a typical PLL (Fig. 3):

$A_o = 320{,}000$
$T_o = 7.96 \times 10^{-4}$ s
$T_v = 1.59 \times 10^{-7}$ s
$T_1 = 2.408 \times 10^{-5}$ s
$T_2 = 2.491 \times 10^{-6}$ s
$T_3 = 4.700 \times 10^{-7}$ s
$K_p = 314 \times 10^6$ V/rad
$K_v = 0.16$ rad/V
$N = 20.$



3. For a fifth-order PLL, four of the time constants are determined by the integrator/filter circuit, and the fifth is determined by the VCO.

The single-sideband phase noise, when calculated by the program for a range of so-called Fourier frequencies (offsets from a carrier, $f = \omega/2\pi$), can be plotted as in Fig. 4 (dotted line). Although this output phase noise can be reduced by varying circuit constants to increase the loop's bandwidth, proceed with caution, because other desirable operating characteristics (such as circuit stability or speed of response) could be compromised. The program, however, offers an easy way to determine how systematic changes in the parameters affect noise.

Oscillator noise should be low

In addition to the calculated PLL noise, Fig. 4 shows a plot of the SSB-noise characteristics of the circuit's VCO and crystal-reference oscillator. The oscillators are the main source of phase noise in a PLL. The information for plotting their noise can be obtained from the manufacturers of the oscillators, or from measurements made by the user.

Where noise reduction is of prime importance, select oscillators that generate minimum noise and have noise spectral densities that complement each other (as in Fig. 5). The point at which the two curves

Noise in 5th order PLL

Step	Instructions	Input Data/Units	Keys	Output Data/Units
1	Enter program			
2	Store	T_0	STO 0	
		T_1	STO 1	
		T_2	STO 2	
		T_3	STO 3	
		T_V	STO 4	
		Kp	STO 5	
		Kvo	STO 6	
		N	STO 7	
		Ao	STO 8	
		180	STO 9	
		10	STO .5	
3	Calculate	f	GSB 0	
		$S\phi ref$	R/S	
		$S\phi vto$	R/S	$S\phi o$
4	Repeat step 3 for other Fourier frequencies			

Note: Enter $S\phi ref$ and $S\phi vto$ in dB. $S\phi o$ answer is in dB.

Step	Key Entry	Key Code	Step	Key Entry	Key Code
001	(g) LBL 0	25 14 00	050	RCL 9	55 09
002	PRx	65	051	—	31
003	(g) DEG	25 24	052	STO .1	45 .1
004	(g)π	25 63	053	R↓	12
005	x	51	054	÷	61
006	2	02	055	RCL 5	55 05
007	x	51	056	x	51
008	STO .0	45 .0	057	RCL 6	55 06
009	(g) x²	25 53	058	x	51
010	RCL 0	55 00	059	RCL 7	55 07
011	x	51	060	÷	61
012	RCL 8	55 08	061	RCL 1	55 01
013	÷	61	062	÷	61
014	RCL 4	55 04	063	RCL .0	55 .0
015	x	51	064	÷	61
016	RCL 3	55 03	065	STO .2	45 .2
017	x	51	066	RCL .1	55 .1
018	RCL 3	55 03	067	x ⇄ y	11
019	—	31	068	(f) → R	16 34
020	RCL 4	55 04	069	1	01
021	—	31	070	+	41
022	RCL .0	55 .0	071	(g) → P	25 34
023	(g) x²	25 53	072	(g) 1/x	25 64
024	x	51	073	STO .3	45 .3
025	RCL 8	55 08	074	RCL .2	55 .2
026	RCL 1	55 01	075	RCL 7	55 07
027	x	51	076	x	51
028	(g) 1/x	25 64	077	x	51
029	+	41	078	STO .4	45 .4
030	RCL .0	55 .0	079	(g) x²	25 53
031	(g) x²	25 53	080	R/S	64
032	RCL 3	55 03	081	RCL .5	55 .5
033	x	51	082	÷	61
034	RCL 4	55 04	083	(g) 10^x	25 33
035	x	51	084	x	51
036	1	01	085	RCL .3	55 .3
037	—	31	086	(g) x²	25 53
038	RCL .0	55 .0	087	R/S	64
039	x	51	088	RCL .5	55 .5
040	CHS	22	089	÷	61
041	(g) →P	25 34	090	(g) 10^x	25 33
042	x ⇄ y	11	091	x	51
043	RCL 2	55 02	092	+	41
044	RCL .0	55 .0	093	(f) log	16 33
045	x	51	094	RCL .5	55 .5
046	1	01	095	x	51
047	(g) → P	25 34	096	PRx	65
048	R↓	12	097	(g) SPC	25 65
049	+	41	098	(g) RTN	25 13

REGISTERS

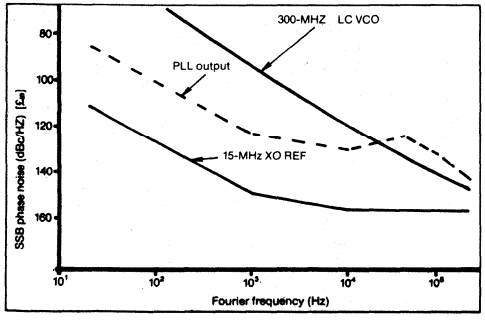
0 T_0	1 T_1	2 T_2	3 T_3	4 T_V	5 Kp	6 Kvo	7 N	8 Ao	9 180
S0	S1	S2	S3	S4	.5 10	S6	S7	S8	S9

0

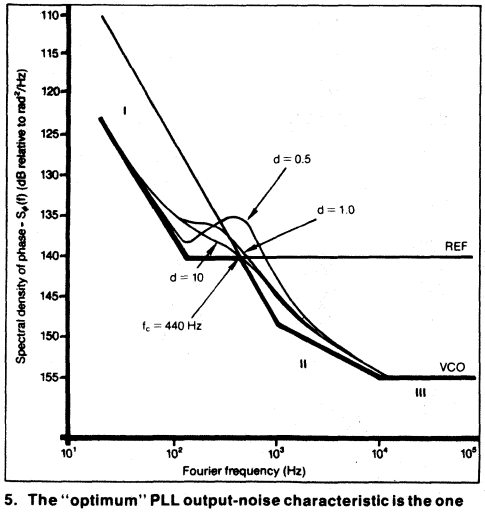
PLL noise and stability

cross is called the crossover frequency (f_c). This frequency is an important parameter for optimizing a PLL's noise characteristics.

In Fig. 5, the VCO noise-distribution plot is divided into three characteristic regions. High-quality oscillators generally exhibit this spectral-density relationship. In region I, $S_{\phi(f)}$ is typically proportional to $1/f^3$, so-called flicker-frequency noise; in region II, $S_{\phi(f)}$ is proportional to $1/f^2$, so-called white-frequency noise; and in region III, $S_{\phi(c)}$ is constant, so-called white-phase noise. Beyond region III, the bandwidth limitation of the circuit attenuates the noise to negligible levels.



4. A PLL is optimized for performance characteristics, such as stability, response time, and sideband levels; but the noise characteristics generally fall where they may, as exemplified in this plot of a fifth-order PLL.



5. The "optimum" PLL output-noise characteristic is the one that coincides most closely with the PLL's intersecting reference crystal oscillator and VCO-oscillator noise characteristics (heavy lines). A high damping-factor value (such as d = 10) makes the best correspondence with this criterion.

Region I noise stems from fluctuations in oscillator-circuit frequency-control components; region II, from thermal noise in the oscillator's gain element; and region III, from additive thermal noise from other elements of the circuit (including the gain element).

A plot of the optimum phase-noise characteristic of a PLL would coincide with the lower parts of the two oscillator curves (heavy lines in Fig. 5).

The type-2, second-order PLL circuit in Fig. 6 helps to illustrate how closely this condition can be approached. This circuit can be generalized by relating the integrator's time constants (T_1 and T_2) and the VCO's and phase comparator's transfer coefficients (K_v and K_p) with a damping factor (d), and with the reference and VCO crossover frequency ($f_c = \omega_c/2\pi$), as follows:

$$d = (T/2)\sqrt{K_pK_v/T_1};\ d>>1$$
$$T_2 = 4d^2/\omega_c$$
$$T_1 = T_2K_pK_v/\omega_c.$$

When these circuit parameters are considered together with the circuit's open-loop gain (note: $H(\omega) = 1$),

$$G(\omega)H(\omega) = \frac{K_pK_v}{T_1\omega^2}(-j\omega T_2 - 1),$$

and substituted in the phase-noise equation for $S_{\phi(\omega)0}$, the PLL's spectral density becomes

$$S_{\phi(\omega)0} = S_{\phi(\omega)VCO}\left[\frac{1}{\left(1-\frac{\omega_c^2}{4d^2\omega^2}\right)+\left(\frac{\omega_c^2}{\omega}\right)}\right]+$$
$$S_{\phi(\omega)REF}\left[\frac{\left(\frac{1}{2d}\right)^2\left(\frac{\omega_c}{\omega}\right)^2+\left(\frac{\omega_c}{\omega}\right)^2}{\left(1-\frac{\omega_c^2}{4d^2\omega^2}\right)+\left(\frac{\omega_c}{\omega}\right)^2}\right]$$

The "Optimizing PLL Phase Noise" program, with its subroutine 0, solves this equation for any Fourier frequency ($f = \omega/2\pi$). In Fig. 5, solutions are shown for damping-factor values (d) of 0.5, 1.0, and 10.

The largest damping factor (d = 10) causes the noise curve to approach the "optimum" noise characteristic most closely—when it lies completely between the VCO/reference-oscillator lines and as closely as possible to the lower lines. To satisfy this criterion, the curve generally passes through the frequency crossover point previously mentioned. Larger damping values than 10 will provide little further improvement. In fact, a larger damping value would slow response more than it would lower the noise output. Special cases may require low damping

10

Optimizing PLL phase noise

Step	Instructions	Input Data/Units	Keys	Output Data/Units
1	Enter program			
2	Store	fc	STO 2	
		d	STO 3	
		K_p	STO 7	
		K_v	STO 8	
3	Calculate phase noise	f	GSB 0	
		$S\phi_{vco}$	R/S	
		$S\phi_{ref}$	R/S	$S\phi_o$
4	Repeat step 3 for other values of Fourier frequency			
5	Calculate time constants		GSB 1	T1 T2

Note: —$S\phi$vco, $S\phi$ref and $S\phi$o in dB

Subroutine 0 must be performed before the time constants can be calculated with subroutine 1

Step	Key Entry	Key Code
001	(g) LBL 0	25 14 00
002	PRx	65
003	(g) π	25 63
004	x	51
005	2	02
006	x	51
007	(g) 1/x	25 64
008	RCL 2	55 02
009	(g) π	25 63
010	x	51
011	2	02
012	x	51
013	STO 1	45 01
014	x	51
015	(g) x^2	25 53
016	STO 4	45 04
017	RCL 3	55 03
018	(g) x^2	25 53
019	÷	61
020	4	04
021	÷	61
022	STO 6	45 06
023	CHS	22
024	1	01
025	+	41
026	(g) x^2	25 53
027	RCL 4	55 04
028	+	41
029	STO 5	45 05
030	(g) 1/x	25 64
031	R/S	64
032	1	01
033	0	00
034	÷	61
035	(g) 10^x	25 33
036	x	51
037	RCL 6	55 06
038	(g) x^2	25 53
039	RCL 4	55 04
040	+	41
041	RCL 5	55 05
042	÷	61
043	R/S	64
044	1	01
045	0	00
046	+	61
047	(g) 10^x	25 33
048	x	51
049	+	41
050	(f) log	16 33
051	1	01
052	0	00
053	x	51
054	PRx	65
055	(g) SPC	25 65
056	(g) RTN	25 13
057	(g) LBL 1	25 14 01
058	RCL 3	55 03
059	(g) x^2	25 53
060	4	04
061	x	51
062	RCL 1	55 01
063	+	61
064	PRx	65
065	RCL 7	55 07
066	x	51
067	RCL 8	55 08
068	x	51
069	RCL 1	55 01
070	÷	61
071	PRx	65
072	(g) SPC	25 65
073	(g) RTN	25 13

REGISTERS

0	1	2	3	4	5	6	7	8	9
		fc	d				K_p	K_v	

0

PLL noise and stability

factors—a value of 1 or even 0.5—to get a faster response or the special noise-distribution shapes that these lower damping factors produce.

After the phase-noise characteristics (based on the f_c of the oscillators and a selected damping factor) have been calculated, a second part of the optimizing program (subroutine 1) can then be used to calculate the time constants T_1 and T_2 for the given K_p and K_v of a type-2 second-order PLL.

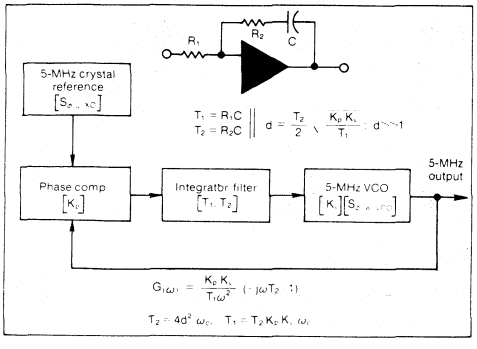
Determining a PLL's short-term frequency stability requires integration of the spectral density of the phase fluctuations to obtain the so-called Allan variance (a dimensionless measure of stability, where σ_y^2 is $\Delta f/f$ in a short sample period). Thus

$$\sigma_y^2(\tau, f_h) = \frac{2}{(\tau\nu\pi)^2} \int_0^{f_h} S_{\phi(f)} \sin^4(\pi f\tau)\,df,$$

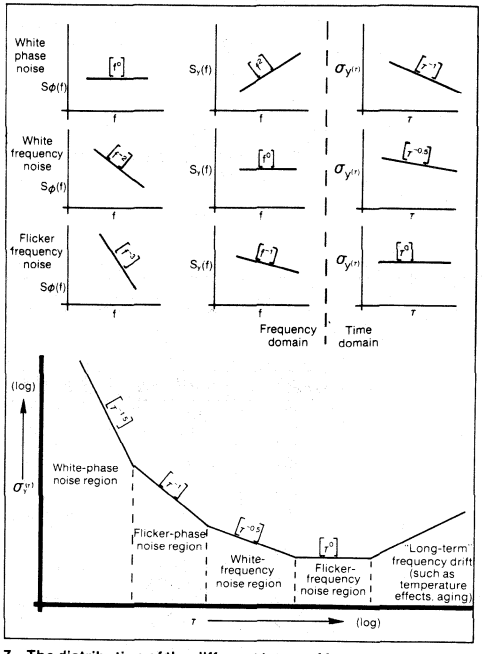
where τ is the sampling time (in seconds), ν is the long-term average frequency (in Hz), and f_h is the bandwidth, or maximum excursion of the offset from the carrier (the maximum Fourier frequency).

Figure 7 (top) shows the relationship between frequency or phase and the frequency spectral-noise densities, along with the resultant short-term frequency stabilities, for several distinct types of phase or frequency noise. A typical complex signal source (such as a PLL) could have a combined short-term frequency stability as in Fig. 7 (bottom). But such noise types generally do not obey simple integer-power curves and, therefore, pose a problem: The Allan equation does not have a closed-form solution for fractional powers, so it cannot be used directly. Nevertheless, very accurate answers can be obtained with Simpson's Rule and a programmable calculator.

Although the Allan equation requires integration over the Fourier frequency range of 0 to f_h, the low-frequency limit of 0 Hz cannot be used in a log-log Simpson's Rule integration. Fortunately, frequencies below $(2\pi\tau_h)^{-1}$, where τ_h is the longest sampling time, do not contribute appreciably to the value of the Allan variance. The longest sampling time for short-term effects is generally 1 s; therefore, for a measuring-system bandwidth of 1000 Hz, just the Fourier frequencies between about 0.16 and an f_h of 1000 Hz need be considered. (Since the manufacturer did not supply data below 2 Hz for the reference oscillator and VCO used in Fig. 5; a new oscillator with data to 0.1 Hz was substituted in Fig. 8, top.)



6. The phase-output noise in this type-2 second-order PLL can be optimized by adjusting the damping factor (d) in relation to the oscillator-noise crossover frequency (f_c).



7. The distribution of the different types of frequency and phase noise can be expressed as line segments that represent powers of frequency or time (top), and the overall distribution of a system can be shown by combining appropriate segments (bottom).

As shown in Fig. 7 (bottom) and Fig. 8 (top), the phase-noise curves can be approximated with straight-line segments. The segments are plotted on semilog paper with $S_{\phi(f)}$ measured in dBc on the vertical axis. Therefore, the segments,

$$y = ax^b,$$

can be established from the end points on their phase-noise curves—where $S_{\phi(f_1)}$ and $S_{\phi(f_2)}$ correspond to the low-frequency (f_1) and the high-frequency (f_2) end points, as follows:

$$b = \frac{S_{\phi(f_1)} - S_{\phi(f_2)}}{10\,(\log f_1 - \log f_2)}$$

and

Allan variance calculations

Step	Instructions	Input Data/Units	Keys	Output Data/Units
1	Key in the program			
2	Store	b	STO 7	
		α	STO .1	
		υ	STO .0	
		τ	STO 8	
3	Enter and start program	f_1	ENT ↑	
		f_2	ENT ↑	
		n	GSB .3	$\sigma^2 y$

Step	Key Entry	Key Code	Step	Key Entry	Key Code
001	(g) LBL 7	25 14 07	044	RCL 4	55 04
002	RCL 4	55 04	045	STO + 5	45 41 05
003	x	51	046	RCL 5	55 05
004	x ≠ y	11	047	GSB 0	13 00
005	÷	61	048	GSB 6	13 06
006	GTO 2	14 02	049	(g) RTN	25 13
007	(g) LBL 6	25 14 06	050	(g) LBL 5	25 14 05
008	ENT ↑	21	051	3	03
009	+	41	052	RCL 0	55 00
010	STO + 0	45 41 00	053	GTO 7	14 07
011	(g) RTN	25 13	054	(g) LBL 0	25 14 00
012	(g) LBL 3	25 14 03	055	(g) RAD	25 23
013	STO 3	45 03	056	STO 6	45 06
014	R ↓	12	057	(g) π	25 63
015	STO 2	45 02	058	x	51
016	R ↓	12	059	RCL 8	55 08
017	STO 1	45 01	060	x	51
018	GSB 0	13 00	061	(f) sin	16 42
019	STO 0	45 00	062	(g) x^2	25 53
020	RCL 2	55 02	063	(g) x^2	25 53
021	GSB 0	13 00	064	RCL 6	55 06
022	STO + 0	45 41 00	065	RCL 7	55 07
023	RCL 2	55 02	066	(f) y^x	16 54
024	RCL 1	55 01	067	x	51
025	STO 5	45 05	068	(g) DEG	25 24
026	—	31	069	(g) RTN	25 13
027	RCL 3	55 03	070	(g) LBL 2	25 14 02
028	+	61	071	(g) π	25 63
029	STO 4	45 04	072	RCL 8	55 08
030	0	00	073	x	51
031	STO 9	45 09	074	RCL .0	55 .0
032	(g) LBL 8	25 14 08	075	x	51
033	GSB 4	13 04	076	(g) x^2	25 53
034	STO + 0	45 41 00	077	(g) 1/x	25 64
035	2	02	078	x	51
036	STO + 9	45 41 09	079	2	02
037	RCL 3	55 03	080	x	51
038	RCL 9	55 09	081	RCL .1	55 .1
039	(f) x = y	16 61	082	x	51
040	GTO 5	14 05	083	PRx	65
041	GSB 4	13 04	084	(g) SPC	25 65
042	GTO 8	14 08	085	(g) RTN	25 13
043	(g) LBL 4	25 14 04			

REGISTERS

0	1	2	3	4	5	6	7 b	8 τ	9
0 ν	1 α	2	3	4	5	S6	S7	S8	S9

0

PLL noise and stability

$$a = 10^{\left(\frac{S_{\phi(f_1)} - 10\ b \log f_1}{10}\right)}.$$

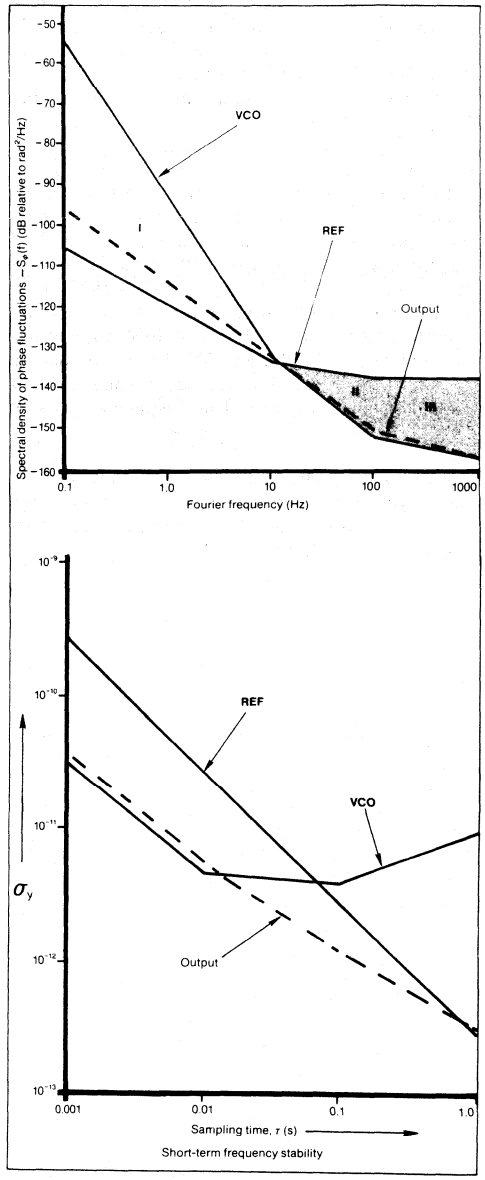
With coefficients a and b established for each line segment, the contributions of each segment to the overall Allan variance σ_y^2 can be calculated with the approximate Allan equation,

$$\sigma_y^2(\tau,f) = \frac{2a}{(\tau\nu\pi)^2} \int_{f_1}^{f_2} f^b \sin^4(\pi f \tau) df,$$

by a modified Simpson's Rule program supplied by Hewlett-Packard (HP-19C/29C *Applications' Book*, 1977). The Simpson's Rule is incorporated into the

Calculated short-term stability

Device	Segment I			
Reference oscillator	f_1 = 0.1 Hz, f_2 = 10 Hz a = 1.26 × 10^{-12}, b = −1.40			
	T/n 0.001/10	0.01/10	0.1/20	1/100
	σy^2 1.10 × 10^{-27}	1.05 × 10^{-25}	4.80 × 10^{-25}	1.76 × 10^{-26}
Voltage-controlled oscillator	f_1 = 0.1 Hz, f_2 = 10 Hz a = 5.01 × 10^{-10}, b = −3.90			
	T/n 0.001/10	0.01/10	0.1/20	1/100
	σy^2 4.49 × 10^{-27}	4.39 × 10^{-25}	1.34 × 10^{-23}	8.10 × 10^{-23}
PLL output	f_1 = 0.1 Hz, f_2 = 100 Hz a = 4.64 × 10^{-12}, b = −1.83			
	T/n 0.001/10	0.01/20	0.1/100	1/1000
	σy^2 2.43 × 10^{-24}	1.46 × 10^{-23}	1.19 × 10^{-24}	8.21 × 10^{-26}
Device	**Segment II**			
Reference oscillator	f_1 = 10 Hz, f_2 = 100 Hz a = 1.26 × 10^{-13}, b = −0.40			
	T/n 0.001/10	0.01/20	0.1/100	1/1000
	σy^2 3.27 × 10^{-23}	8.22 × 10^{-23}	7.56 × 10^{-25}	7.56 × 10^{-27}
Voltage-controlled oscillator	f_1 = 10 Hz, f_2 = 100 Hz a = 6.31 × 10^{-12}, b = −2.00			
	T/n 0.001/10	0.01/20	0.1/100	1/1000
	σy^2 1.59 × 10^{-24}	1.06 × 10^{-23}	1.63 × 10^{-25}	1.27 × 10^{-27}
PLL output	f_1 = 100 Hz, f_2 = 1000 Hz a = 2.51 × 10^{14}, b = −0.70			
	T/n 0.001/20	0.01/100	0.1/1000	1/10,000
	σy^2 1.04 × 10^{-21}	1.00 × 10^{-23}	1.01 × 10^{-25}	1.01 × 10^{-27}
Device	**Segment III**			
Reference oscillator	f_1 = 100 Hz, f_2 = 1000 Hz a = 2.00 × 10^{14}, b = 0.00			
	T/n 0.001/20	0.01/100	0.1/1000	1/10,000
	σy^2 6.08 × 10^{-20}	5.47 × 10^{-22}	5.47 × 10^{-24}	5.47 × 10^{-26}
Voltage-controlled oscillator	f_1 = 100 Hz, f_2 = 1000 Hz a = 6.31 × 10^{-15}, b = −0.50			
	T/n 0.001/20	0/01/100	0.1/1000	1/10,000
	σy^2 8.88 × 10^{-22}	8.27 × 10^{-24}	8.28 × 10^{-26}	



8. The phase-noise characteristics of the reference oscillator and the VCO can be expressed with three straight-line segments (I, II, and III); and the PLL output, by two (top). The short-term stability in terms of the Allan variance can then be calculated by keying the required coefficients as determined from the coordinates of these line-segment ends into the calculator (see Table) and plotting the results (bottom).

complete program for an HP-19C calculator—"Allan Variance Calculations." With a, b, ν, and τ established, the only decision remaining is the number of intervals, n, into which the segments must be divided. The more intervals chosen, the more accurate the calculation, but the longer the calculation takes. A good choice for a minimum n value (which must be an even number) is

$$n \geq 10\ [\tau(f_2 - f_1)].$$

The calculation time, then, is 0.056 n + 0.15 min.

To illustrate an application of the Allan variance calculations, the (a and b) program coefficients for the straight-line segments making up the VCO, reference oscillator, and overall output noise were determined from Fig. 8 (top). The coefficients are listed in the "Calculated Short-term Stability" table. Sample times of 1, 10, 100, and 1000 ms and end frequencies of 0.1, 10, and 1000 Hz were employed.

With these inputs, σ_y^2 was determined with the Allan variance program. The frequency stability,

$$\sigma_y(\tau) = \sqrt{\Sigma\sigma_y^2(\tau, f_h)},$$

was calculated, after summing the individual σ_y^2 contributions of each segment. A plot of σ_y vs sampling time for the VCO, reference, and output is shown in Fig. 8 (bottom).□

Acknowledgments

The author wishes to thank Dr. D. Halford and Dr. Fred L. Walls of the National Bureau of Standards, whose constructive discussions contributed to a more insightful understanding of the problems involved in working with PLL noise and short-term frequency stability.

References

1. Przedpelski, A.B., "Phase Lock Loops," *R.F. Design*, Sept./Oct., 1979, p. 24.

2. Halford, D., et al, "Spectral Density Analysis: Frequency Domain Specification and Measurement of Signal Stability," *Proceedings of the 27th Annual Symposium on Frequency Control*, U.S. Army Electronics Command, Fort Monmouth, NJ, June, 1973, p. 421.

3. Barnes, J.A., et al, "Characterization of Frequency Stability," *IEEE Transactions of Instruments and Measurements*, 1971, p. 105.

4. Lance, A.L., et al., "Phase Noise Characteristics of Frequency Standards," *Ninth Annual Precise Time and Time Interval Applications and Planning Meeting*, NASA-GSFC, Greenbelt, MD, 1977.

5. Walls, F.L., and Stein, S.R., "A Frequency-Lock System for Improved Quartz Crystal Oscillator Performance," *iEEE Transactions of Instruments and Measurements*, 1978, p. 249.

6. Stein, S.R., et al, "A Systems Approach to High-Performance Oscillators," *NBS Technical Note*, Boulder, CO.

7. Stein, S.R., and Walls, F.L., "Composite Oscillator Systems for Meeting User Needs for Time and Frequency," *NBS Technical Note*, Boulder, CO.

8. Cutler, L.S., and Searle, C.L., "Some Aspects of the Theory and Measurement of Frequency Fluctuations in Frequency Standards," *Proceedings of the IEEE*, February, 1966, p. 136.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

AN806A
Application Note

OPERATION OF THE MC14469

Prepared By:
Len Bogle and Bill Cravy
Logic and Special Functions Applications
Austin, Texas

The MC14469 is an addressable asynchronous receiver transmitter that finds applications in control of remote devices, transfer of data to and from remote locations on a shared wire and as an interface from remote sensors to a central processor.

OPERATION OF THE MC14469

The MC14469 is an asynchronous receiver/transmitter fabricated in metal-gate CMOS technology. The asynchronous data format consists of a serial stream of data bits, preceded by a start bit and followed by one or more stop bits. The asynchronous data format is used to eliminate the need to transmit the system clock along with the data bit stream. The fact that the MC14469 is made in CMOS technology means that it offers the high noise immunity and low power consumption characteristic of this technology.

The MC14469 can receive one or two eleven-bit words in a serial data stream. The first received word contains a seven-bit address and if it matches the programmed address of the receiver, the transmitter can be enabled to transmit its two data words. The 7 bits of the received address word must correlate bit by bit with the 7 address pins of the MC14469. A second word may optionally be received for data or control use. This word will contain seven data bits which will be latched onto the command data outputs if it has a valid command format. With 7 address lines, 2^7 or 128 separate units may be interconnected for simplex or full duplex data transmission. The MC14469 is capable of operation at data rates in excess of 30,000 baud controlled by an on chip oscillator. Applications include transmitting data from remote A/D converters, temperature sensors, or remote digital transducers as well as single line control of remote devices such as motors, lights or security devices.

DEVICE OPERATION

As shown in the block diagram of Figure 1, the MC14469 consists of three different sections: the receiver, the transmitter, and the oscillator. The receiver must receive (at least) a valid address on its receive data input (pin 19) in order to set up the necessary internal conditions to allow the transmitter to transmit its two data words. The address word consists of a start bit, seven address bits, the address identifier, an even parity bit and a stop bit. The address will be valid only if: a) the seven address bits match the address that is programmed on input pins A0 through A6, b) if the address identifier is high, and c) if the state of the parity bit causes the total number of ones in the address word, including the address identifier and parity bit, to be even. After reception of a valid address, the MC14469 can optionally receive a command word. Similar to the address word, the command consists of a start bit, seven data bits, a command identifier, an even parity bit and a stop bit. The command will be valid if the command identifier is low and the total number of ones, including the parity bit, is even. The reception of either a valid address or both valid address and a valid command can be used to set up the necessary internal conditions for transmission. The format of address and command words is shown in Figure 2.

Upon receipt of a valid address data stream, the MC14469 generates a valid address pulse (VAP) which in turn sets the internal valid address latch (VAL) and the internal send enable latch (SEL). See Figure 3 for a timing diagram. SEL remains high for eight data bit times or until the send input (pin 30) is taken high. If SEL is allowed to time out and a valid command word is subsequently received, a command strobe (CS) is generated which sets SEL high again. It again remains high for eight data bit times after being set. However, once the valid address latch (VAL) is set high, it will remain high until SEND goes high and resets it.

In order for the MC14469 to transmit its two data words, SEND must receive a rising edge while the valid address latch and send enable latch are both set high. Therefore, a send input must occur within eight bit times after the generation of either a valid address pulse or a command strobe, depending on the system configuration. After eight bit times, SEL will time out and transmission will be inhibited.

Figure 1A. MC14469 Block Diagram

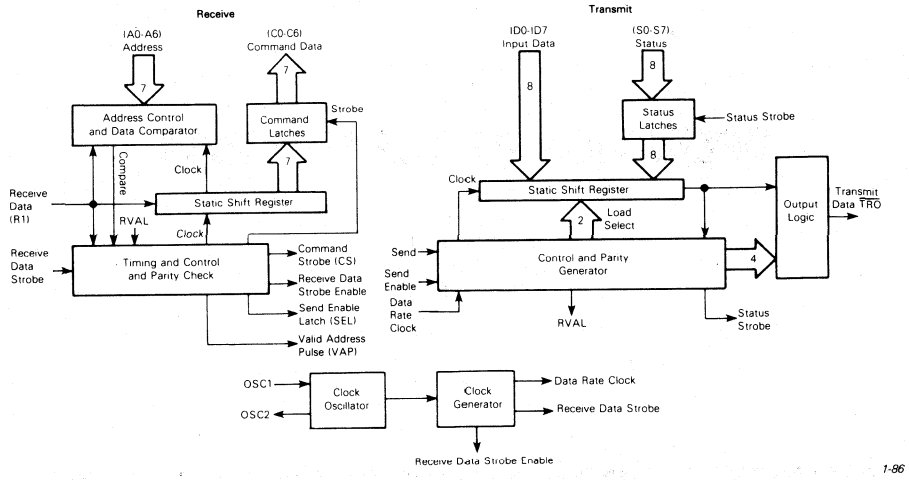
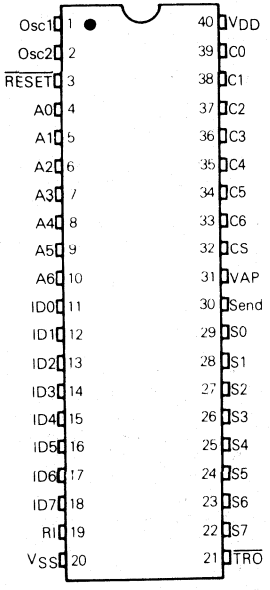


Figure 1B. Pin Assignments



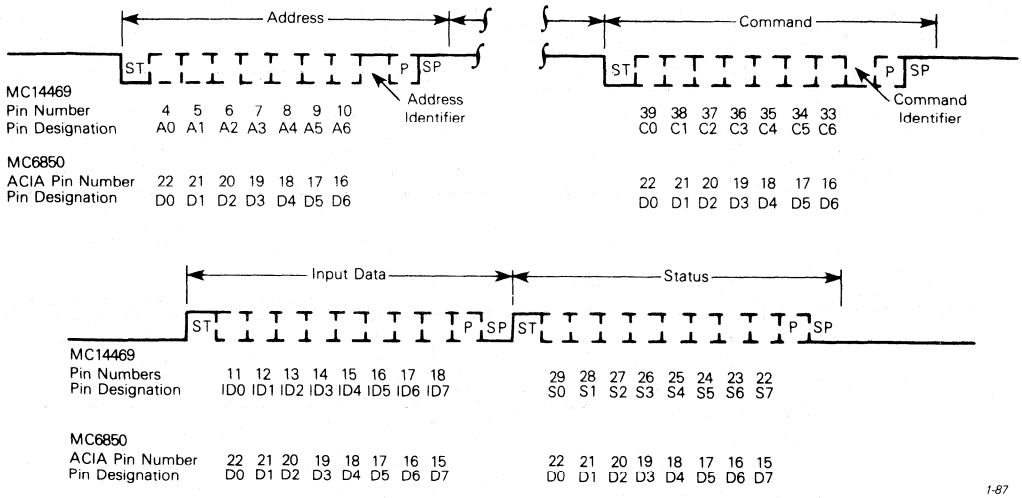
SEND going high resets VAL and SEL, and initiates the transmission of the data defined by input pins 11-18 and the status word defined by input pins 22-29. The transmitted words each contain a start bit, eight data bits, an even parity bit and a stop bit, all in UART compatible format. The transmitted data has the format shown in Figure 3. Note that the transmitted data must be inverted before being presented to the receiving device. This is usually accomplished by the line driver or transistor used to drive the common transmit wire.

OSCILLATOR OPERATION

The oscillator can be controlled by a ceramic resonator, a crystal or by an externally generated clock, and will typically operate at frequencies up to 2 MHz at a V_{DD} of 12 V. The oscillator frequency is divided by 64 to derive the receive data strobe and the data rate clock. Thus, the data bit period is 64 times the oscillator period. To allow for maximum phase jitter, the receive data strobe is centered at the middle of each data bit. The receipt of a start bit initiates the receive data strobe and synchronizes the strobe to the receive data bit stream.

Since data is sent asynchronously, the transmit oscillator and receive oscillator must be the same frequency to ensure that the receive data strobe occurs at the middle of the bit period. The maximum permissible variation in oscillator frequency between a transmitting unit and a receiving unit can be such that over the entire receive data word time the total error is plus or minus one-half data bit period.

Figure 2A. Data Format



Note: Pin numbers apply to plastic DIP only.

Figure 2B. Example Data Words

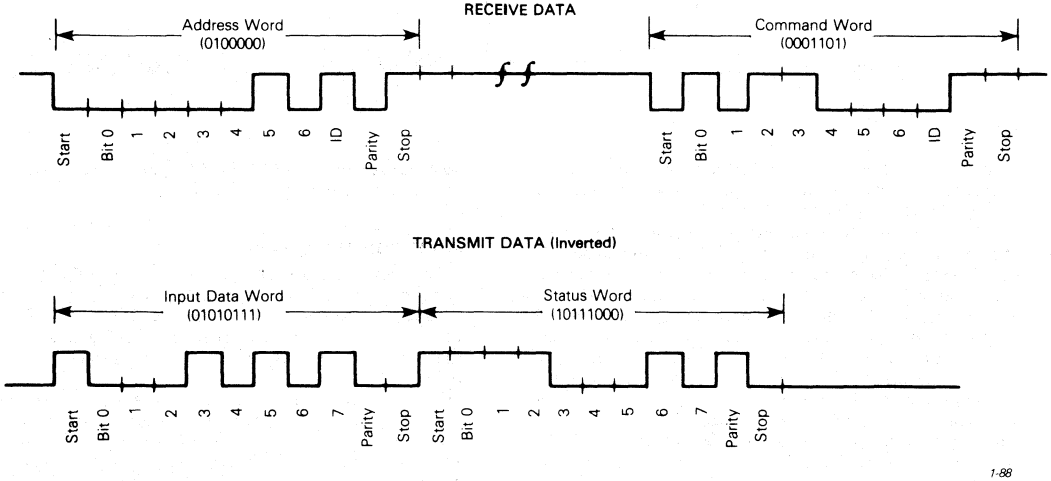
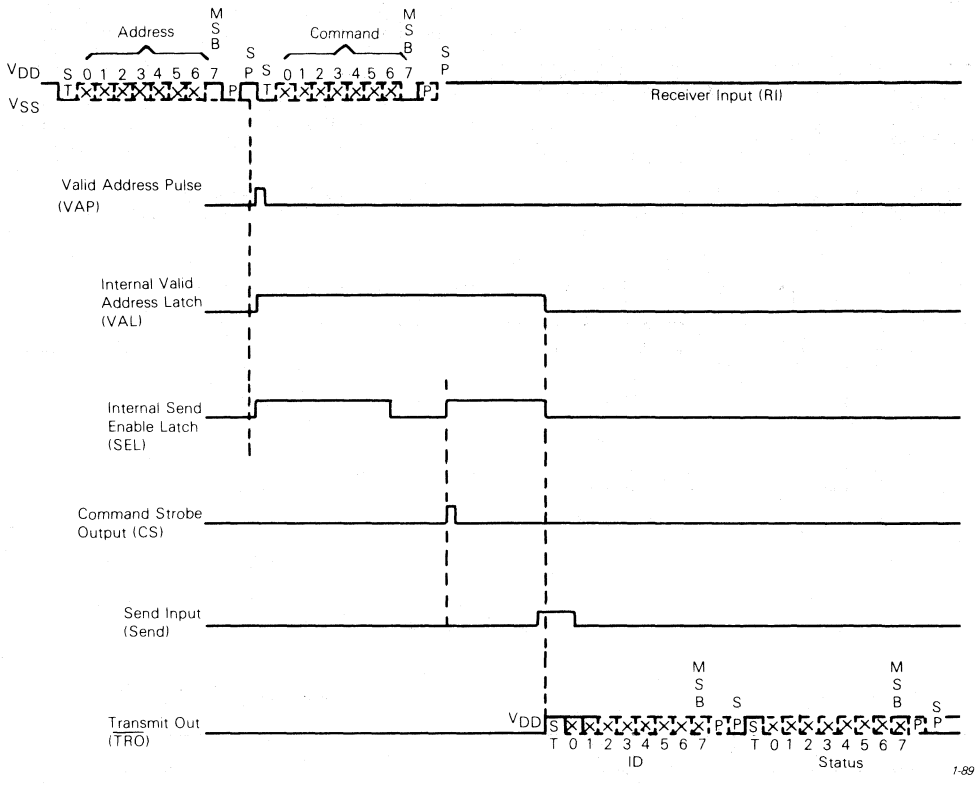


Figure 3. Typical Receive/Send Cycle



Each received data word consists of 11 bits, and thus the variation in oscillators cannot be more than half a bit time divided by 11 bit times or 4.5%.

The internal oscillator active circuitry consists of a normal CMOS inverter. When a high value resistor is used to provide DC feedback, the inverter is biased into its linear region and acts as an AC simplifier. The size of the feedback resistor is unimportant but needs to be small enough to overcome leakages and large enough to not load the oscillator output. Values in the range of 1 MΩ to 22 MΩ are common.

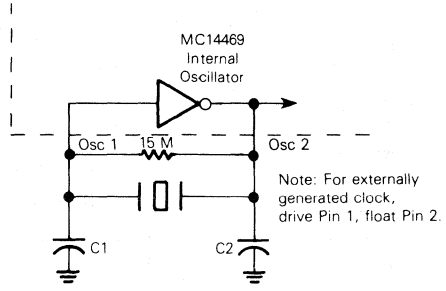
With the inverter biased as an AC amplifier the usual oscillator design is the Pierce type oscillator using a parallel resonant crystal. See Figure 4. Two capacitors, one from input to ground and one from output to ground, present the required capacitive load to the crystal. The series connection of the capacitors through ground avoids feedback of signal through the parallel capacitive path. An inductor or ceramic resonator can be substituted for the crystal to form a Colpitts oscillator ususally at less cost than a crystal but at the expense of frequency stability.

MODES OF OPERATION

The various modes of operation of the MC14469 are discussed below. For most applications, the send input is tied to either VAP or CS for fully automatic operations. If this is not done, the send input must receive a rising edge within eight bit times after VAP or CS in order for a transmission to occur.

It is possible to operate the MC14469 in a receive-only mode by tying SEND to V_{SS}. The device can receive valid address words only or both address and command words. Three different modes of operation of the MC14469 are possible depending on the signal used to drive the SEND input. These are RECEIVE ONLY MODE, SEND EQUALS VAP and SEND EQUALS CS.

Figure 4. Oscillator Circuit



Note: Ceramic Resonators
307.2 kHz ± 1 kHz for 4800 Baud Rate
C1 ≈ 50 pF
C2 ≈ 200 pF

1-90

RECEIVE ONLY MODE

If the MC14469 is in the receive only mode (i.e., if SEND is tied to V_{SS}) and if it is receiving valid address words only, it will respond with a valid address pulse after every other valid address. The intervening addresses will cause no output. The reason for this can be seen by examining the flow chart (Figure 5).

Assume the MC14469 has been reset, the receiver is initialized and is ready to be addressed. If the MSB of the first word received is a one (signifying an address), the device checks to see if the valid address and send enable latches are set. If neither is set, and if the word is a valid address, VAL and SEL are set and a valid address pulse is generated. If SEND is not taken high within eight bit times, SEL is reset and the device is re-initialized and ready to receive a command. If the next word received is an address rather than a command, the MC14469 will find that VAL is still set. It will then reset VAL, initialize the receiver, and wait for another address to be sent. As a result, the second consecutive address to be received will not result in the generation of a VAP. This problem does not arise when the device is enabled to transmit every time it is addressed, since VAL is reset during the transmission cycle. Notice that once VAL has been set by the reception of a valid address, the only way it can be reset without rejecting an address is by going through the transmission cycle.

A similar situation arises when the MC14469 is in the receive only mode and valid addresses and valid commands are alternately received. On the reception of the first valid address, VAL and SEL are set and a VAP is generated. After eight bit times, SEL is reset and the receiver is re-initialized. If the next received word is a command, the MSB will be zero, and when the device checks the valid address latch, it will find that it is set. If the command word has a valid format, it will be latched onto the command data outputs (C_0-C_6). A command strobe will be generated and the send enable latch will be set. Once again SEL will be reset after eight bit times and the receiver will be re-initialized. Thus, the reception of the first valid address and command words will result in the generation of a valid address pulse and a command strobe respectively, as expected. However, since data has not been transmitted, the next incoming address word will be rejected because the valid address latch has not been reset. The MC14469 will then reset VAL and re-initialize the receiver. The following word is a command word and because the valid address latch is not set, the command is also rejected and the receiver is re-intialized.

The next address and command words received will result in the generation of a VAP and CS. Thus, in the receive only mode, every other address and command words will be rejected.

SEND EQUALS VAP

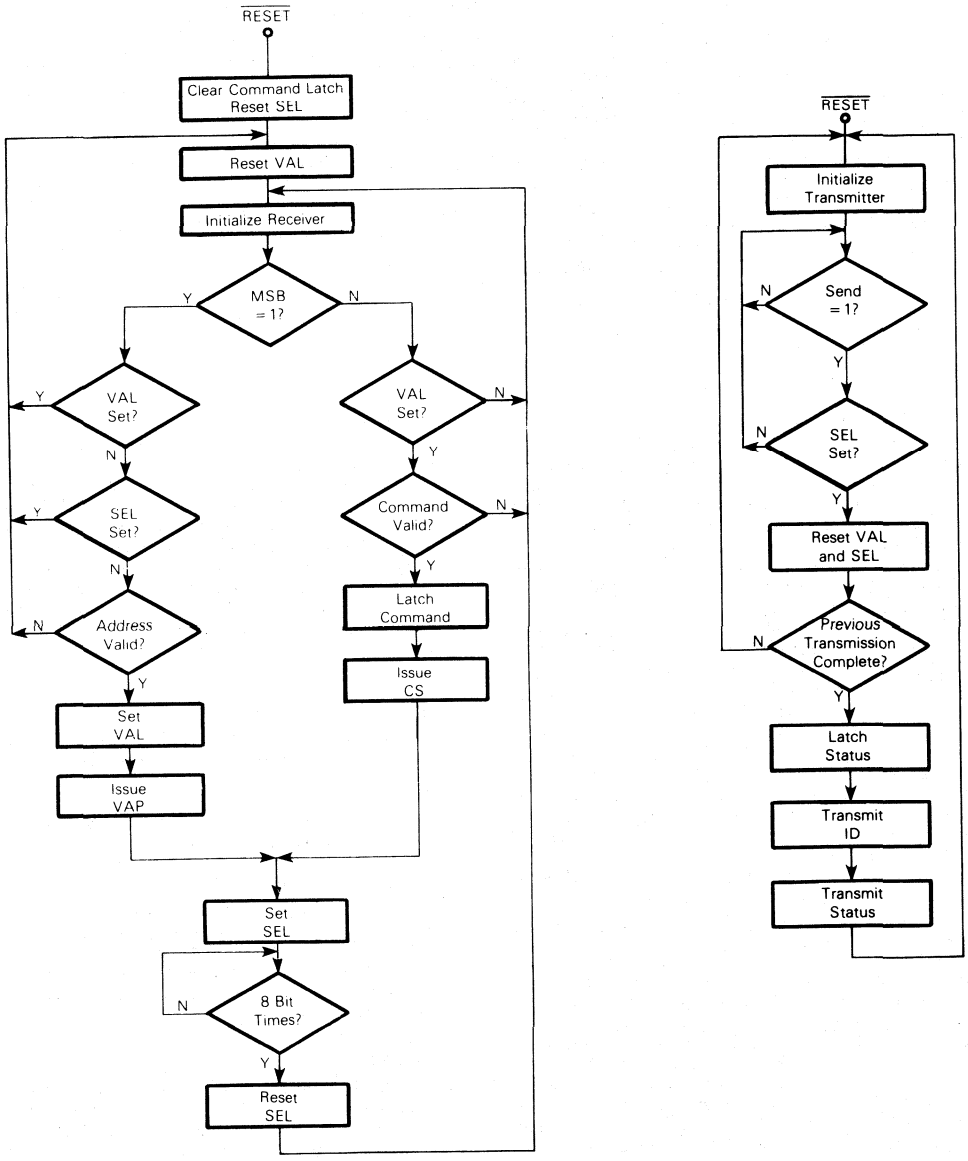
If only addresses are being received and if VAP is tied to SEND, a VAP is generated and data is transmitted when a valid address is received. Normally the transmit cycle is completed before a new address word is received. It is possible, however, for the reception of a new address to overlap the transmission of data. If this occurs, the current transmission is completed before the transmitter is allowed to start another transmission (see Figure 5).

If address and command words are alternately received while SEND is tied to VAP, a VAP is generated every time an address is received. The transmission of data begins as soon as a VAP is generated. This results in VAL and SEL being reset before completion of the received command word and causes the command word to be ignored.

SEND EQUALS CS

If SEND is tied to CS and if address and command words are alternately received, a VAP and CS are generated every time an address and command are received. Data is transmitted every time a CS is generated. Once again, data transmission can overlap the reception of a new address and command word. However, the current transmission will be allowed to finish transmitting (see Figure 5).

Figure 5. Flow Chart of MC14469 Operation



1-91

THE MC14469 AS A MASTER TRANSMITTER

The MC14469 can transmit only after it has received a valid address. For this reason it is usually considered to be a remote or slave device controlled by a UART, MPU or similar control system. However, it is possible to use the MC14469 as a master transmitter by giving it a start pulse on its receive input that has the format of a valid address. The idea is to set the address of the MC14469 that is to be used as a master transmitter in such a way that a valid address will consist of a single pulse which goes low for a certain number of bit times and then goes back high and remains high. This will allow the use of a one-shot or RC network to generate a start pulse which will look like a valid address to the MC14469. On receiving the start pulse, the MC14469 will generate a valid address pulse which can be tied to the SEND input in order to initiate a transmission.

As shown in Figure 2B, if the address of the MC14469 has an even number of ones, the parity bit will be high. The address identifier and stop bit are also high. Therefore, if the address begins with any odd number of zeros and ends with an even number of ones, the address word (start pulse) will need to go low for the start bit, stay low for an odd number of address bits, go high for the rest of the address bits, the address identifier, parity and stop bits. For example, if the address of the MC14469 is set to hex 00, a valid address will consist of a signal which goes low for eight bit times and then goes back high (see Figures 6 and 7). The other addresses for which the scheme will work are hex 60, hex 78 and hex 7E.

Figure 6.

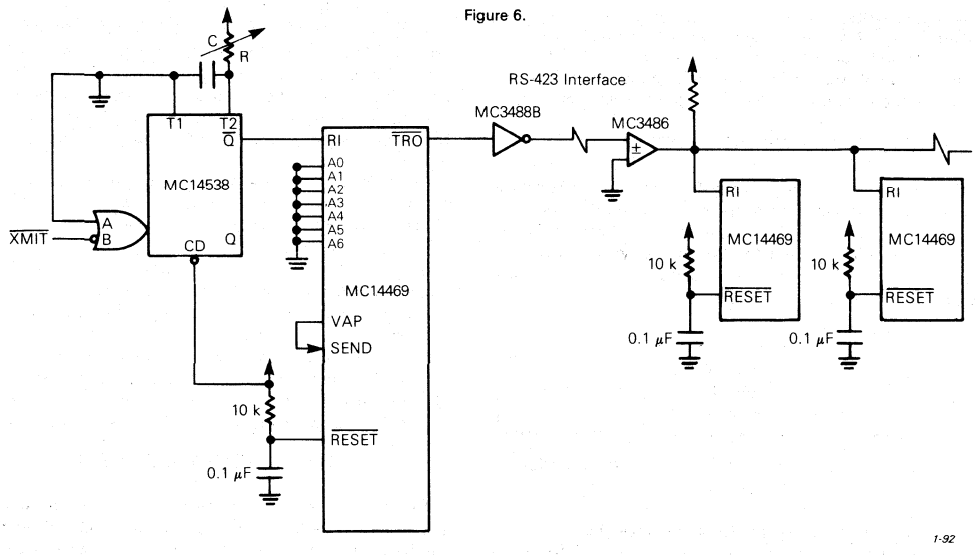
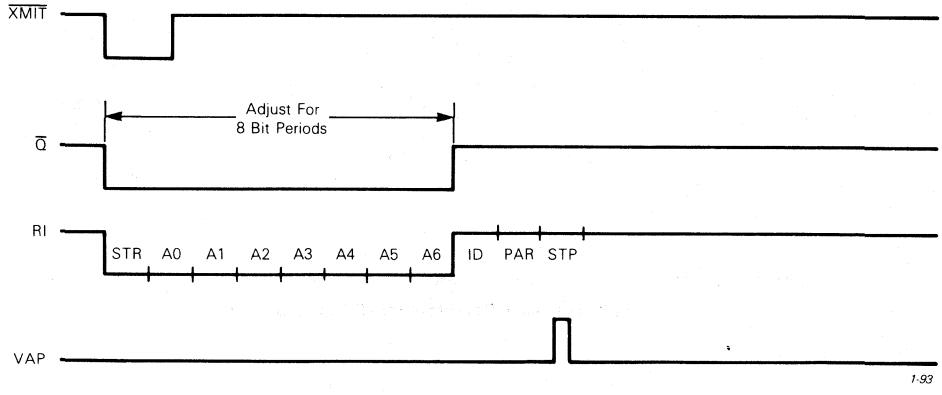


Figure 7. Transmitter Timing Diagram



AN1016

Infrared Sensing and Data Transmission Fundamentals

Prepared by: Dave Hyder
Field Applications Engineer

Many applications today benefit greatly from electrical isolation of assemblies, require remote control, or need to sense a position or presence. Infrared light is an excellent solution for these situations due to low cost, ease of use, ready availability of components, and freedom from licensing requirements or interference concerns that may be required by RF techniques. Construction of these systems is not difficult, but many designers are not familiar with the principles involved. The purpose of this application note is to present a "primer" on those techniques and thus speed their implementation.

THE GENERAL PROBLEM

Figure 1 represents a generalized IR system. The transmitting portion presents by far the simplest hurdle. All that needs to be accomplished is to drive the light source such that sufficient power is launched at the intended frequency to produce adequate reception. This is quite easy to do, and specific circuits will be presented later.

Figure 1. Simplified IR Sensing/Data Transmission System

The bulk of the challenge lies in the receiving area, with several factors to consider. The ambient light environment is a primary concern. Competing with the feeble IR transmitted signal are light sources of relatively high power, such as local incandescent sources, fluorescent lighting, and sunlight. These contribute to the problem in two ways. First, they produce an ambient level of stimulation to the detector that appears as a dc bias which can cause decreased sensitivity and, worst of all, saturation in some types of detectors. Second, they provide a noise level often 60 dB greater than the desired signal, especially in the form of the 50 or 60 Hz power frequency. Also, recall that the sensitivity of silicon photo detectors extends well into the visible range. This sensitivity, albeit reduced, causes severe interference since the sources in this region are often of significant power, e.g., incandescent lighting and sunlight. In addition to the visible component, both produce large amounts of infrared energy, especially sunlight.

Some IR applications are not exposed to this competition, and for them dc excitation of the source may be adequate. These include some position sensing areas and slow data links over short distances.

But the bulk of IR needs require a distance greater than 30 cm, speeds greater than 300 baud, and exposure to interfering elements. For these needs high-frequency excitation of the source is necessary. This ac drive permits much easier amplification of the detected signal, filtering of lower frequency components, and is not difficult to produce at the driving end. Optical filtering for removal of the visible spectrum is usually required in addition to the electrical, but this too is quite simple.

A WORD ABOUT DETECTORS

Figure 2 shows the three basic detection schemes: a phototransistor, a Darlington phototransistor, and a photodiode. All three produce hole-electron pairs in response to photons striking a junction. This is seen as a current when they are swept across the junction by the bias voltage, but they differ greatly in other respects.

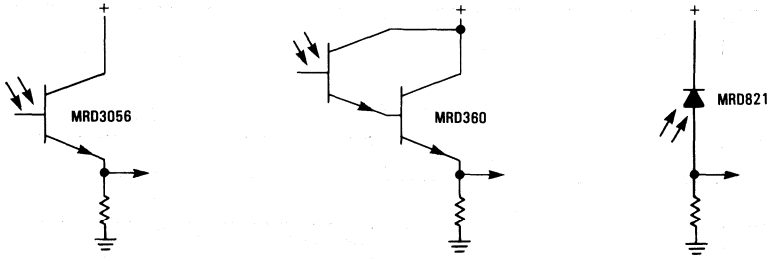


Figure 2. The Basic Detectors for IR Photosensing

The most sensitive is the Darlington. The penalties are temperature drift, very-low tolerance to saturation, and speeds, limited to about 5 kHz (usually much less). Next is the single transistor, having similar penalties (but to a lesser degree), with speeds limited to less than 10 kHz. Typically, they are limited to less than half that number. These two detectors normally find their use in enclosed environments, where ample source intensity is available to provide large voltage outputs without much additional circuitry (their prime advantage). Their detection area is almost never exposed to ambient light.

In virtually all remote-control applications (implying distance), the diode is the detector of choice. This is due primarily to its near-freedom from saturation, even in most sunlit environments. The penalty is sensitivity, often in the nanoamp or low microamp region, but balanced by response speed in the nanosecond range. This permits transmission frequencies in the 50-100 kHz area, providing ample data rates, inexpensive amplification, and easy filtering of noise.

For more information on the internal characteristics of these devices, see the appropriate section of the Motorola Optoelectronics data book (#DL118/D).

SHORT DISTANCES

Many applications in position sensing lend themselves well to the sensitive, if slow, nature of phototransistors. When a go, no-go situation exists, these provide a simple solution provided that ambient light is not present at the detector. The designer must ensure that the system operates even if this portion of the equipment is exposed, as by opening a hatch during servicing or final adjustment during production. This is often achieved via covers, tubes limiting light paths, or that enough directionality exists in the basic device construction to provide the needed isolation. Also available for this application are logic-level output devices, usually of the open-collector type, making processor or logic interfacing convenient.

The light source for these uses is chosen primarily by the distance needed. LEDs work well up to about 5 cm. Above this, incandescents are often used due to their high output and ease of drive with low-voltage ac. Fluorescent sources are seldom adequate due to their "cool" color temperature compared to incandescent. That is, not enough output in the near-infrared or infrared portion of the spectrum.

Data can be transmitted in these short distance situations, provided the speeds required are not great. An example is the electrical isolation of two adjacent PC boards in a rack, with IR elements facing each other across the short space. Here the data can be used to drive the LED directly; modulating a high frequency is not necessary.

Speed and sensitivity are the tradeoff. The resistor used to develop a voltage can be made larger to provide increased sensitivity, but speed suffers and tendency toward saturation increases. Values of 50-200 Ω are common, but can be higher.

MODERATE DISTANCES

For the general case of remote control or sensing at distances greater than 30 cm, the vast majority of applications utilize an LED source switched at a carrier frequency of 20 kHz to 50 kHz and a diode detector coupled to ac band-limited amplifiers. Although certainly more complex than the simpler short-distance sensors, today's product offerings make it an easy task to achieve 10 meters with a data rate of around 5,000 baud at very modest cost.

The transmission end is easily configured. Figure 3 shows a simple IR source capable of 50 kHz transmission. Note that no special techniques are needed to switch the diode at these frequencies. A burst of high frequency is created for each bit time in the data being sent. This mode of gating a carrier on and off is known as CW (continuous wave).

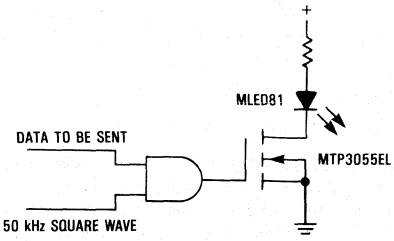


Figure 3. Basic IR Source Drive for CW Operation

The main areas of interest are the switch device and the diode current. Today's IREDs (infrared emitting diodes) are generally capable of around one ampere peak currents, but applications typically limit this to half that value. Most designs that use a 50 percent duty cycle square wave switching waveform have diode currents in the 100-500 mA range. It is important to realize that although IRED output increases linearly with drive current, it drops rapidly with increasing temperature. Therefore, reliability is not the only reason for resisting the temptation to increase range by driving the IRED harder. A diode with a 100 mA continuous rating can be reliably driven with a 200 mA square wave, and so on. It is quite common to use more than one IRED in series for increasing output and range, lowering the current requirements, and increasing reliability of the diodes.

The driver device can be a bipolar transistor or a FET. The bipolar works fine, but requires enough base current for saturation that the driving circuitry often must provide 10-20 mA or more. This may not be available directly from CMOS devices. Darlingtons solve this problem, but are usually much too slow. Another solution is an inexpensive logic-level FET such as the MTP3055EL, its physically smaller cousin, the MTD3055EL, or a MTP4N06L. This provides plenty of speed while being driven directly from any CMOS device, with absolute minimum parts count. A resistor (50-500 Ω) is sometimes used in series with the gate to moderate the very-high switching speed and noise from high frequency oscillations. The resistor is usually not needed if the gate is driven from a medium-speed CMOS gate such as the MC14081B or MC14011UB.

THE RECEIVING PROCESS

At the receiving end, the first item encountered is an IR optical filter as shown in Figure 4. This serves the sole purpose of attenuating the visible portion of the spectrum while leaving the IR intact. It can be a material specifically designed for the purpose, such as the Kodak filter series, but is usually an inexpensive acrylic plastic. This is almost any readily-available red, non-opaque plastic. Suitability is easily proven by inserting a sample between an emitter and detector while observing the

detector output. The IR signal should be minimally altered. This filter may be incorporated into the system as a unique piece of the material in front of the detector, or the entire front panel of the product may be made of this plastic. Sometimes lenses are actually molded from it (discussed in a later section).

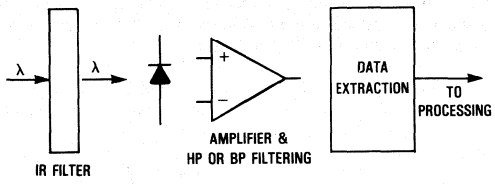


Figure 4. Basic IR Receiver

The detector diode behind the filter is usually constructed as a large-geometry device specifically designed for IR remote control, and presents a large area simply for more IR energy absorption or increased aperture. It is not unusual to find the material used for encapsulation to be red or black, and apparently opaque. The encapsulation serves as an IR filter, as in the case of the MRD821. Even so, an additional one is usually employed as mentioned above, often for the cosmetics of the product.

In addition to visible-light filtering mentioned above, electrical filtering must be applied to greatly attenuate the low-frequency interference present in both the visible spectrum and the IR. This is accomplished by three methods. First, coupling capacitance values are judiciously chosen to begin rolloff just below the transmitted frequency. This is quite effective since the area of interest is usually about a factor of 10^3, or some 9 to 10 octaves above the power-line frequencies.

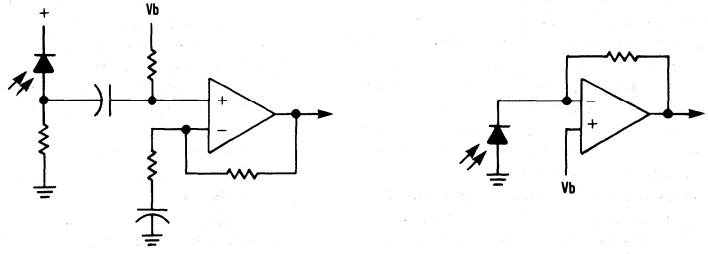
The second method is to use explicit high-pass filter circuitry, but in practice this is seldom needed due to the effectiveness of the other techniques. A third option is to use a bandpass amplifier, usually with an LC tank. More discussion of this later.

After the signal is brought up to a level sufficient for detection, some method must be employed to extract the data. Most common is a simple peak detector. This detects the presence of the high-frequency pulses, charging a capacitor up to a threshold in a few cycles, at which point a comparator signals the new level. In the absence of a signal (the carrier), the capacitor discharges until the comparator's lower threshold is reached, signifying the opposite logic level. Other techniques are also available, such as the phase-locked loop, whose lock-detect output can be used as the recovered logic-level data.

MORE ON RECEIVING CIRCUITS

Two general methods are used to begin the amplification. First the diode light current (a few microamps or less) may be used to develop a voltage across a series resistance, which is then capacitively coupled to the amplifier using the rolloff of low frequencies mentioned above, as shown in Figure 5a. Second, the current may be driven directly into the amplifier, as in Figure 5b, where the photo current is summed with the feedback current at the amplifier input. Note that in these and other figures, the amplifier symbol does not necessarily denote an actual integrated operational amplifier, but may symbolize a discrete amplifier.

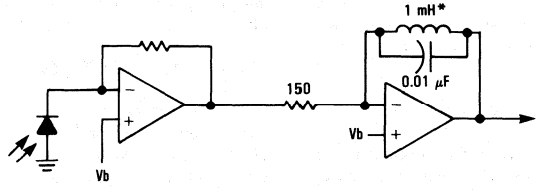
Figure 6 shows an amplifier system coupled to a bandpass amplifier centered about 50 kHz. Here the front end is actually an operational amplifier, used in the mode of Figure 5b. Various choices for operational amplifiers exist; perhaps the first hinges



(a) CAPACITIVELY-COUPLED FRONT END

(b) DIRECT-COUPLED DIODE FRONT END

Figure 5. Front-End Amplifier Options



*Toko type 10 PA or equivalent. Available from Digi-Key Corporation, phone (800) 344-4539.

Figure 6. Amplifier Chain Showing 50 kHz Bandpass Filter Second Stage

on the supply voltage. Some recent advances in the technology have greatly increased slew rates and gain-bandwidth products. This has permitted devices that are capable of operation on a single 5 volt supply, yet can be used in the 50 kHz range. An example of this is the MC34072 series, whose input common mode range includes ground, permitting the diode or the other amplifier input to be referenced there. If greater gains are needed, and higher supply rails are available, the MC34082 series provides slew rates of 25 V/μs, or twice that of the MC34083. These operational amplifiers in general do not have the low-noise performance of discrete versions, with the above devices being in the 30 nV/$\sqrt{\text{Hz}}$ region. However, the MC33077 provides excellent noise performance of about 4.5 nV/$\sqrt{\text{Hz}}$ at a similar slew rate on a 5 volt supply, although its common mode range does not include ground. A simple discrete amplifier example is shown in Figure 7.

Another option that should be considered for data reception is the MC3373 (Figure 8), which integrates many of the functions already described. This device contains the front-end amplifier, a negative-peak detector with comparator, and requires only a few external components. The amplifier may have the diode directly connected to it, or ac coupled for purposes of rolloff. A tuned circuit can be used for the better noise performance of a band-limited system. Some words of caution: supply bypassing close to the device, particularly at the gain-determining impedance (resistance or tuned circuit), is critical. Without proper bypassing, gain and range suffer. Also, a higher supply voltage of around 12 volts or so assists in greater range performance.

The vast majority of IR links in consumer products (VCRs, TVs) use an LC tank. The inductor is a shielded, adjustable slug type in the 1-5 mH range. Shielding in the form of a metal can usually encloses the entire subassembly, and the designer should expect to employ such shielding in most applications requiring moderate or long distance operation.

Note that in Figures 7, 8, and 9 the bias supply to the receiving diode is heavily decoupled from the supply via an RC. Any noise present at this point directly impacts system noise and sensitivity. Bandwidth is also often limited at the upper end as an aid in overall noise performance as seen in Figures 7 and 9. These amplifiers use small capacitors (33 pF, 10 pF, 100 pF) to roll off frequencies above 100 kHz.

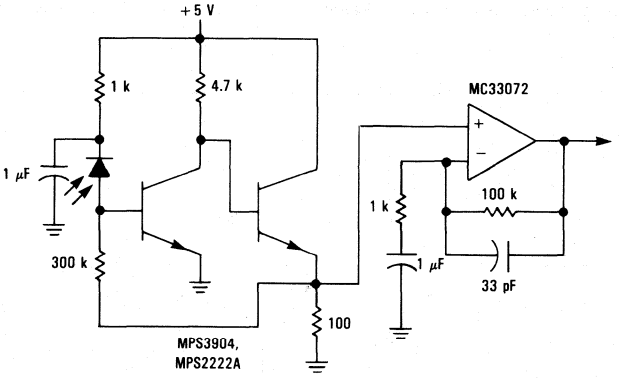


Figure 7. Simple Discrete Front End with Op Amp

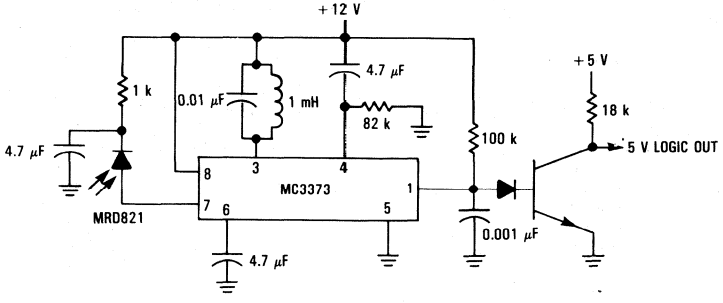


Figure 8. IR Receiver Using the Integrated MC3373

LONG DISTANCES

When the distance to be covered extends beyond 10 meters or so, other methods must be considered. The methods described below have resulted in ranges of 100 meters or more.

At the transmitting end, most of the options available center on increasing the power output. One way is to increase the IRED current, but this is subject to limits as previously discussed. Another solution is to use multiple diodes in series, often three. Note that this does not require additional supply current. Multiple diodes also provide one solution to those applications requiring less directionality, with the IREDs being slightly misaligned from one another.

The diodes can also be driven much harder, and produce proportionally higher instantaneous power, if they are pulsed with a very-short duty cycle. Currents of about an ampere are common, but for only a few microseconds and with a duty cycle of 5 percent or less. This also requires modified receiving techniques.

At the receiving end, most solutions center on increasing the aperture of the system such that simply more energy is gathered. Multiple receiver diodes can be connected in parallel, adding their currents, with the additional possibility of reducing directionality if needed. Another technique is to add a lens, with the diode being placed at the focal point. In higher volume production, this is often molded into a front panel and is usually of the red filtering plastic mentioned earlier. Some systems make use of a flat Fresnel lens, being somewhat more difficult to mount but very effective. They can also be hidden behind a plastic panel.

Front-end amplifiers superior to the simple operational amplifier or discrete versions already mentioned may be found in these highest-performance situations. Such an amplifier is shown in Figure 9, where low-noise transistors are used in a circuit designed specifically for low-noise applications.

When pulsed sources are used, some encoding scheme is normally used to transmit the data. One common technique is to use a single pulse for one edge of a data bit, and two or more closely spaced pulses to signal the opposite edge. These are simply differentiated by some flip-flops and a small amount of timing circuitry. Other schemes use multiple pulses at close intervals to indicate one logic level, and a differing number to denote the other.

CONCLUSION

As can be seen from this discussion, IR links have become quite easy to implement. With the basic principles in mind, the designer should be able to adapt the techniques mentioned here to his specific system needs.

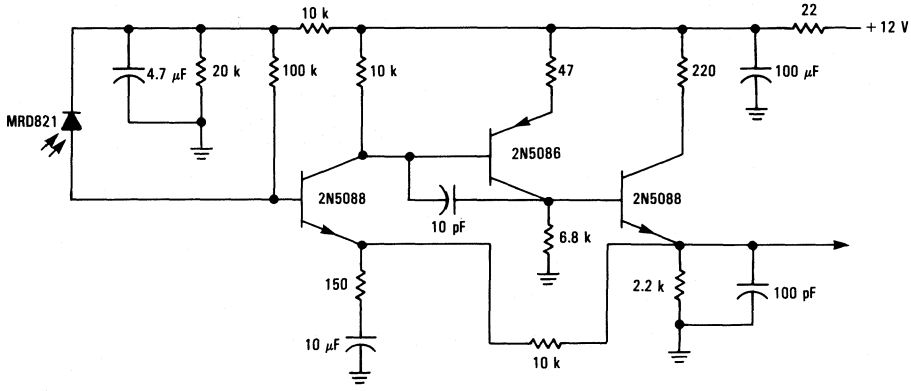


Figure 9. High-Performance Discrete Front-End Amplifier with Special Attention Paid to Noise

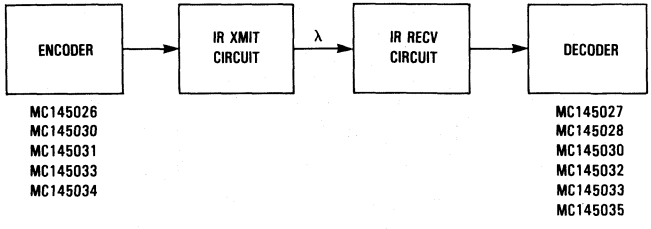


Figure 10. Utilizing Motorola's Encoders and Decoders

TECH BRIEFS

SIMPLIFIED REMOTE CONTROL CIRCUITS

DAVID BABIN
Application Engineering Manager
Motorola Inc.
Austin, TX

A new chip now provides a simple way to design remotely-controlled on/off devices such as valves and relays. The IC (MC145030) combines serial encoding and decoding functions that form the heart of many remote control circuits.

The 20-pin chip also contains an input amplifier, an output flip-flop, power-on reset, and an oscillator requiring only external *RC* components. No crystals or ceramic resonators are required. The IC is optimized for use in harsh industrial environments, operating from a 2 to 6 V supply over a temperature range of −40 to 85°C. Standby current drain is 100 μA maximum at room temperature while operating current is at most 2.5 mA at the worst-case supply voltage.

A typical remote control application would use the IC in both the controlling and receiving stations. At the master end, the chip would encode the nine-bit parallel address input and send this address onto a serial output line via a three-state encoder-out pin. This output returns to a high-impedance state after encoding is complete.

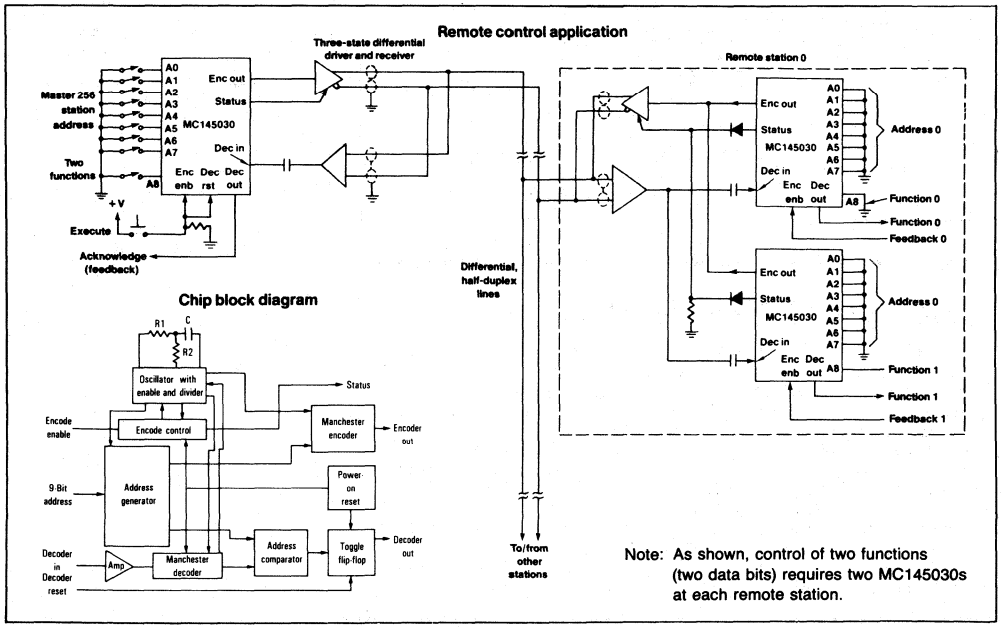
At the receiving end, another MC145030 chip serves as a decoder. The serial stream is received from the master and the address information is decoded. The IC would then compare this decoded address to the address applied to its own address lines. If the two addresses match, the chip would actuate the decoder-out line which would normally be connected to some output device such as a solenoid.

An output device toggles the receiver chip's encoder-enable input as an acknowledgment of either the output signal or of a completed operation. Once the chip senses this acknowledgment, the address is sent back to the master station over the serial line.

The master station treats this address as an acknowledgment that the output operation took place. The chip would compare the information with the address applied on its address lines. If the two addresses matched, decoder-out would toggle.

The master chip can activate any of 512 decoding stations in this manner. Alternatively, the designer can partition the nine address bits into address and data. This allows each remote station to perform several functions as in the remote control application shown.

The serial output of the encoder is in the form of Manchester Code,



Note: As shown, control of two functions (two data bits) requires two MC145030s at each remote station.

Reprinted from Machine Design, June 11, 1987.

TECH BRIEFS

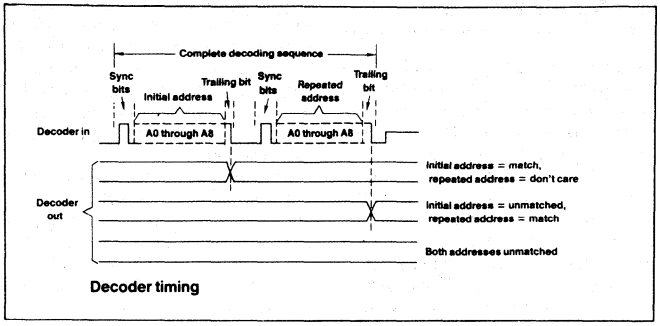
also known as Biϕ-L (biphase-level) code. The encoding technique allows both data and sync information to flow on one signal line instead of two.

The encode-enable input may connect directly to a push-button switch and pull-down resistor without external debounce circuitry. A rising edge on encode-enable aborts any decoding sequence in progress and starts an encoding sequence. Decoding functions are inhibited during this sequence, allowing half-duplex operation.

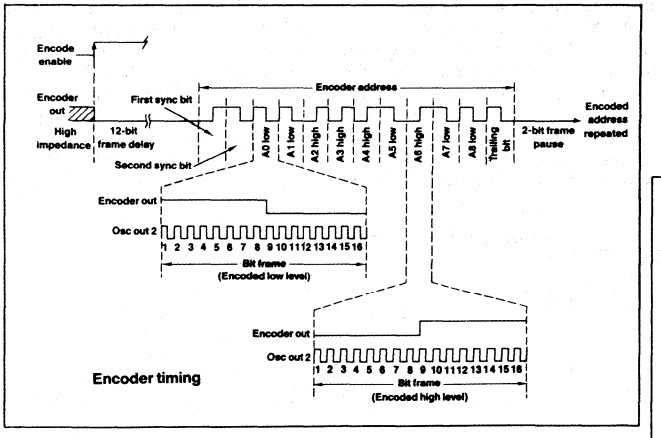
The chip issues an address twice during an encoding sequence to guard against system electrical noise problems. A status pin, when high, indicates that the device is encoding. The device is in standby or decoding when status is low.

Address inputs on the IC have on-chip pull-up devices which are inactive during standby to reduce power consumption. These pull-ups facilitate direct connection of SPST switches or jumpers to V_{ss}.

The decoder in pin is the input to the on-chip amplifier. Signal levels as low as 200 mV_{p-p} may capacitively couple through a 0.1 μF capacitor to this pin. The source impedance driving the series capacitor may be as high as 5 kΩ. Capacitive coupling provides proper amplifier biasing on chip. ■



Decoder timing



Encoder timing

Example RC values

f_{osc} (approx.)	R1	R2	C	Encode enable switch debounce time (approx.) *
452 kHz	30kΩ	5.6kΩ	100pF	1.3 ms
220 kHz	47kΩ	10kΩ	100 pF	2.8 ms
70 kHz	47kΩ	10kΩ	510 pF	8.7 ms
4.1 kHz	330kΩ	47kΩ	2,200pF	148 ms

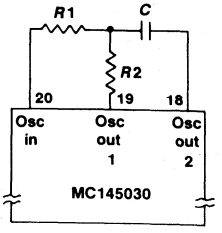
* And max. time for an encoding sequence.

Guidelines: 100 pF≤C≤0.1 μF
10kΩ≤R2≤500kΩ
2 (R2)<R1<10(R2)
R1 ≤ 1MΩ

CHOOSING THE R AND C

For design purposes, the maximum difference in oscillator frequency between encoding and decoding MC145030 chips should be no more than ±11%. Ambient temperature and supply voltage difference between the ICs affect this frequency difference. Tolerances of frequency-determining components $R2$ and C are calculated by a rule of thumb: $\Delta R2 + \Delta C + \Delta f_{IC} + \Delta f_{temp} + \Delta f_{sup} \leqq \pm 11\%$, where $R2$ = tolerance of $R2$, %; C = tolerance of C, %; f_{IC} = IC frequency variation from part to part (expected value = ±4%); f_{temp} = IC frequency variation over temperature (expected value = ±2% at 25°C ±40°); f_{sup} = IC frequency variation with supply (expected value = ±2% at 5 V ±0.5 V).

For example, from the above variances, $\Delta R2 + \Delta C + (\pm 4\%) + (\pm 2\%) + (\pm 2\%) \leqq \pm 11\%$; therefore, $\Delta R2 + \Delta C \leqq \pm 3\%$. Choose $R2$ with a ±1% tolerance and C with a ±2% tolerance. Polystyrene or mylar capacitors are recommended. $R1$ may be ±5%.



ANE425

Use of the MC68HC68T1 RTC with M6805 Microprocessors

Prepared by
Peter TOPPING
Microprocessor Applications
Motorola, East Kilbride

INTRODUCTION

The MC68HC68T1 is a real time clock (RTC) which also contains 32 bytes of RAM. Communication is via a serial port making the T1 suitable for use with single-chip microprocessors. The features on the MC68HC68T1 are similar to those on the MC146818 which, with its multiplexed-bus, is not so appropriate for use with MCUs. The MC68HC68T1 has, in addition, watchdog and power fail capabilities.

The MC68HC68T1 can be controlled using a clocked serial port, typically an SPI, but can also use port lines. This would be of use with a micro with no serial capability or in an application where the serial port was dedicated to another task. The example software was developed for use on an MC68HC05C4 and includes routines to use either the SPI or port lines.

Using one or other of these methods the code could be used in any 6805 microprocessor. The code would need to be modified to exclude the STOP instruction in an HMOS processor.

The example software constitutes an alarm clock using an 8-digit triplexed LCD display with ICM7231B driver, an MC68HC805C4 microprocessor and the RTC as shown in Figure 1. The software leaves the micro in stop mode until it is interrupted by the MC68HC68T1 in order to update the display. This is selected to be 1Hz by the software. The watchdog requirement cannot be met while the micro is in stop mode and is consequently not enabled in the software. As the software is for a battery supplied clock the power fail capability is also not used.

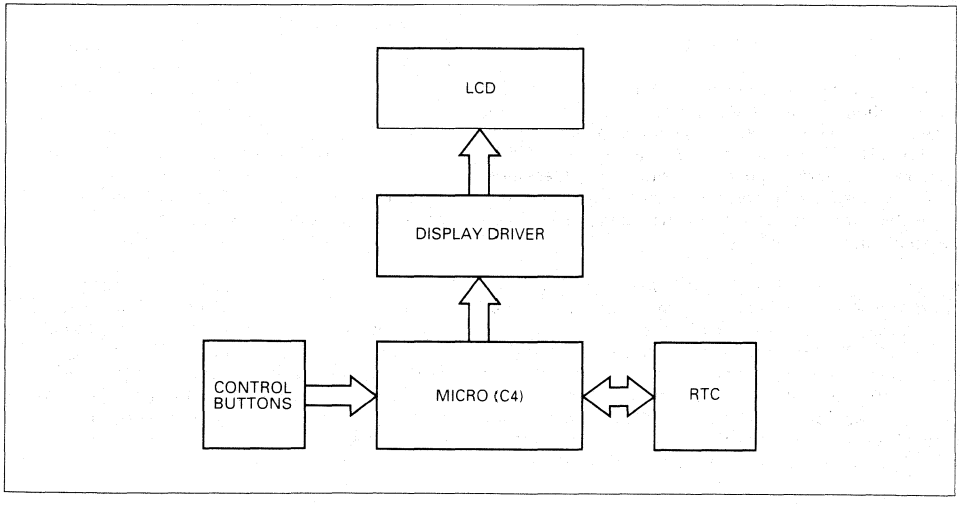


Figure 1.

CIRCUIT

Figure 2 shows the circuit used. The MC68HC68T1 can be connected either to port lines or to the SPI. With the two jumpers on MOSI and SCK connected between 1 & 2 the port lines are used. The third jumper on PD7 should also be connected between 1 & 2 to indicate to the software that I/O port communication is required. Jumper connection between 2 & 3 selects SPI communication. As MISO is an output from the RTC it can be connected in parallel to both the MISO and PC7 inputs on the C4.

The RTC uses a 32KHz clock for low power dissipation. The RTC and display driver consume about 65 microamps at 5.0v while the 2 milliamps taken by the C4 at a duty cycle of less than 1% contributes only another 15 microamps. The crystal frequency used on the C4 does not significantly affect overall consumption, 2MHz was used.

The ICM7231B LCD driver requires each character to be addressed through pins A0, A1 & A2 and the appropriate data written to pins D0, D1, D2, & D3. As the display is written to after the RTC registers have been read the port lines PC0 & PC1 can be used for both interfaces. The annunciators and decimal points (the latter not used in the example software) are controlled by their own pins. The ICM7231B driver used in the clock, displays -, E, H, L, P and blank to represent A, B, C, D, E and F respectively. The "A" version of this driver displays A through F normally but does not display a "-" or a blank and is therefore not suitable. Contrast can be adjusted using the potentiometer on pin 2 of the ICM7231B. With the clock supplied by a battery of four zinc-carbon cells a fixed 100 kohms from pin 2 to ground was found to be satisfactory.

SOFTWARE

The first page of the software listing constitutes hardware address definitions and RAM allocation. As well as working space the RAM contains an image of the registers within the 68HC68T1. These consist of 3 time registers, 4 date registers, 3 alarm registers and 3 status/control registers. The alarm registers are different from the time/date registers in that they are write only and consequently have been treated differently in software.

Interrupts are vectored to address $100 and the code at the start of the second page decides where the interrupt has come from. If it is not the result of a button press it must be from the MC68HC68T1 and its registers are read. Firstly the status register is read. This serves to return the interrupt line to a high and also allows the alarm bit (bit 1) to be checked to see if an alarm has occurred. If it has then bit 7 on port B is set high and the T1's clock output is enabled at 64 Hz. Either signal can be used to provide an alarm.

All the time registers are then read and displayed according to the selected display format (see below). The second page handles time displays and the third page those of date and alarm. As the alarm registers in the MC68HC68T1 are write only, alarm data is derived from the RAM of the micro.

Button 1 has two functions according to whether the clock is in the normal or the set-up mode. The mode is contained in status bit 0 in RAM location STAT. In set-up mode it increments the display format in RAM location DSPLY. In the set-up mode it increments the register currently "opened" by button 2. In this mode it sets STAT bit 1 to indicate to the main set-up routine that a change has been made. This part of the software also keeps track of the maximum permissible value for each register.

Button 2 is only used for set-up. When pressed it selects the set-up mode and displays the first register (time seconds). Subsequent presses move to the next register. A press from the last register (alarm hours) returns the clock to normal mode. Entry to the set-up routine stops further interrupts from the MC68HC68T1. The time and date registers are read from the MC68HC68T1 and so will be correct if it's power has been maintained even if the micro's RAM is not valid (alarm values are read from RAM). If a value is changed, by pressing button 1, then the new value is written to the appropriate MC68HC68T1 register when the next register is selected. Alarm values are written immediately to the MC68HC68T1 so that the displayed value is the same as that in the corresponding MC68HC68T1 alarm register.

The serial routine on page 12 communicates with the MC68HC68T1 using I/O lines and the next page shows how this can be done with less code using the SPI. The software is written for the level 1 SPI contained in the MC68HC05C4 & L6.

ALARM CLOCK OPERATION

The clock is controlled by two buttons. Button 1 selects the format of the display by sequencing through the formats shown in Table 1.

Format 5 shows the day of the week using the annunciator on the display. A "1" in register 6 ($23) of the MC68HC68T1 which corresponds to Sunday displays at position 2 and so on through Saturday at position 8. This only appears when the display is set to date. Position 1 is reserved to indicate that the alarm is enabled and shows on all display formats if the alarm SPST switch is closed. Button 1 is also used to cancel the alarm.

Button 2 allows the various registers in the MC68HC68T1 to be set up. When this button is pressed the number in position 5 of the display indicates the register whose contents are being displayed in position 7 and 8 (see table 2). Pressing button 2 again moves to the next register without changing anything, pressing button 1 while in this mode increments the contents of the displayed register, the new contents are written into the register when button 2 is used to move to the next register.

Pressing button 2 when the last register (9) is being displayed returns the clock to the normal run mode in which the required format can be selected using button 1.

No.	Display Format
1	Time - hours (24 hr format), minutes and seconds.
2	Time - hours (24 hr format), minutes and date.
3	Time - hours (12 hr format), minutes and seconds.
4	Time - hours (12 hr format), minutes and date.
5	Date - day, month and year including day of week.
6	Alarm time in 24 hr format.

Table 1 Display Formats

Display	Address	Function	Range
0	$20	seconds	0 - 59
1	$21	minutes	0 - 59
2	$22	hours	0 - 23
3	$23	day of week	1 - 7 (Sun. - Sat.)
4	$24	day of month	1 - 31
5	$25	month	1 - 12
6	$26	year	0 - 99
7	$28	alarm seconds	0 - 59
8	$29	alarm minutes	0 - 59
9	$2A	alarm hours	0 - 23

Table 2 MC68HC68T1 Registers

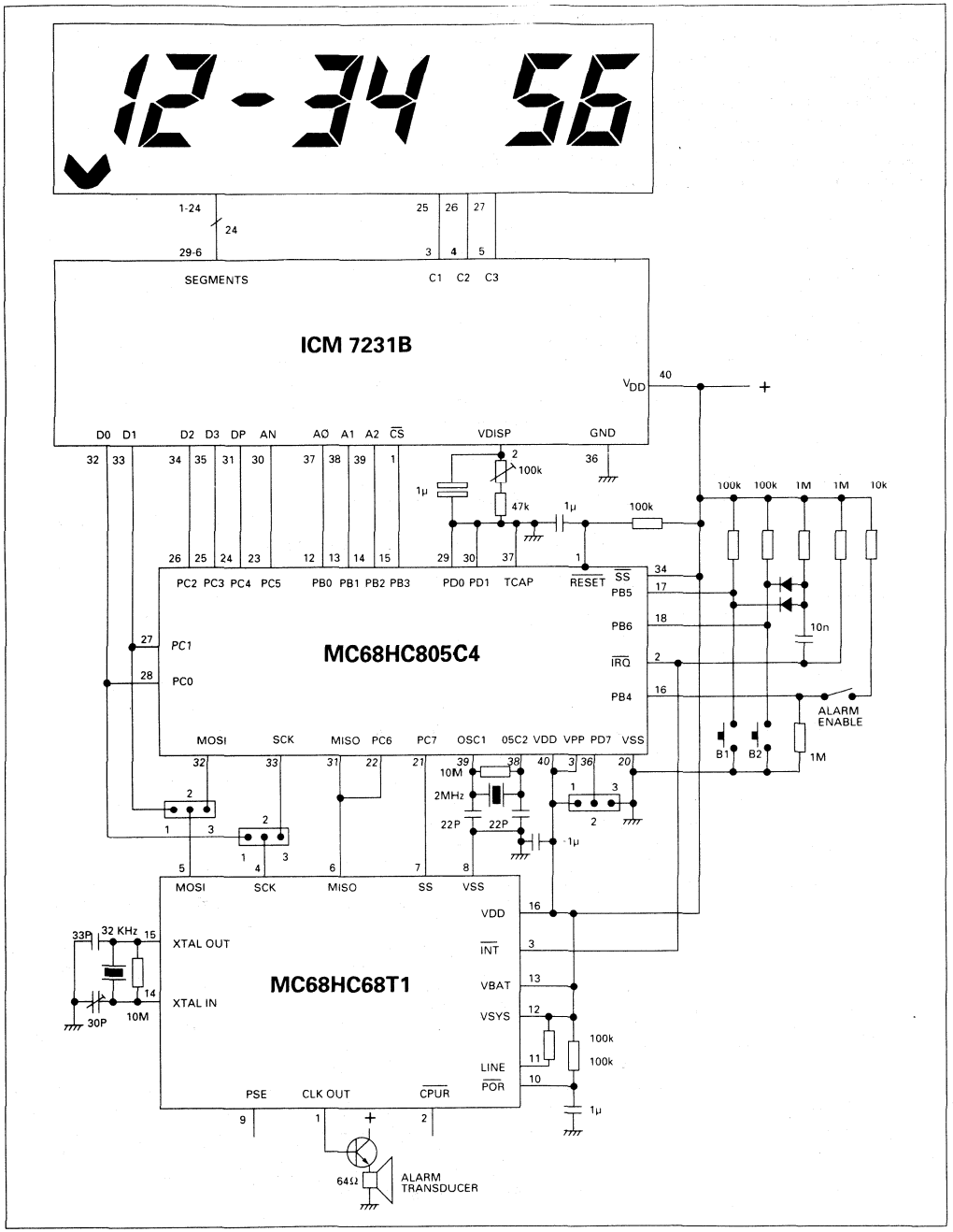

12-34 56
1-24
24
29-6
25 26 27
3 4 5
SEGMENTS
C1 C2 C3
ICM 7231B
VDD
40
+
D0 D1 D2 D3 DP AN A0 A1 A2 CS VDISP GND
32 33 34 35 31 30 37 38 39 1 36
2
100k
1µ
47k
1µ
100k
100k 100k 1M 1M 10k
26 25 24 23 12 13 14 15 29 30 37 1
PC2 PC3 PC4 PC5 PB0 PB1 PB2 PB3 PD0 PD1 TCAP RESET SS
34
PB5
17
PB6
18
10n
MC68HC805C4
27
PC1
28
PC0
IRQ
2
PB4
16
ALARM ENABLE
MOSI SCK MISO PC6 PC7 OSC1 05C2 VDD VPP PD7 VSS
32 33 31 22 21 39 38 40 3 36 20
10M
2MHz
22P 22P
1µ
B1 B2
1M
MOSI SCK MISO SS VSS
5 4 6 7 8
VDD
16
INT
3
VBAT
13
VSYS
12
100k
100k
LINE
11
POR
10
1µ
MC68HC68T1
33P
32 KHz
15
XTAL OUT
XTAL IN
14
30P
10M
PSE CLK OUT CPUR
9 1 2
64Ω
ALARM TRANSDUCER

Figure 2.

rtc4.s05

```
                        ************************************************
                        *                                              *
                        *       MC68HC68T1 - MC68HC05C4 Clock          *
                        *                                              *
                        *       P. Topping          16th March '89     *
                        *                                              *
                        ************************************************

00000001                PORTB   EQU     $0001           PORT B DATA
00000002                PORTC   EQU     $0002           PORT C DATA
00000003                PORTD   EQU     $0003           PORT D DATA
00000005                DDRB    EQU     $0005           PORT B DDR
00000006                DDRC    EQU     $0006           PORT C DDR

0000000a                SPCR    EQU     $000A           SPI CONTROL REGISTER
0000000b                SPSR    EQU     $000B           SPI STATUS REGISTER
0000000c                SPD     EQU     $000C           SPI DATA REGISTER

00000000                SCK     EQU     0               SERIAL CLOCK
00000001                MOSI    EQU     1                 "    OUT (MCU)
00000006                MISO    EQU     6                 "    IN  (MCU)
00000007                SS      EQU     7                 "    ENABLE

                        ORG     $0050


00000050                STAT    RMB     1               STATUS FLAGS
                        *                               0: MODE   0: NORM, 1: SET-UP
                        *                               1: CHANGE 0: NO,   1: YES
                        *                               2: REG.   0: TIME, 1: ALARM

00000051                Q       RMB     8               DISPLAY REGISTER
00000059                DSPLY   RMB     1               DISPLAY MODE
0000005a                W1      RMB     1               TEMP. STORAGE
0000005b                W2      RMB     1                 "       "
0000005c                W3      RMB     1                 "       "
0000005d                W4      RMB     1                 "       "
0000005e                W5      RMB     1                 "       "
0000005f                W6      RMB     1
00000060                ADDR    RMB     1               SERIAL ADDRESS
00000061                DPNT    RMB     1               RAM POINTER

00000062                SEC     RMB     1               68HC68T1 TIME  SECONDS  ($20)
00000063                MIN     RMB     1                   "       "  MINUTES  ($21)
00000064                HOUR    RMB     1                   "       "  HOURS    ($22)
00000065                DAY     RMB     1                   "       "  DAY      ($23)
00000066                DATE    RMB     1                   "       "  DATE     ($24)
00000067                MONTH   RMB     1                   "       "  MONTH    ($25)
00000068                YEAR    RMB     1                   "       "  YEAR     ($26)
00000069                ASEC    RMB     1                   "    ALARM SECONDS  ($28)
0000006a                AMIN    RMB     1                   "       "  MINUTES  ($29)
0000006b                AHOUR   RMB     1                   "       "  HOURS    ($2A)
0000006c                STREG   RMB     1               STATUS REGISTER         ($30)
0000006d                CCREG   RMB     1               CLOCK CONTROL REGISTER  ($31)
0000006e                ICREG   RMB     1               INT. CONTROL REGISTER   ($32)

                        ORG     $0100
```

rtc4.s05

```
                                ****************************************************
                                *                                                  *
                                *       Interrupts originating from the HC68T1     *
                                *       or a keypress start here.                  *
                                *                                                  *
                                ****************************************************

00000100  0a0103        IRQ1    BRSET   5,PORTB,IRQ2
00000103  cc01ba                JMP     BUT1            1 PRESSED
00000106  0c0103        IRQ2    BRSET   6,PORTB,IRQ3
00000109  cc0212                JMP     BUT2            2 PRESSED

0000010c  a601          IRQ3    LDA     #1              READ STATUS REGISTER
0000010e  b75a                  STA     W1              TO RESTORE IRQ TO HIGH
00000110  a630                  LDA     #$30
00000112  b760                  STA     ADDR
00000114  a66c                  LDA     #STREG
00000116  b761                  STA     DPNT
00000118  cd02f6                JSR     READ

0000011b  09010e                BRCLR   4,PORTB,NOTAL   ALARMS ARMED ?
0000011e  036c0b                BRCLR   1,STREG,NOTAL   YES, HAS ONE OCCURED ?
00000121  1e01                  BSET    7,PORTB         YES, DO IT
00000123  a601                  LDA     #1
00000125  b75a                  STA     W1
00000127  a6bf                  LDA     #$BF            64Hz CLOCK OUT
00000129  cd02d4                JSR     CCONLY

0000012c  3f5e          NOTAL   CLR     W5              READ ALL TIME REGISTERS
0000012e  a607                  LDA     #7              FROM 68HC68T1
00000130  cd028d                JSR     RWSU
00000133  cd02f6                JSR     READ
00000136  ae08                  LDX     #8              PREPARE TO WRITE DISPLAY
00000138  045932                BRSET   2,DSPLY,DISP2   NOT TIME ?
0000013b  a60a          DISP1   LDA     #$0A            TIME DISPLAY
0000013d  b753                  STA     Q+2
0000013f  b662                  LDA     SEC             SECONDS
00000141  01590a                BRCLR   0,DSPLY,SC
00000144  a401                  AND     #$01            DISPLAY DASH ONLY
00000146  2704                  BEQ     DT              ON EVEN SECONDS
00000148  a60f                  LDA     #$0F            IF DATE DISPLAY
0000014a  b753                  STA     Q+2             IS SELECTED
0000014c  b666          DT      LDA     DATE            DATE INSTEAD OF SECONDS
0000014e  ad56          SC      BSR     SPLIT
00000150  b657                  LDA     Q+6             LEADING DIGIT
00000152  2604                  BNE     CONT            A ZERO ?
00000154  a60f                  LDA     #$0F            YES, REPLACE WITH BLANK
00000156  b757                  STA     Q+6
00000158  b663          CONT    LDA     MIN             MINUTES
0000015a  ad4a                  BSR     SPLIT
0000015c  b664                  LDA     HOUR            HOURS
0000015e  cd02e0                JSR     FORMAT
00000161  ad43                  BSR     SPLIT
00000163  b651                  LDA     Q               ZERO ?
00000165  2637                  BNE     OK              NO
00000167  a60f                  LDA     #$0F            YES REPLACE
00000169  b751                  STA     Q               WITH BLANK
0000016b  2031                  BRA     OK
```

rtc4.s05

```
118                                  ************************************************
119                                  *                                              *
120                                  *       Date and alarm displays.               *
121                                  *                                              *
122                                  ************************************************
123
124 0000016d  00591e     DISP2   BRSET   0,DSPLY,DISP3   NOT DATE ?
125 00000170  b668               LDA     YEAR            DATE DISPLAY
126 00000172  ad32               BSR     SPLIT
127 00000174  b667               LDA     MONTH           MONTH
128 00000176  ad2e               BSR     SPLIT
129 00000178  b666               LDA     DATE            DATE
130 0000017a  ad2a               BSR     SPLIT
131 0000017c  a60a               LDA     #$0A            INSERT DASHES
132 0000017e  b753               STA     Q+2
133 00000180  b756               STA     Q+5
134 00000182  be65               LDX     DAY             DAY OF WEEK
135 00000184  271c               BEQ     DISPJ           ZERO ?
136 00000186  e651               LDA     Q,X             NO, GET DIGIT
137 00000188  aa20               ORA     #$20            SET BIT FOR ANNUNCIATOR
138 0000018a  e751               STA     Q,X             PUT BACK
139 0000018c  2014               BRA     DISPJ
140
141 0000018e  b669     DISP3   LDA     ASEC            ALARM SECONDS
142 00000190  ad14               BSR     SPLIT
143 00000192  b66a               LDA     AMIN            ALARM MINUTES
144 00000194  ad10               BSR     SPLIT
145 00000196  b66b               LDA     AHOUR           ALARM HOURS
146 00000198  ad0c               BSR     SPLIT
147 0000019a  a60a               LDA     #$0A
148 0000019c  b753               STA     Q+2
149 0000019e  a60f     OK        LDA     #$0F            BLANK SIXTH DIGIT
150 000001a0  b756               STA     Q+5
151 000001a2  cd02a1   DISPJ     JSR     DISP
152 000001a5  80                 RTI
153
154 000001a6  b75b     SPLIT     STA     W2              EXTRACT 2 PACKED BCD
155 000001a8  a40f               AND     #$0F            DIGITS AND PUT INTO Q
156 000001aa  5a                 DECX
157 000001ab  e751               STA     Q,X             LS BYTE
158 000001ad  b65b               LDA     W2
159 000001af  44                 LSRA
160 000001b0  44                 LSRA
161 000001b1  44                 LSRA
162 000001b2  44                 LSRA
163 000001b3  a40f               AND     #$0F            MS BYTE
164 000001b5  5a                 DECX
165 000001b6  e751               STA     Q,X
166 000001b8  5a                 DECX
167 000001b9  81                 RTS
```

rtc4.s05

```
169                                     ***************************************************
170                                     *                                                 *
171                                     *       Button 1 routines.                        *
172                                     *                                                 *
173                                     ***************************************************
174
175 000001ba  cd0285                    BUT1    JSR     DELAY           DEBOUNCE
176 000001bd  0b01fd                            BRCLR   5,PORTB,*       STAY UNTIL KEY RELEASED
177 000001c0  015003                            BRCLR   0,STAT,SK2      SETUP MODE
178 000001c3  cc01e9                            JMP     SET             YES
179 000001c6  0f010c                    SK2     BRCLR   7,PORTB,NOA     ALARM ?
180 000001c9  1f01                              BCLR    7,PORTB         YES, CANCEL IT
181 000001cb  a601                              LDA     #1
182 000001cd  b75a                              STA     W1
183 000001cf  a6bc                              LDA     #$BC
184 000001d1  cd02d4                            JSR     CCONLY          CLOCK OUT LOW
185 000001d4  80                                RTI
186
187 000001d5  3c59                      NOA     INC     DSPLY           NO, MOVE TO NEXT
188 000001d7  b659                              LDA     DSPLY           DISPLAY OPTION
189 000001d9  a106                              CMP     #$06
190 000001db  2602                              BNE     NOT6            TOO FAR ?
191 000001dd  3f59                              CLR     DSPLY           YES, GO BACK TO ZERO
192 000001df  cc010c                    NOT6    JMP     IRQ3
193
194                                     ***************************************************
195                                     *                                                 *
196                                     *       Button 1 setup function.                  *
197                                     *                                                 *
198                                     ***************************************************
199
200 000001e2  59592307311299            TABL1   FCB     $59,$59,$23,$07,$31,$12,$99
201
202 000001e9  1250                      SET     BSET    1,STAT          CHANGE MADE
203 000001eb  3c5c                              INC     W3              INCREMENT BYTE
204 000001ed  be5e                              LDX     W5              POINTER
205
206 000001ef  d601e2                            LDA     TABL1,X         MAXIMUM FOR REGISTER ?
207 000001f2  055003                            BRCLR   2,STAT,NAL      ALARM ?
208 000001f5  d601db                            LDA     TABL1-7,X       YES, OFFSET TABLE
209
210 000001f8  b15c                      NAL     CMP     W3              COMPARE MAX WITH ACTUAL
211 000001fa  2402                              BHS     NTB             MAX HIGHER OR SAME ?
212 000001fc  3f5c                              CLR     W3              NO, SO SET TO ZERO
213
214 000001fe  b65c                      NTB     LDA     W3              DECIMAL ADJUST
215 00000200  a40f                              AND     #$0F            LOOK AT LS NIBBLE
216 00000202  a10a                              CMP     #$0A            MORE THAN 9 ?
217 00000204  2508                              BLO     NOADJ           NO, DO NOTHING
218 00000206  a610                              LDA     #$10            YES, INC. MS NIBBLE
219 00000208  bb5c                              ADD     W3
220 0000020a  a4f0                              AND     #$F0            CLEAR LS NIBBLE
221 0000020c  b75c                              STA     W3
222 0000020e  b65c                      NOADJ   LDA     W3
223 00000210  204b                              BRA     DW5             DISPLAY NEW CONTENTS
```

rtc4.s05

```
                                ************************************************
                                *                                              *
                                *       Button 2 routine (set-up).             *
                                *                                              *
                                ************************************************

00000212  cd0285        BUT2    JSR     DELAY           DEBOUNCE
00000215  0d01fd                BRCLR   6,PORTB,*       STAY UNTIL KEY RELEASED
00000218  00500b                BRSET   0,STAT,REG      SETUP MODE ?
0000021b  cd02c6                JSR     INTOFF          NO, STOP INTERRUPTS
0000021e  1050                  BSET    0,STAT          AND GO TO SET-UP MODE
00000220  3f5e                  CLR     W5              INITIALISE POINTER
00000222  3a5e                  DEC     W5              FIRST INC GIVES ZERO
00000224  1350                  BCLR    1,STAT          CHANGE FLAG RESET
00000226  03500b        REG     BRCLR   1,STAT,NOSTOR   STORING

00000229  be5e                  LDX     W5              YES
0000022b  b65c                  LDA     W3
0000022d  e762                  STA     SEC,X           STORE NEW VALUE IN RAM
0000022f  ad5a                  BSR     RWSU1
00000231  cd02f2                JSR     WRITE           AND ALSO IN HC68T1

00000234  1350          NOSTOR  BCLR    1,STAT          CHANGE FLAG RESET
00000236  3c5e                  INC     W5              NEXT REGISTER
00000238  be5e                  LDX     W5
0000023a  a30a                  CPX     #$0A            TOO FAR ?
0000023c  2741                  BEQ     EXSET           YES, EXIT FROM SETUP

0000023e  a307                  CPX     #$07
00000240  2504                  BLO     U7              TIME REGISTER ?
00000242  1450                  BSET    2,STAT          NO, ALARM REGISTER
00000244  2007                  BRA     NORD            WRITE ONLY

00000246  1550          U7      BCLR    2,STAT          YES, TIME
00000248  ad41                  BSR     RWSU1           SO READ BYTE FROM RTC
0000024a  cd02f6                JSR     READ

0000024d  be5e          NORD    LDX     W5
0000024f  e662                  LDA     SEC,X           FETCH RAM DATA
00000251  b75c                  STA     W3
00000253  055007                BRCLR   2,STAT,DW5      IF ALARM THEN
00000256  ad33                  BSR     RWSU1           WRITE RAM DATA
00000258  cd02f2                JSR     WRITE           INTO 68HC68T1
0000025b  b65c                  LDA     W3
```

rtc4.s05

```
                                ****************************************************
                                *                                                  *
                                *       Set-up mode display.                       *
                                *                                                  *
                                ****************************************************

0000025d  b75b          DW5     STA     W2
0000025f  44                    LSRA
00000260  44                    LSRA
00000261  44                    LSRA
00000262  44                    LSRA
00000263  b757                  STA     Q+6             MS DIGIT
00000265  b65b                  LDA     W2
00000267  a40f                  AND     #$0F
00000269  b758                  STA     Q+7             LS DIGIT
0000026b  a60f                  LDA     #$0F
0000026d  b751                  STA     Q               CLEAR
0000026f  b752                  STA     Q+1             REST
00000271  b753                  STA     Q+2             OF
00000273  b754                  STA     Q+3             DISPLAY
00000275  b756                  STA     Q+5
00000277  be5e                  LDX     W5              REGISTER
00000279  bf55                  STX     Q+4             ADDRESS
0000027b  cd02a1                JSR     DISP
0000027e  80                    RTI

0000027f  1150          EXSET   BCLR    0,STAT          RETURN
00000281  cd02ca                JSR     INTON           TO NORMAL MODE
00000284  80            ALEN    RTI

00000285  aeff          DELAY   LDX     #$FF            DEBOUNCE DELAY
00000287  5a            AG      DECX
00000288  26fd                  BNE     AG
0000028a  81                    RTS

                                ****************************************************
                                *                                                  *
                                *       Read/write a byte to/from RAM at DPNT      *
                                *       from/to serial address ADDR.               *
                                *                                                  *
                                ****************************************************

0000028b  a601          RWSU1   LDA     #1
0000028d  b75a          RWSU    STA     W1
0000028f  a620                  LDA     #32
00000291  bb5e                  ADD     W5
00000293  a126                  CMP     #$26            IF GREATER THAN $26
00000295  2301                  BLS     NO6             INCREMENT TO SKIP
00000297  4c                    INCA                    UN-USED BYTE AT $27
00000298  b760          NO6     STA     ADDR
0000029a  a662                  LDA     #SEC
0000029c  bb5e                  ADD     W5
0000029e  b761                  STA     DPNT
000002a0  81                    RTS
```

rtc4.s05

```
325                                 ***************************************************
326                                 *                                                 *
327                                 *       Display contents of Q.                    *
328                                 *                                                 *
329                                 ***************************************************
330
331 000002a1  b601      DISP    LDA     PORTB           CLEAR
332 000002a3  a4f0              AND     #$F0            LS BYTE OF PORTB
333 000002a5  b701              STA     PORTB           IE DIGIT ADDRESS = 0
334 000002a7  ae08              LDX     #8
335 000002a9  090102            BRCLR   4,PORTB,AGAIN   ALARM ?
336 000002ac  1a51              BSET    5,Q
337 000002ae  e650      AGAIN   LDA     Q-1,X
338 000002b0  b702              STA     PORTC
339 000002b2  1701              BCLR    3,PORTB         LATCH
340 000002b4  1601              BSET    3,PORTB         DIGIT
341 000002b6  5a                DECX
342 000002b7  2704              BEQ     OUT             DONE ?
343 000002b9  3c01              INC     PORTB           NO, GOTO NEXT DIGIT
344 000002bb  20f1              BRA     AGAIN
345 000002bd  b601      OUT     LDA     PORTB
346 000002bf  a480              AND     #$80            DON'T CANCEL ALARM
347 000002c1  b701              STA     PORTB
348 000002c3  3f02              CLR     PORTC
349 000002c5  81                RTS
350
351                                 ***************************************************
352                                 *                                                 *
353                                 *       Control reg. init. & 12hr. formatting.    *
354                                 *                                                 *
355                                 ***************************************************
356
357 000002c6  a600      INTOFF  LDA     #%00000000
358 000002c8  2002              BRA     DOIT
359 000002ca  a61c      INTON   LDA     #%00011100      SET-UP CLOCK CONTROL
360 000002cc  b76e      DOIT    STA     ICREG           AND INTERRUPT CONTROL
361 000002ce  a602              LDA     #2
362 000002d0  b75a              STA     W1
363 000002d2  a6bc              LDA     #%10111100      ENABLE COUNTERS
364 000002d4  b76d      CCONLY  STA     CCREG           SELECT 32kHz CRYSTAL
365 000002d6  a631              LDA     #$31            CLOCK OUT DISABLED
366 000002d8  b760              STA     ADDR
367 000002da  ae6d              LDX     #CCREG
368 000002dc  bf61              STX     DPNT
369 000002de  2012              BRA     WRITE
370
371 000002e0  03590e    FORMAT  BRCLR   1,DSPLY,EXIT    12 HOUR DISPLAY MOD.
372 000002e3  2602              BNE     NOTMID          MIDNIGHT ?
373 000002e5  a612              LDA     #$12            YES, MAKE IT 12
374 000002e7  a112      NOTMID  CMP     #$12            NO, PM ?
375 000002e9  2306              BLS     EXIT            NO, DO NOTHING
376 000002eb  abee              ADD     #$EE            YES, SUBTRACT $12
377 000002ed  2902              BHCS    EXIT            USING HALF CARRY FOR
378 000002ef  a006              SUB     #$06            DEC. ADJUST OF 8 & 9PM
379 000002f1  81        EXIT    RTS
```

rtc4.s05

```
381                                 ***************************************************
382                                 *                                                 *
383                                 *       68HC68T1 serial routine (I/O PINS).       *
384                                 *                                                 *
385                                 ***************************************************
386
387 000002f2  1e60               WRITE   BSET    7,ADDR          BIT 7 HIGH
388 000002f4  2002                      BRA     SERT
389
390 000002f6  1f60               READ    BCLR    7,ADDR          BIT 7 LOW
391
392 000002f8  1e02               SERT    BSET    SS,PORTC        ENABLE HIGH (CPOL=0)
393
394 000002fa  0f0347                     BRCLR   7,PORTD,SPI     SELECT SERIAL LINK
395
396 000002fd  b660               PPSER   LDA     ADDR            SEND CHIP ADDRESS
397 000002ff  ad2c                       BSR     SHIFT           CHIP ADDRESS OUT
398 00000301  0e601b                     BRSET   7,ADDR,WRBUS    READ OR WRITE ?
399
400 00000304  be61               RDBUS   LDX     DPNT
401 00000306  a608                       LDA     #8
402 00000308  b75d                       STA     W4
403 0000030a  1002               LOOP2   BSET    SCK,PORTC       CLOCK HIGH
404 0000030c  0c0200                     BRSET   MISO,PORTC,*+3  DATA LINE (RESULT IN CARRY)
405 0000030f  1102                       BCLR    SCK,PORTC       CLOCK LOW
406 00000311  79                         ROL     0,X
407 00000312  3a5d                       DEC     W4
408 00000314  26f4                       BNE     LOOP2
409 00000316  3c61                       INC     DPNT
410 00000318  3a5a                       DEC     W1
411 0000031a  26e8                       BNE     RDBUS
412 0000031c  1f02                       BCLR    SS,PORTC        ENABLE LOW
413 0000031e  81                         RTS
414
415 0000031f  be61               WRBUS   LDX     DPNT            DATA BUFFER POINTER
416 00000321  f6                         LDA     0,X             DATA
417 00000322  ad09                       BSR     SHIFT
418 00000324  3c61                       INC     DPNT
419 00000326  3a5a                       DEC     W1              No. BYTES
420 00000328  26f5                       BNE     WRBUS
421 0000032a  1f02                       BCLR    SS,PORTC        ENABLE LOW
422 0000032c  81                         RTS
423
424 0000032d  ae08               SHIFT   LDX     #8              SHIFT OUT 8 BITS
425 0000032f  49                 SHIFT1  ROLA
426 00000330  2404                       BCC     SHIFT2          ZERO ?
427 00000332  1202                       BSET    MOSI,PORTC      NO, DATA = 1
428 00000334  2004                       BRA     SHIFT3
429 00000336  1302               SHIFT2  BCLR    MOSI,PORTC      DATA = 0
430 00000338  2000                       BRA     SHIFT3          DELAY
431 0000033a  1002               SHIFT3  BSET    SCK,PORTC       CLOCK HIGH
432 0000033c  1102                       BCLR    SCK,PORTC       CLOCK LOW
433 0000033e  1302                       BCLR    MOSI,PORTC      DATA LOW
434 00000340  5a                         DECX
435 00000341  26ec                       BNE     SHIFT1
436 00000343  81                         RTS
```

rtc4.s05

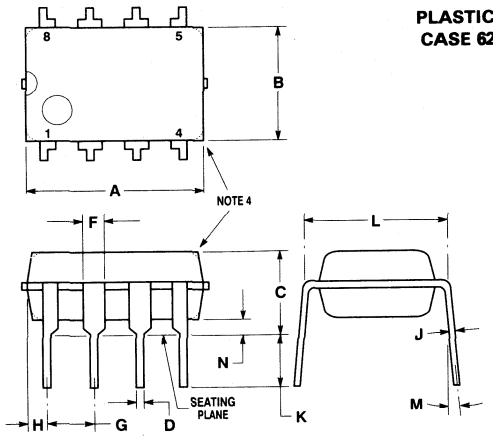
```
438                                  ****************************************************
439                                  *                                                  *
440                                  *       SPI serial routine.                        *
441                                  *                                                  *
442                                  ****************************************************
443
444 00000344  b660          SPI      LDA     ADDR            GET ADDRESS
445 00000346  b70c                   STA     SPD             SEND IT
446 00000348  0f0bfd                 BRCLR   7,SPSR,*        WAIT TILL FINISHED
447 0000034b  be61                   LDX     DPNT            LOCATION OF 1st BYTE
448 0000034d  f6            SPILP    LDA     0,X             GET IT
449 0000034e  b70c                   STA     SPD             SEND IT
450 00000350  0f0bfd                 BRCLR   7,SPSR,*        WAIT TILL FINISHED
451 00000353  0e6003                 BRSET   7,ADDR,SKIP     ARE WE WRITING ?
452 00000356  b60c                   LDA     SPD             NO, SO READ BYTE
453 00000358  f7                     STA     0,X             AND SAVE IT
454 00000359  5c            SKIP     INCX                    NEXT BYTE
455 0000035a  3a5a                   DEC     W1              DECREMENT COUNT
456 0000035c  26ef                   BNE     SPILP           FINISHED ?
457 0000035e  1f02          SPIP     BCLR    SS,PORTC        YES, ENABLE LOW
458 00000360  81                     RTS
459
460                                  ****************************************************
461                                  *                                                  *
462                                  *       Reset routine.                             *
463                                  *                                                  *
464                                  ****************************************************
465
466 00000361  3f01          RESET    CLR     PORTB
467 00000363  3f02                   CLR     PORTC
468 00000365  a68f                   LDA     #$8F            PORTB
469 00000367  b705                   STA     DDRB            4, 5, & 6 INTPUTS
470 00000369  a6bf                   LDA     #$BF            PORTC
471 0000036b  b706                   STA     DDRC            ALL OUTPUTS EXCEPT 6
472 0000036d  a655                   LDA     #%01010101      ENABLE SPI AS MASTER AT
473 0000036f  b70a                   STA     SPCR            500kHz, NO INTERRUPTS
474 00000371  cd02ca                 JSR     INTON           INIT TO 1Hz INTERRUPTS
475 00000374  3f50                   CLR     STAT
476 00000376  3f59                   CLR     DSPLY
477 00000378  8e            STOPP    STOP
478 00000379  20fd                   BRA     STOPP
479
480                                  ****************************************************
481                                  *                                                  *
482                                  *       MC68HC05C4 Vectors.                        *
483                                  *                                                  *
484                                  ****************************************************
485
486                                          ORG     $1FF4
487 00001ff4  0361                       FDB     RESET   SPI STATUS
488 00001ff6  0361                       FDB     RESET   SCI STATUS
489 00001ff8  0361                       FDB     RESET   TIMER
490 00001ffa  0100                       FDB     IRQ1    EXTERNAL INTERRUPT
491 00001ffc  0361                       FDB     RESET   SWI
492 00001ffe  0361                       FDB     RESET   RESET
493
494                                      END
```

Package Dimensions

1

Package availability and ordering information are given on the individual data sheets.

8-LEAD PACKAGE



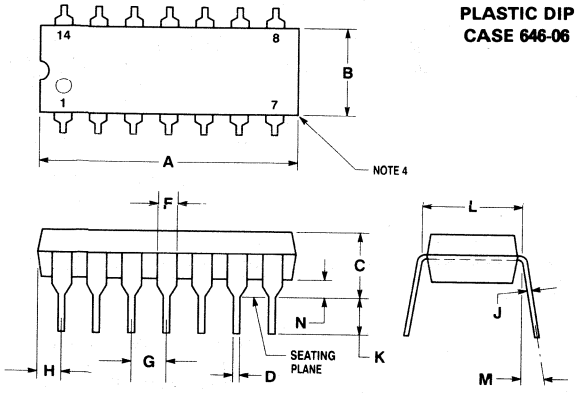
PLASTIC DIP
CASE 626-04

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.51	0.76	0.020	0.030

NOTES:
1. LEAD POSITIONAL TOLERANCE:
   ⌖ | ϕ0.13 (0.005) Ⓜ | T | A Ⓜ | B Ⓜ
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
4. DIMENSIONS A AND B ARE DATUMS.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

1

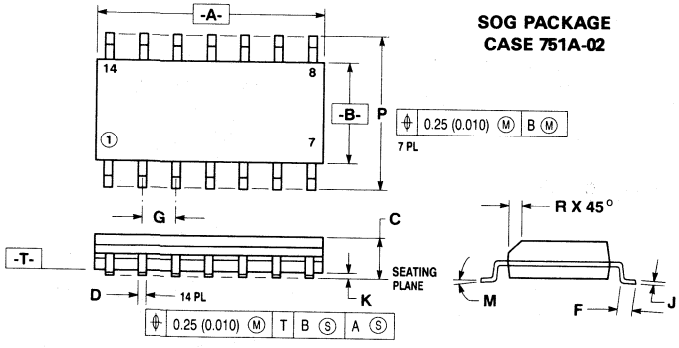
PLASTIC DIP
CASE 646-06



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.039

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

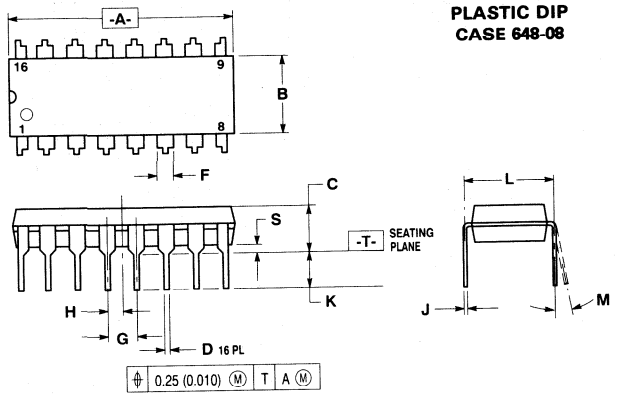
SOG PACKAGE
CASE 751A-02



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

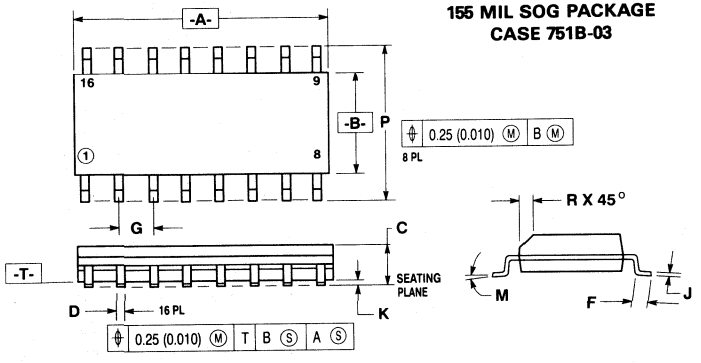
PLASTIC DIP
CASE 648-08



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

155 MIL SOG PACKAGE
CASE 751B-03

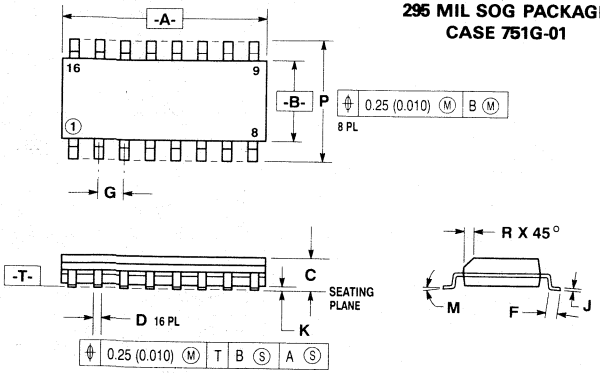


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

16-LEAD PACKAGES (Continued)

295 MIL SOG PACKAGE
CASE 751G-01

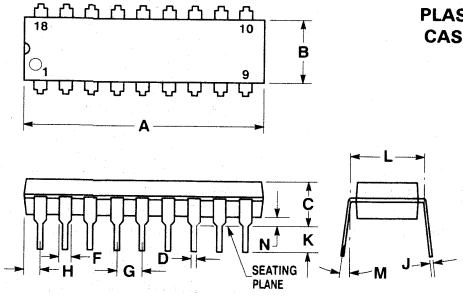


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

18-LEAD PACKAGE

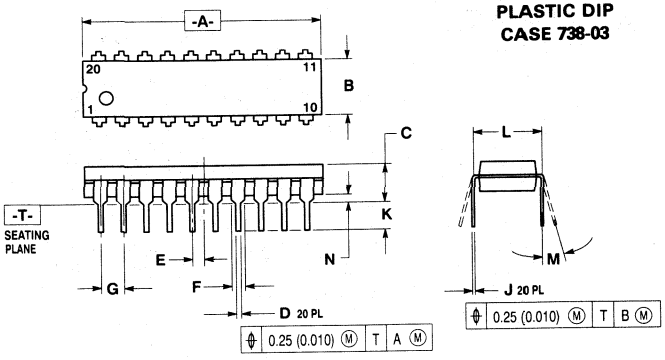
PLASTIC DIP
CASE 707-02



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

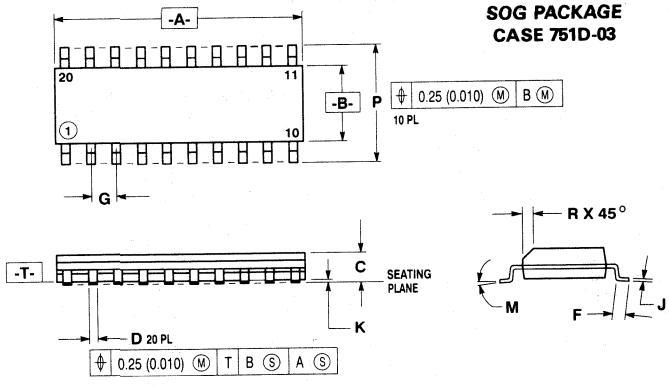
PLASTIC DIP
CASE 738-03



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	25.66	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.81	4.57	0.150	0.180
D	0.39	0.55	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.

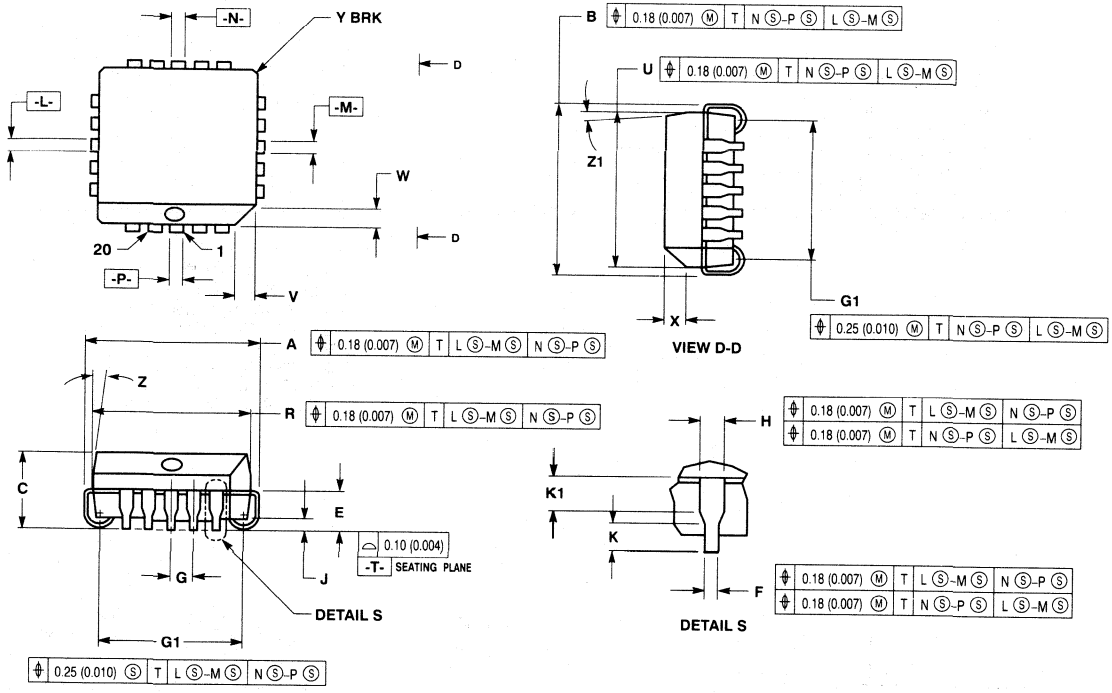
SOG PACKAGE
CASE 751D-03



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

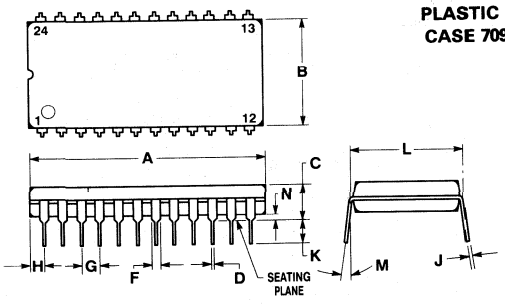
PLCC
CASE 775-02



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.78	10.03	0.385	0.395
B	9.78	10.03	0.385	0.395
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	8.89	9.04	0.350	0.356
U	8.89	9.04	0.350	0.356
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	7.88	8.38	0.310	0.330
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

NOTES:
1. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
2. DIM GI, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.

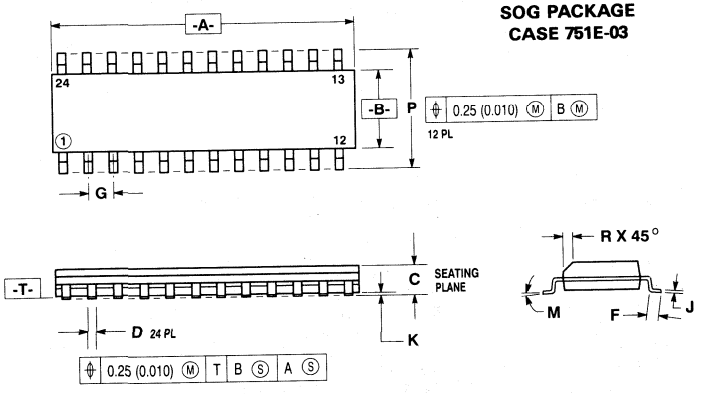
PLASTIC DIP
CASE 709-02



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

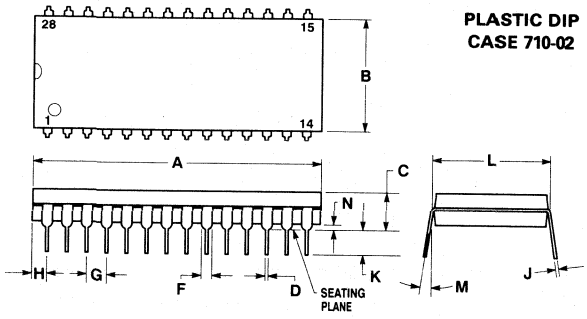
NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

SOG PACKAGE
CASE 751E-03



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.229	0.317	0.0090	0.0125
K	0.127	0.292	0.0050	0.0115
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

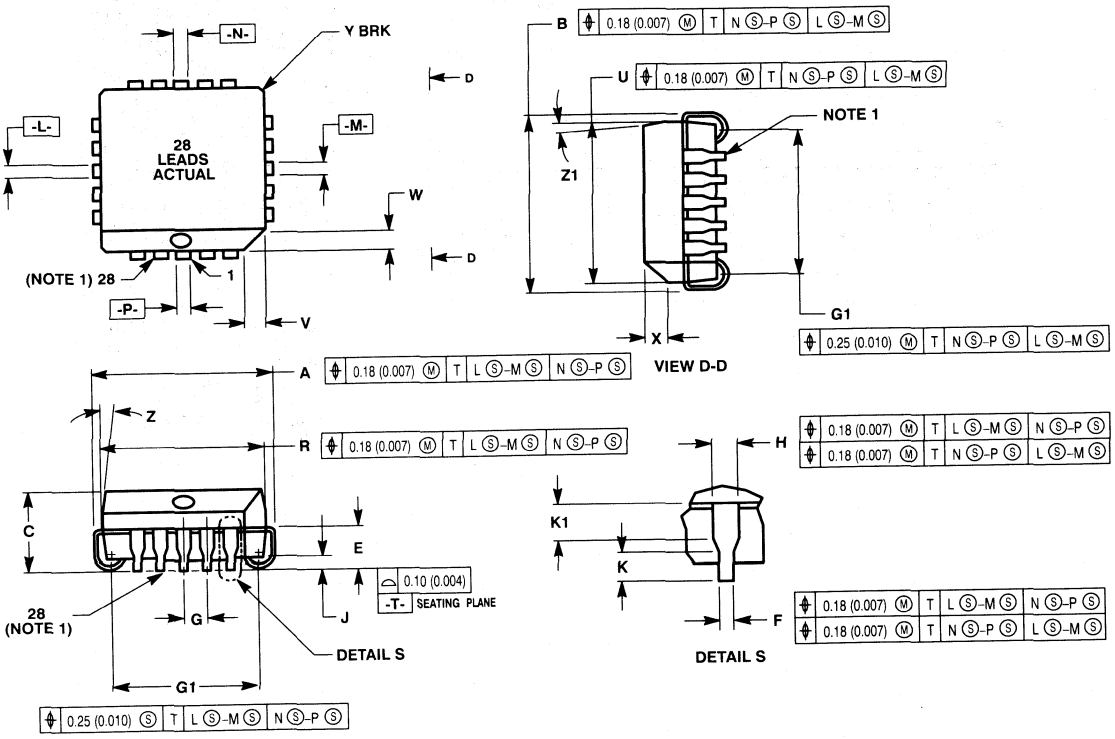


PLASTIC DIP
CASE 710-02

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

PLCC
CASE 776-02

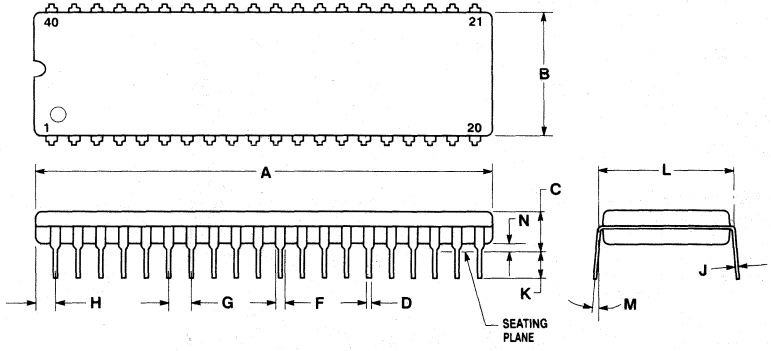


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.32	12.57	0.485	0.495
B	12.32	12.57	0.485	0.495
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	11.43	11.58	0.450	0.456
U	11.43	11.58	0.450	0.456
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	10.42	10.92	0.410	0.430
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

NOTES:
1. **DUE TO SPACE LIMITATION, CASE 776-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 28 LEADS.**
2. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.

40-LEAD PACKAGE

PLASTIC DIP
CASE 711-03

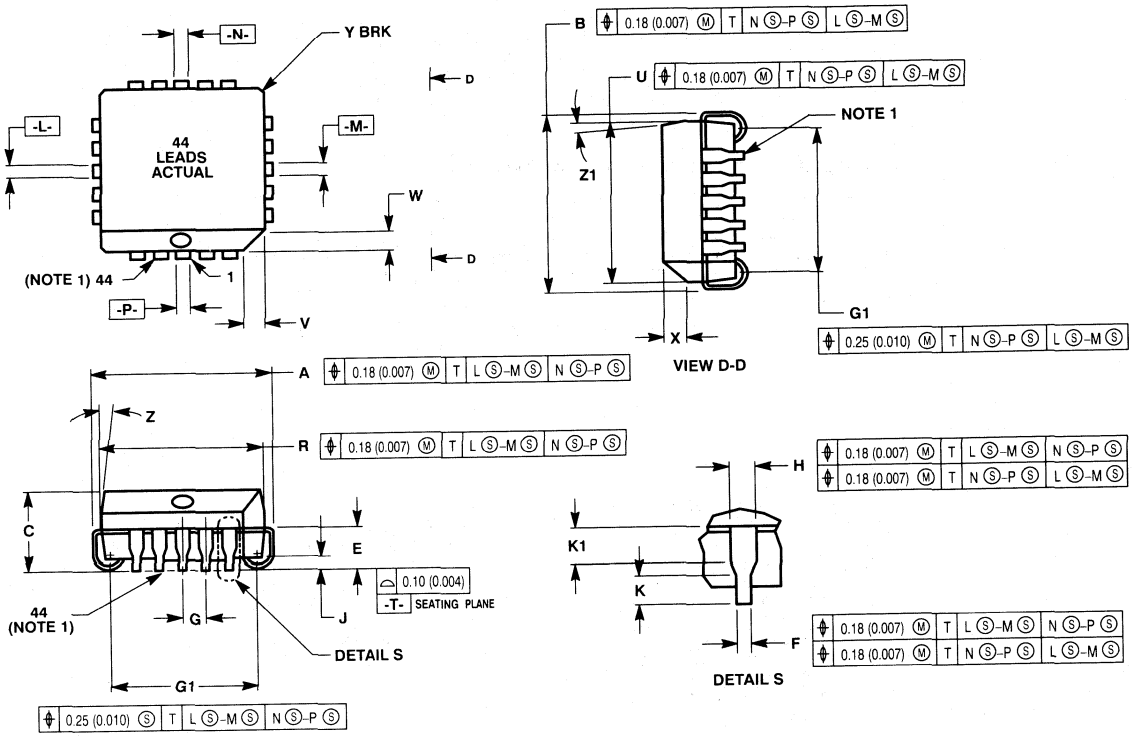


	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

44-LEAD PACKAGE

PLCC
CASE 777-02



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	17.40	17.65	0.685	0.695
B	17.40	17.65	0.685	0.695
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	16.51	16.66	0.650	0.656
U	16.51	16.66	0.650	0.656
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	15.50	16.00	0.610	0.630
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

NOTES:
1. **DUE TO SPACE LIMITATION, CASE 777-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 44 LEADS.**
2. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. *DIM R AND U DO NOT INCLUDE MOLD* PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.

Handling and Design Guidelines

ADCs/DACs

Decoders/Display Drivers

Operational Amplifiers/Comparators

PLL Frequency Synthesizers

Remote Control Functions

Smoke Detectors

Miscellaneous Functions

Reliability

Applications Information

Package Dimensions

Handling and Design Guidelines

ADCs/DACs

Decoders/Display Drivers

Operational Amplifiers/Comparators

PLL Frequency Synthesizers

Remote Control Functions

Smoke Detectors

Miscellaneous Functions

Reliability

Applications Information

Package Dimensions

A16682-8 PRINTED IN THE USA 11/90 13899 30,000 MOS DIG/ANLG YFAAA

MOTOROLA

Literature Distribution Centers:

USA: Motorola Literature Distribution; P.O. Box 20912, Phoenix, Arizona 85036.
EUROPE: Motorola Ltd.; European Literature Center, 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan.
ASIA PACIFIC: Motorola Semiconductors H.K. Ltd., Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.